IBIS in the Frequency Domain

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Agenda

Frequency Domain and Related Aspects

Area 1: Maximum Switching Frequency

Area 2: C_comp Stability

Area 3: Buffer Impedance and Passive Modeling

Area 4: Edge Rate vs. Switching Frequency

Summary

Frequency Domain Analysis

SI frequency domain (FD) analysis, modeling options are increasingly popular

- Interface speeds approaching microwave region
  - *Microwave methods migrating into SI world*
- FD analysis, popular for resonance/reflection detection, tends to be faster than time domain
- Tools, industry specifications now defining “channel-based” methods and requirements
  - *Serial ATA, PCI Express* loss requirements*
- S-parameters for interconnects (e.g., ICM)

How well does IBIS perform in these kinds of applications?

Key Areas for IBIS and FD

Several key areas should be considered when using IBIS in FD applications

1. Maximum switching frequency of the buffer
2. Variability of C_comp
3. Passive modeling of buffer impedance
4. Edge rate vs. switching frequency distinction

All these areas must be understood and checked to ensure IBIS is applicable.

These should be familiar to long-time users.

Area 1: Maximum Switching Frequency

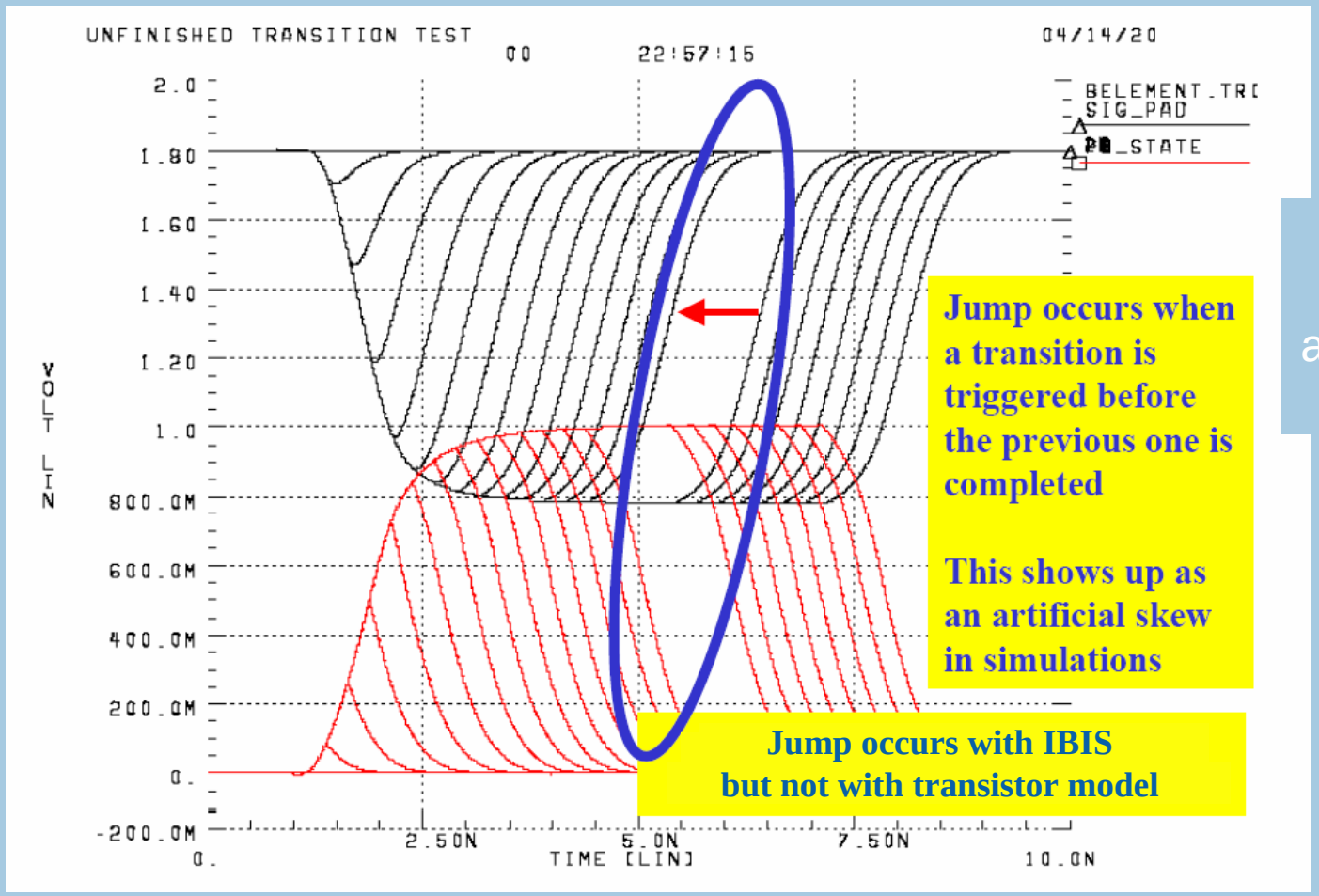
The maximum *switching* frequency for an IBIS model is:

$$Freq(Hz) \leq \frac{1}{2 * Vt\_table\_duration(seconds)}$$

- V-t *data* must start and end with settled DC voltages
  - *Enables matching to I-V load-line intercepts*
- Switching buffer more slowly than V-t duration avoids "switching into an unfinished edge"
- Some tools may be intelligent enough to cut V-t table data to include only transition information

Trying to "overclock" an IBIS model can lead to unpredictable results

Switching into an unfinished edge (review)



Accuracy compromised at inappropriate frequencies

Courtesy

Arpad Muranyi,

June 2003

Ad Hoc presentation

Issues with Switching Frequency

Not technically “in frequency domain”

- *Not analyzing buffer with periodic sinusoids but…*

For some interfaces, buffers may have limited ramp rates to reduce radiation

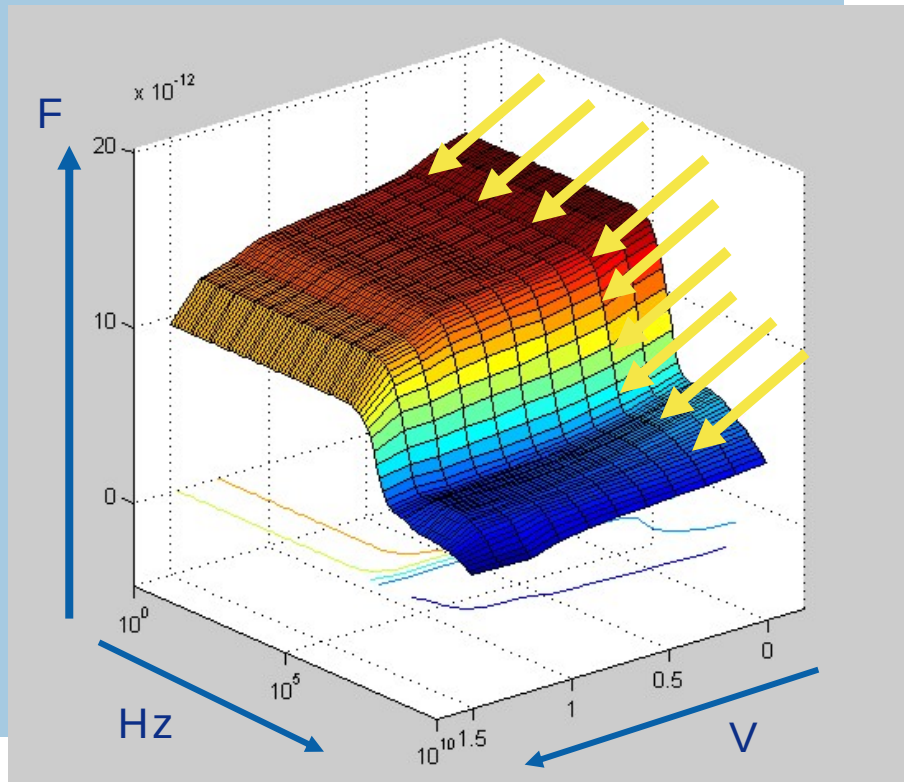
- *Nearest-neighbor coupling and EMI*
- *e.g. memory buses with high parallelism*

The maximum switching frequency is determined by the IBIS model data.

In the long term, IBIS overclocking is a tool equation and/or specification problem.

Area 2: C_comp

USB Buffer in the Frequency Domain



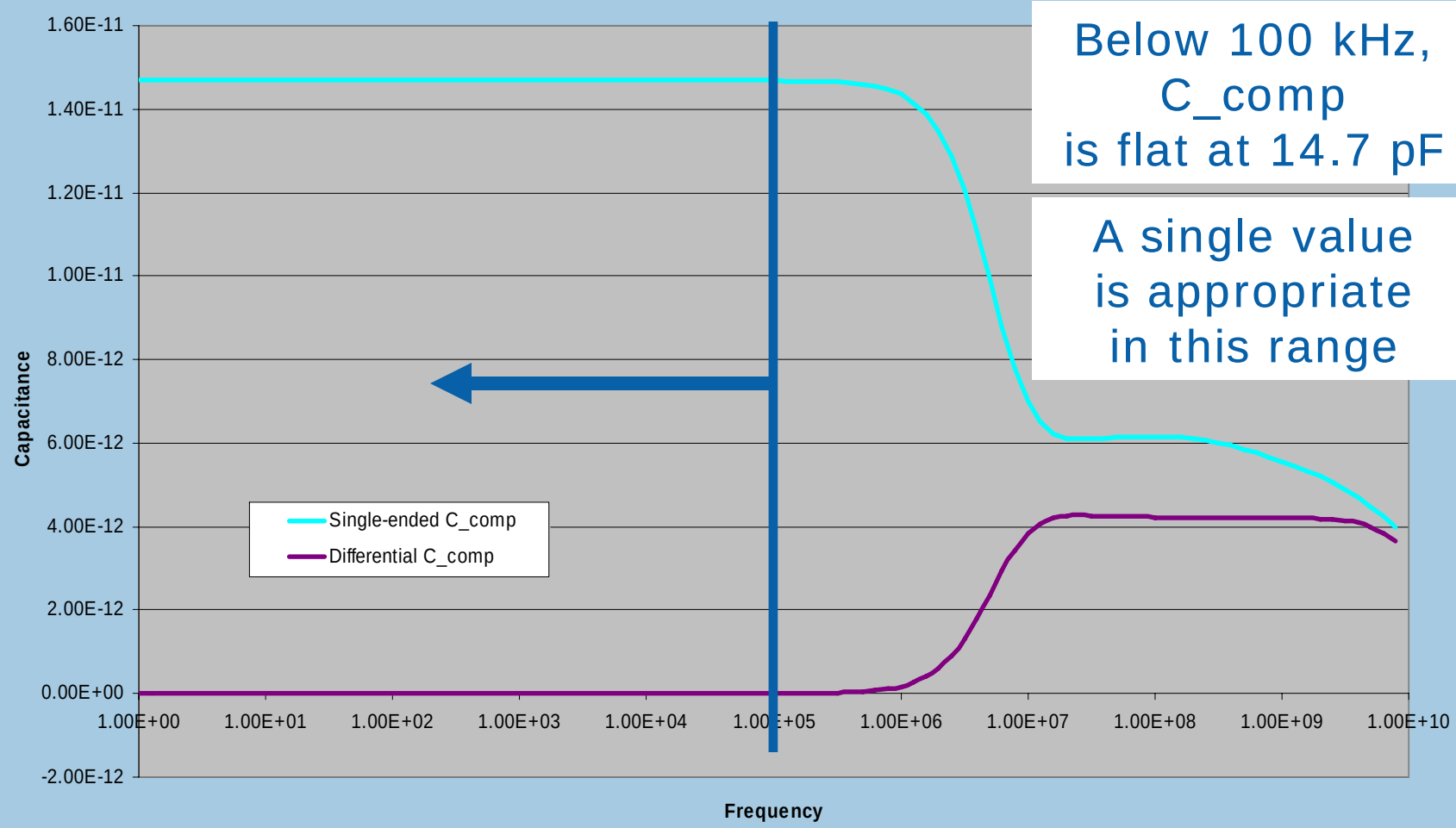
Buffer capacitance is, in part, frequency-dependent

A single value for C_comp may not be universally appropriate for all applications

Can we define a *limited* region where a single value of C_comp is appropriate?

Slice across the C_comp profile…

Area 2: C_comp at 0.3 V



 * Other names and brands may be claimed as the property of others

Issues with C_comp

C_comp is dependent on more than frequency

- Voltage
- Buffer state (high, low, high-impedance)
- See presentations from Giacotto, Mirmak, Muranyi

"Flat" C_comp may be effectively useless

- Based on edge rate and switching frequency (Area 4)
- e.g., USB switches at 1.5 MHz and above

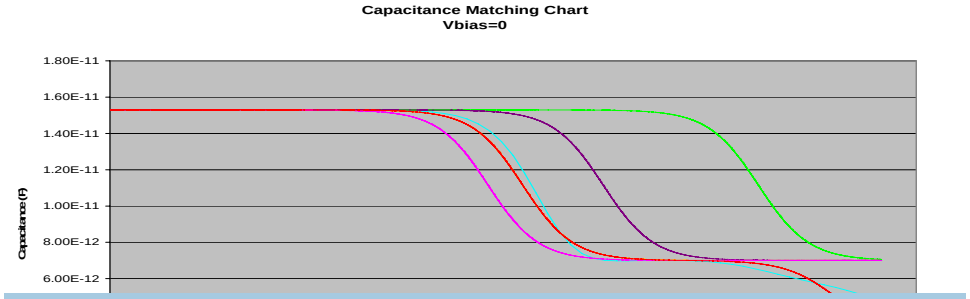
This is a specification-level problem.
C_comp tables? Equations? AMS?

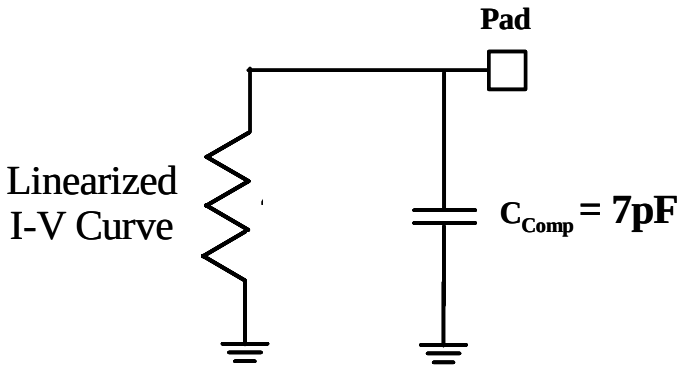
Area 3: Buffer Impedance & Passive Modeling

Related to C_comp

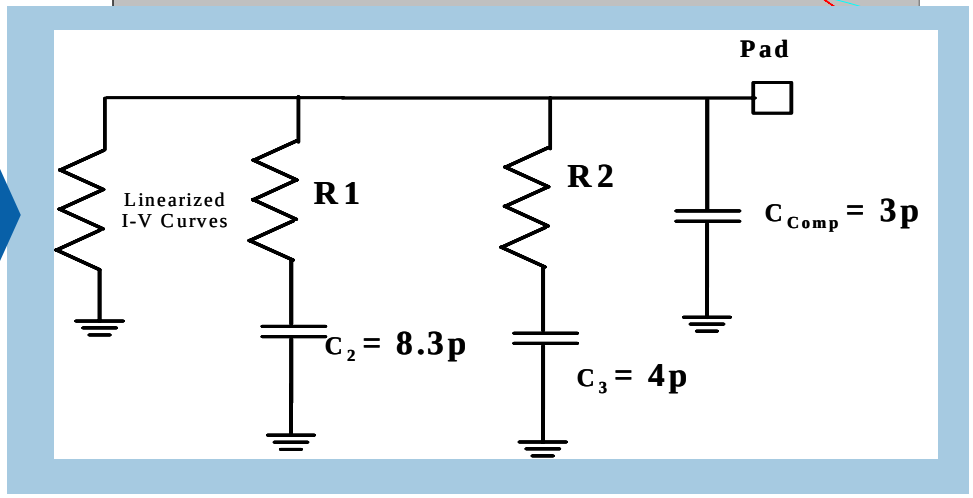
- C_comp is a limited expression of buffer reactance or imaginary portion of total impedance
- I-V tables are the real portion of total impedance, taken at DC

Perform a FD sweep and create a passive model to match behavior





IBIS Equivalent Circuit
(clamps omitted)



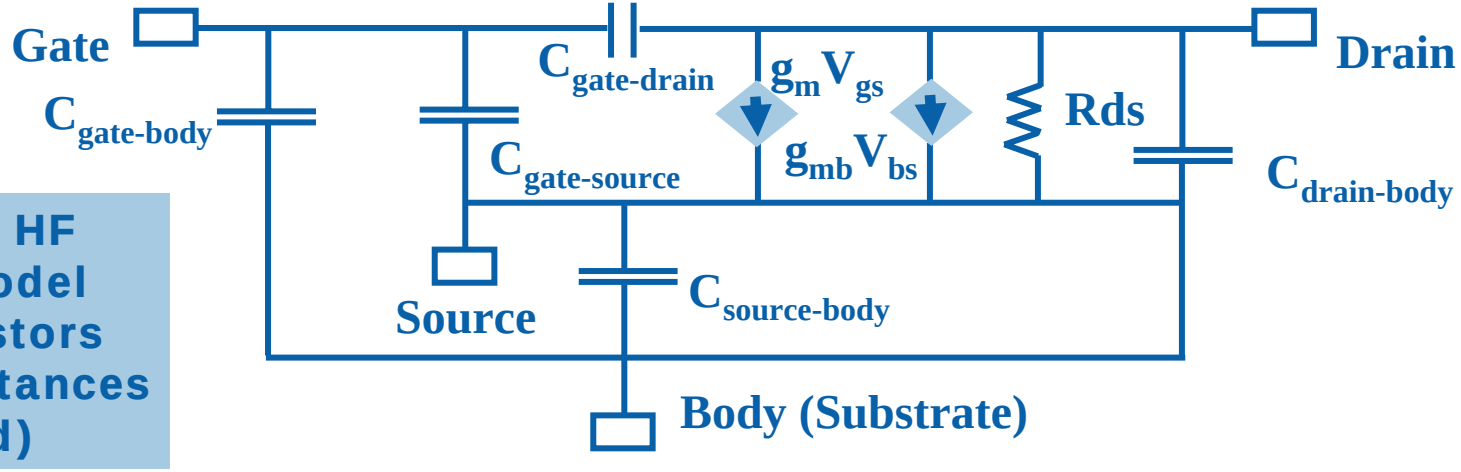
Problems with FD Passive Modeling

Recall C_comp issues

- *Values of R, C change with state, voltage, frequency*
- *Multiple circuit model may be needed; how to transition?*

Passive modeling even of RX buffers questionable

- *See transistor theory: AC model and dependent sources*
- *Also, for TX, see A. Muranyi on gate modulation*



Common HF circuit model for transistors (some resistances omitted)

Need new fundamental buffer circuit model for IBIS

Area 4: Edge Rate vs. Switching Frequency

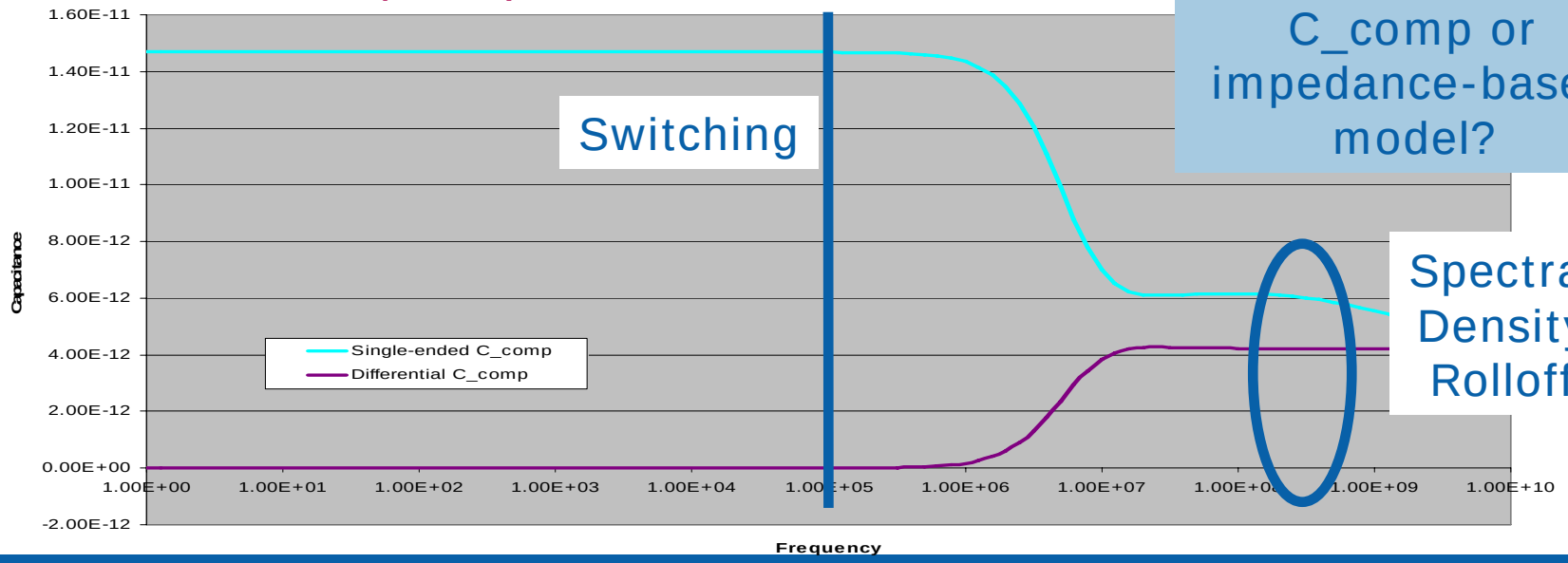
"Maximum frequency" is a vague term

- *Must distinguish between switching and harmonic content*
- *Energy spectral density (Fknee) from edge rate is a useful metric*

An extreme example (alteration of USB scenario)

- *A 100 kHz interface with ~650 ps edge rate*
- *V-t tables should be 5 µs or shorter in duration*
- *BUT knee frequency ~530-770 MHz!*

Which frequency range is "right" for C_comp or impedance-based model?



Edge Rate and Switching

Classic example: System Management Bus (SMBus)*

- *Operating frequency: 10-100 kHz*
- *Rise, fall time maxima between 300 - 1000 ns; no minima*
- *Bus capacitive load maximum per segment: 400 pF*
- *Slow edge rate means lumped load design rules can be used for lines up to 250" in length*
  - No simulations required so long as bus load limited
- *What happens with a "fast" buffer (5 ns edge)?*
  - Interconnects over 5" in length become distributed
  - Must use sim tool, plus spec becomes inappropriate

A problem for IBIS & modeling

- *What load should be used for Ramp, V-t, Vmeas?*
- *Loads for lumped assumption good for distributed system?*

Buffer design, buffer model AND specification must be consistent with interface needs

Summary

IBIS usage changes with FD analysis, increasing frequencies

- *Consumers must use models appropriately*
  - Observe maximum edge rate, switching frequency limits
  - Recognize bounds on fundamental IBIS circuit model

Model & tool makers must keep frequency in mind

- *What behaviors need to be expressed?*
- *Are today's keywords expressive enough? (e.g. C_comp)*
- *AMS: What specific equations, data sets need inclusion in model examples and templates?*

Proposal: Change to complex impedance model for buffers using AMS. Use native IBIS for interface pass/fail criteria and measurements.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