WHAT CAN'T IBIS DO?

Michael Mirmak, DCPAE (michael.mirmak@intel.com)

IBIS Summit at DesignCon 2016

Santa Clara, CA

January 22, 2016

Legal Disclaimer

Notice: This document contains information on products in the design phase of development. The information here is subject to change without notice. Do not finalize a design with this information. Contact your local Intel sales office or your distributor to obtain the latest specification before placing your product order.

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO SALE AND/OR USE OF INTEL PRODUCTS, INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT, OR OTHER INTELLECTUAL PROPERTY RIGHT. Intel products are not intended for use in medical, life saving, or life sustaining applications. Intel may make changes to specifications, product descriptions, and plans at any time, without notice.

All products, dates, and figures are preliminary for planning purposes and are subject to change without notice.

Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

The code names Romley, Grantley, Brickland, Purley, Sandy Bridge, Ivy Bridge, Haswell, Skylake and Jordan Creek presented in this document are only for use by Intel to identify products, technologies, or services in development, that have not been made commercially available to the public, i.e., announced, launched or shipped. They are not "commercial" names for products or services and are not intended to function as trademarks.

Copies of documents which have an order number and are referenced in this document, or other Intel literature may be obtained by calling 1-800-548-4725 or by visiting Intel's website at http://www.intel.com.

Additional Disclaimer

The following is solely the opinion of the author and does not necessarily represent the policies or opinions of Intel Corporation or its subsidiaries.

Agenda

What IBIS Can Do (IBIS Coverage Today)

- The Three Areas of IBIS Coverage

Where Expansion is Needed

- Complex Impedances
- Feedback Support
- Improved Evaluation Criteria

Nice to Haves

- Executable Checking, or Golden Response to Golden Stimuli

Discussion

WHAT IBIS CAN DO

The Three Areas of IBIS Coverage

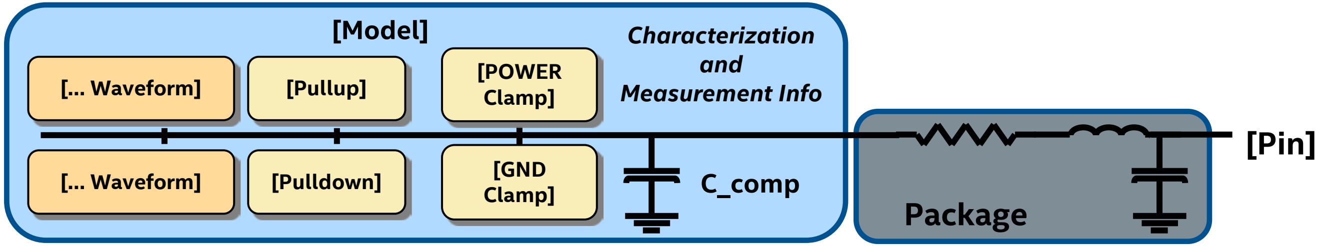
I/O buffers

- Traditional IBIS core: I-V, V-t, C_comp
- Multi-lingual code
- AMI

Packages

Evaluation criteria

- Input logic thresholds, etc.



WHAT IBIS CAN'T DO

Four Areas for Expansion

The major missing parts of IBIS:

- Advanced Packages – not discussed here, as was covered as part of Interconnect updates
- Complex Impedances
- Feedback Support
- Evaluation Criteria

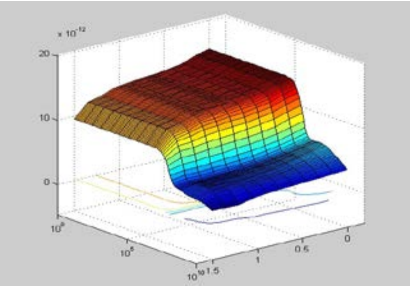
Other advancements are under active development and not mentioned here:

- Improved references (GND treatment)
- Backchannel adaptive equalization

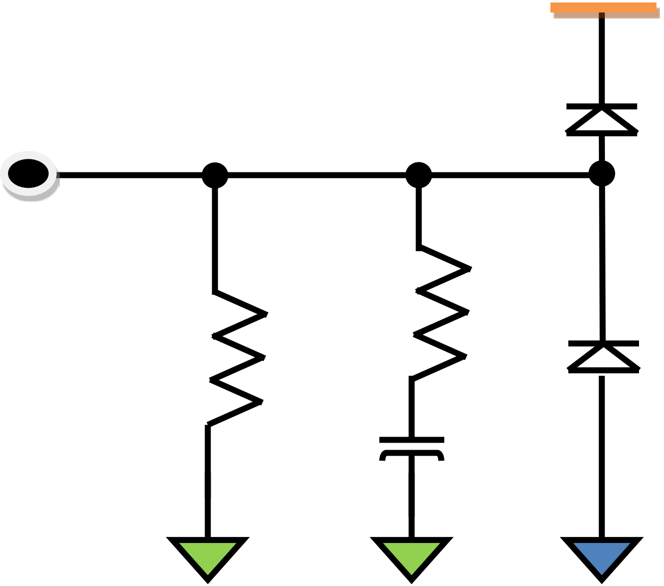
Complex Impedances

How do you represent an AC load (e.g., a complex impedance) in traditional IBIS?

- Behavior shows up in both memory (single-ended) and serial-differential buffers
- Needed for both drivers and receivers
- Ideally frequency- and voltage (state) dependent



Serial-differential buffer single-ended pad impedance plot of C (F) vs. F (Hz) and V (volts)

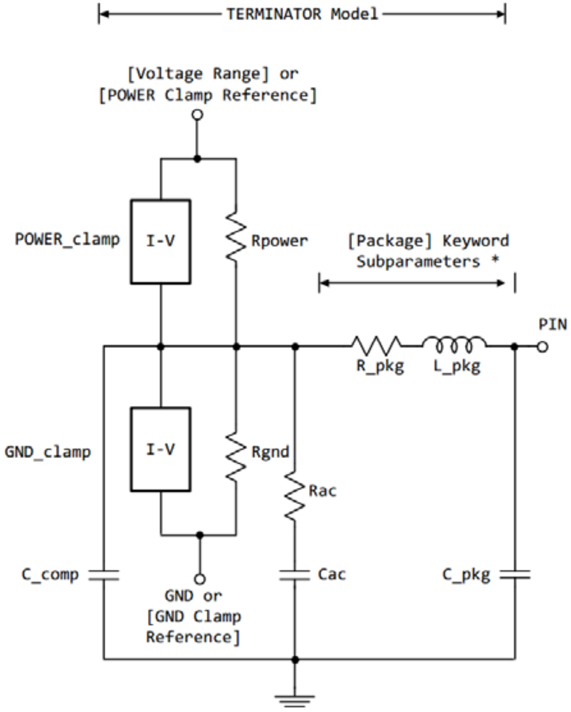


Model_Type Terminator Is Not Enough

For complex impedances, [Rac] and [Cac] are available, but require use of Model_type Terminator

Terminator limits the use of other IBIS features

- Input only, but with no input thresholds
- [Ramp] and [… Waveform] are therefore prohibited
- Prohibited with [Algorithmic Model]

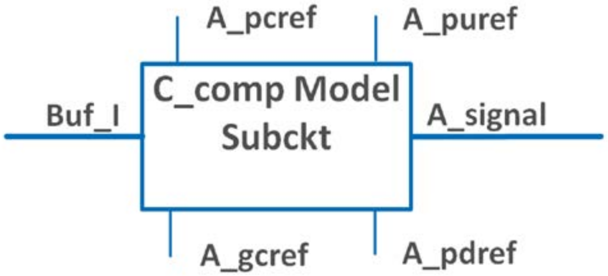


"When [Rgnd], [Rpower], or [Rac] and [Cac] are specified, the Model_type must be Terminator."

Proposals and Challenges

Randy Wolff summarized a proposed treatment from ATM and Interconnect

- "*Improved C_comp Model Case Study*", IBIS Summit at DesignCon 2015
- ISS-based subcircuit



Tricky points

- De-embedding for impedance in V-t, Ramp behaviors
- Separating "C_comp" from interconnect effects
- Accounting for state-dependence
- Measurement/correlation (separation from interconnect, rail effects)

Feedback

Traditional IBIS is a "snapshot"

- I-V data is non-transient, at a given state
- Ramp, V-t data cover state transitions, but with simplified relationship to I-V assumed (2EQ/2UK K-tables)

Approach breaks down if Miller capacitances are large

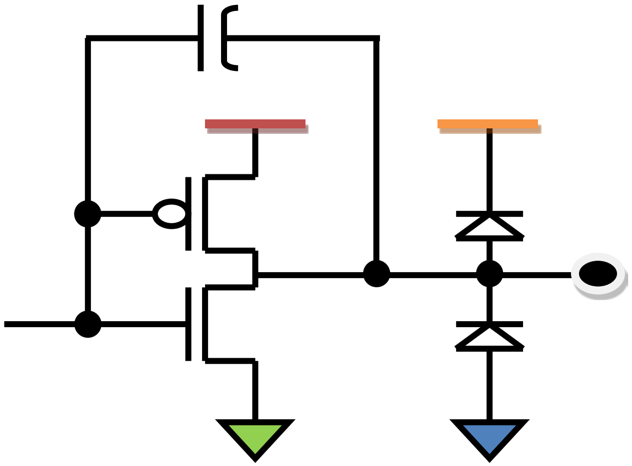
- Internal capacitance is sometimes added to deliberately slow down output edges for "fast" buffers used on "slow" interfaces

Problem part of 2EQ/2UK approach

- L. Giacotto, A. Muranyi, "A VHDL-AMS buffer model using IBIS v3.2 data" IBIS Summit at DAC 2003

Proposal for 3D surface macromodel treatment in:

- G. Signorini, "*Enhanced Macromodels for I/O Buffers*", IBIS Summit at EPEPS 2015 (also EPEPS paper)



Additional capacitance is deliberate here – see notes

Miller capacitance also exists but is effectively ignored in 2EQ/2UK K-table approach

Can we update IBIS [Model] core to include 3D surface approach?

Evaluation Criteria

What is the “goodness” of a signal (at the pad, pin, etc.)?

Supported criteria include:

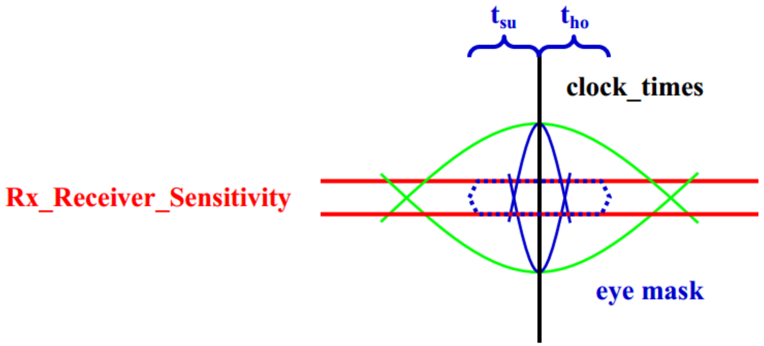
- Vih, Vil and variants to support hysteresis, DDR, etc.
- Included in [Model], [Model Spec], [Receiver Thresholds]

What’s missing? Serial-Differential Eye Support

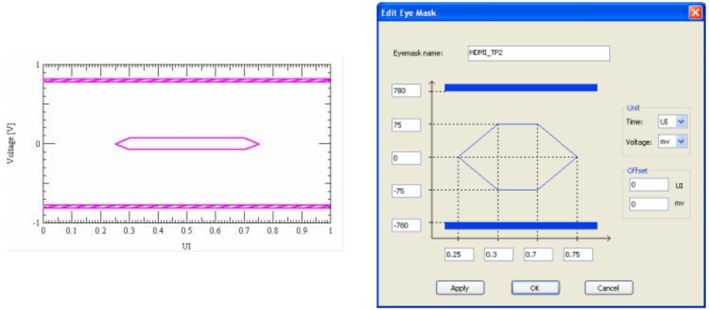
- Eye height, width, shape requirements
- Eye contour as function of BER (e.g., eye mask at target BER)
- Bathtub curves?

Eye masks have been proposed several times in the past:

- Yu Bao Meng – “*Eye Mask in IBIS*”, Asian IBIS Summits 2008
- Arpad Muranyi – “*Should IBIS Support Eye Mask Definitions?*”, DAC IBIS Summit 2012



from “*Should IBIS Support Eye Mask Definitions?*”



from “*Eye Mask in IBIS*”

Need BER-based eye masks at various measurement points

A “Nice to Have”: Algorithmic Checking

The IBISCHK parser checks .ibs (and related) file syntax

No method exists to check algorithmic models in a standardized way

Proposal: “golden input” and “golden output” definitions, similar to [Test Data]

- Optional, additional keywords (and files)
- Golden input: waveform data and configuration information
- Golden output: modified waveform data and parameters

Initial DLL checks proposed in IBIS Quality

- M. LaBonte, *IBISCHK Checks for IBIS-AMI DLL Integrity*
- Covers basic architecture, return value, and symbol table checks

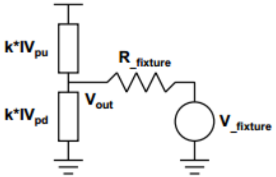
Parser DLL checks should be implemented with Golden Input/Output option

DISCUSSION

intel®

BACKUP

Assumption



$$0 = k_{pu}(t)\cdot IV_{pu}(V_{wfm1}(t)) - k_{pd}(t)\cdot IV_{pd}(V_{wfm1}(t)) - I_{out}(V_{wfm1}(t))$$

$$0 = k_{pu}(t)\cdot IV_{pu}(V_{wfm2}(t)) - k_{pd}(t)\cdot IV_{pd}(V_{wfm2}(t)) - I_{out}(V_{wfm2}(t))$$

- **$k_{pu}(t)$ and $k_{pd}(t)$ are assumed to be the same for the two different waveforms.**
- **Strictly speaking this is not true, because the pre-driver waveform is modified by the output waveform through the Miller capacitance, which makes $k_{pu}(t)$ and $k_{pd}(t)$ dependent on the derivative (dV/dt) of the output waveforms**

Vwfm1(t) and Vwfm2(t) are transitions in the same direction but using different V, R, loads

intel

6/23/2003

*Other brands and names are the property of their respective owners

Page 6

CPD

from L. Giacotto, A. Muranyi, "A VHDL-AMS buffer model using IBIS v3.2 data" IBIS Summit at DAC 2003