Fixing [Pin Mapping]

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IBIS Pin_name Signal_name Definitions

Keyword: **[Pin]**

Required: Yes

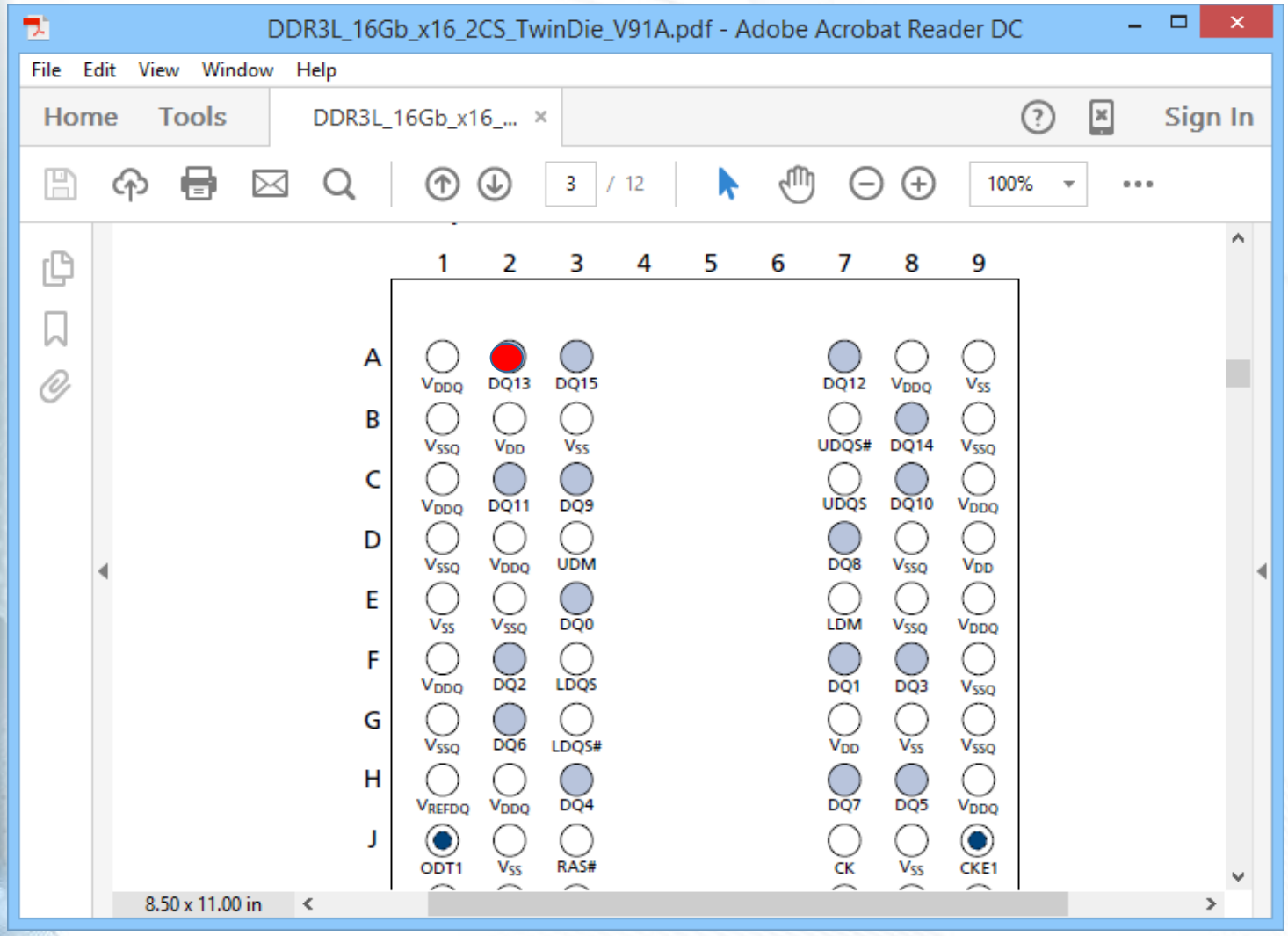
Description: Associates the component's I/O models to its various external pin names and signal names.

Sub-Params: signal_name, model_name, R_pin, L_pin, C_pin

Usage Rules: All pins on a component must be specified. The first column must contain the pin name. The second column, signal_name, gives the data book name for the signal on that pin. The third column, model_name, maps a pin to a specific I/O buffer model or model selector name. Each model_name must have a corresponding model or model selector name listed in a [Model] or [Model Selector] keyword below, unless it is a reserved model name (POWER, GND, or NC).

Note that "pin name" is also referred to as pin_name in IBIS. Other common names for pin_name in the industry are "pin number", "pin assignment", "ball assignment".

Example Data Book Pin_names and Signal_names DQ13 is Signal_name on Pin_name A2



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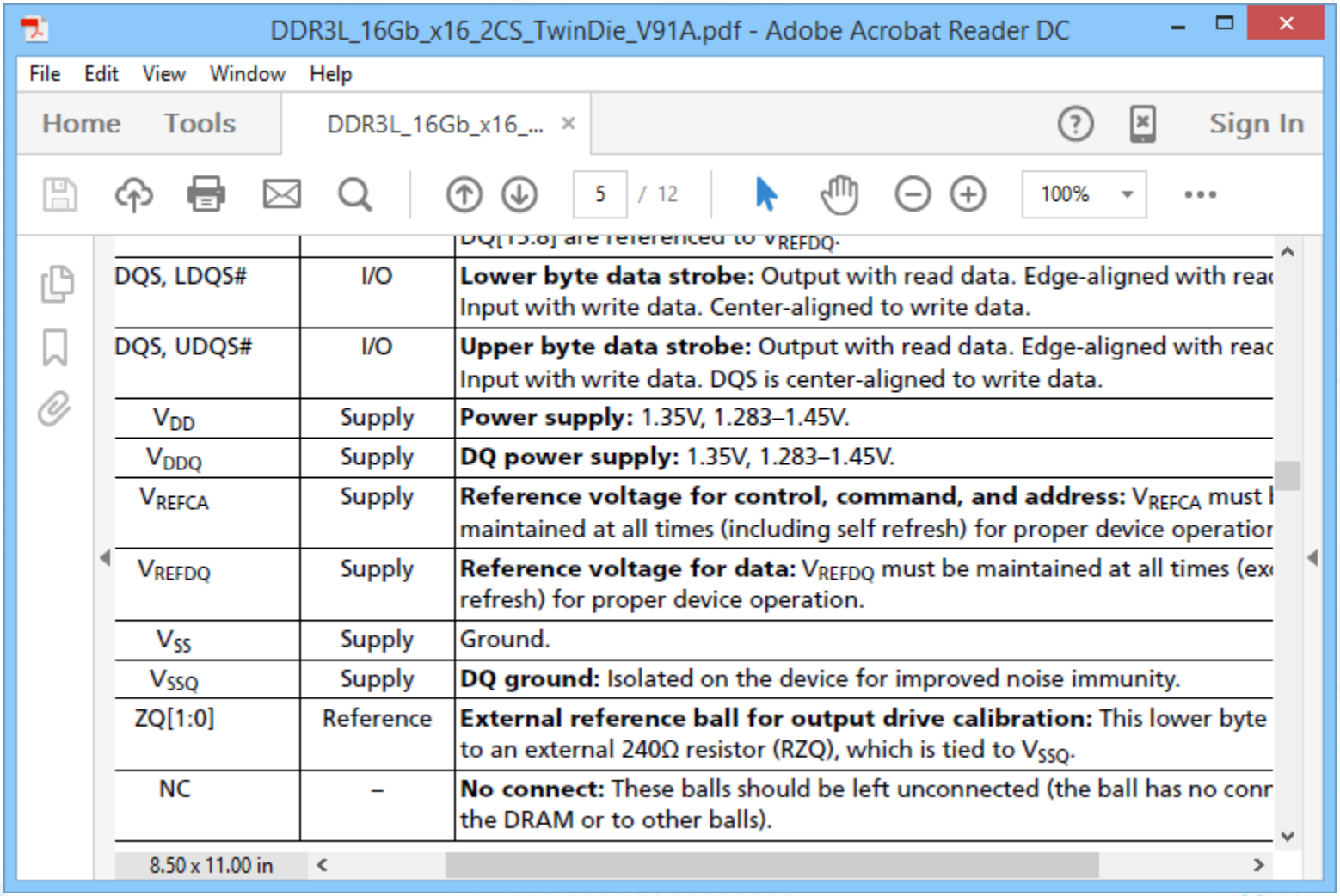
Data Associated with Signal_name



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Non – Power Aware IBIS Example

```
[IBIS Ver]     3.2
[File Name]    base.ibs
[File Rev]     1.1
[Component]      Memory
[Manufacturer]   SiSoft.
[Package]
R_pkg           265.4m      174.5m       406.4m
L_pkg           1.568nH     1.047nH      2.378nH
C_pkg           0.371pF     0.264pF      0.568pF
|
[Pin]  signal_name  model_name | Data Book Information
1      DM1          DM         | Rails are VDD and VSS
11     VDD          POWER      | DC Power Supply 1.2V 1.14-1.26V
12     VSS          GND        | Ground
|
[Model]          DQM
Model_type       Input
Vinl = 860.000mV
Vinh = 1060.000mV
C_comp                 1.100pF   1.000pF   1.200pF
[Voltage Range]        1.2000V   1.1400V   1.2600V
[Temperature Range]    50.0      110.0     0.0
[End]
```

Adding [Pin Mapping] Section Makes Model "Power Aware"

```
[Pin]  signal_name  model_name | Data Book Information
1      DM1          DM         | Rails are VDD and VSS
11     VDD          POWER      | DC Power Supply 1.2V 1.14-1.26V
12     VSS          GND        | Ground

[Pin Mapping] pulldown_ref pullup_ref gnd_clamp_ref power_clamp_ref ext_ref
1      VSS          VDD
11     NC           VDD
12     VSS          NC
```

The names in the [Pin Mapping] section are not signal_names, they are bus_labels. The following is equivalent to the above section. Making bus_labels the same as signal_name is the common method used in the industry.

```
[Pin Mapping] pulldown_ref pullup_ref gnd_clamp_ref power_clamp_ref ext_ref
1      xyz          def
11     NC           def
12     xyz          NC
```

Bus_label Indirection is Problematic IBIS CHK Reports No Errors:

```
[Pin]    signal_name  model_name   | Data Book Information
1        VDD          POWER        | DC Supply 1.2V 1.14-1.26V
2        VDDQ         POWER        | DC Supply 1.2V 1.14-1.26V
3        VDDQ         GND          | DC Supply 1.2V 1.14-1.26V
4        VPP          POWER        | DC Supply -1.2 +/1 0.1V
6        VSS          GND          | Ground
7        VSS          POWER        | Ground
10       DM1          DM           | Rails are VDD VSS
|
[Pin Mapping] pulldown_ref  pullup_ref gnd_clamp_ref power_clamp_ref ext_ref
1              NC            PWR
2              NC            PWR
3              GRND          NC
4              NC            PWR
6              GRND          NC
7              NC            PWR
10            GRND          PWR
```

- Signal_names VDDQ and VSS are both POWER and GND?
- Bus_label GRND shorts VDDQ and VSS
- Bus_label PWR shorts VDD, VDDQ, VPP, and VSS

Enhancements to IBIS

- New Rules
  - All pins with the same signal_name must have the same model_name
  - All POWER and GND pins with the same bus_label must have the same signal_name
- New [Pin Mapping] Option
  - New sub-parameter Signal_names_are_bus_labels
  - If set, then bus_label defaults to signal_name on POWER and GND pins
  - Can still partition pins, pads and buffers with the same signal_name into sub-groups using bus_labels

Signal_names_are_bus_labels Implies:

```
[Pin]    signal_name  model_name  | Data Book Information
1        VDD          POWER       | DC Supply 1.2V 1.14-1.26V
2        VDDQ         POWER       | DC Supply 1.2V 1.14-1.26V
3        VDDQ         POWER       | DC Supply 1.2V 1.14-1.26V
4        VPP          POWER       | DC Supply -1.2 +/- 0.1V
6        VSS          GND         | Ground
7        VSS          GND         | Ground
10       DM1          DM          | Rails are VDD VSS
|
[Pin Mapping] pulldown_ref  pullup_ref gnd_clamp_ref power_clamp_ref ext_ref
1             NC            VDD
2             NC            VDDQ
3             NC            VDDQ
4             NC            VPP
6             VSS           NC
7             VSS           NC
10            VSS           VDD
```

When using Signal_names_are_bus_labels, POWER and GND Pins not Required in [Pin Mapping]

```
[Pin]    signal_name  model_name   | Data Book Information
1        VDD          POWER        | DC Supply 1.2V 1.14-1.26V
2        VDDQ         POWER        | DC Supply 1.2V 1.14-1.26V
3        VDDQ         POWER        | DC Supply 1.2V 1.14-1.26V
4        VPP          POWER        | DC Supply -1.2 +/1 0.1V
6        VSS          GND          | Ground
7        VSS          GND          | Ground
10       DM1          DM           | Rails are VDD VSS
|
[Pin Mapping] pulldown_ref  pullup_ref gnd_clamp_ref power_clamp_ref ext_ref
Signal_names_are_bus_labels
10             VSS            VDD
```

Summary

- Signal_name defined as “Data Book Name” has consequences for power aware IBIS files and Power Deliver Networks.
- New rules are required to make [Pin Mapping] useable.
- Signal_names_are_bus_labels is a major simplification to [Pin Mapping]. I have not seen any [Pin Mapping] section that uses bus_labels other than signal_name.
  - Can still group pins, buffer supply terminals and die pads within a signal_name into bus_labels.