# Fixing [Pin Mapping]

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#### **Overview**

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- Summary



#### IBIS Pin\_name Signal\_name Definitions

#### Keyword: [Pin]

#### Required: Yes

*Description:* Associates the component's I/O models to its various external pin names and signal names.

Sub-Params: signal\_name, model\_name, R\_pin, L\_pin, C\_pin Usage Rules: All pins on a component must be specified. The first column must contain the pin name. The second column, signal\_name, gives the data book name for the signal on that pin. The third column, model\_name, maps a pin to a specific I/O buffer model or model selector name. Each model\_name must have a corresponding model or model selector name listed in a [Model] or [Model Selector] keyword below, unless it is a reserved model name (POWER, GND, or NC).

Note that "pin name" is also referred to as pin\_name in IBIS. Other common names for pin\_name in the industry are "pin number", "pin assignment", "ball assignment".

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#### Example Data Book Pin\_names and Signal\_names DQ13 is Signal\_name on Pin\_name A2

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Ш С				A		DQ13	DQ15				DQ12		∨ <sub>55</sub>					
				C								DQ14						
	•			D			UDM					Vssq					•	
				F														
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### Data Associated with Signal\_name

<b>7</b>	DDR3L_16Gb_x16_2CS_TwinDie_V91A.pdf - Adobe Acrobat Reader DC – 🗖 🗙								
File E	File Edit View Window Help								
Hon	ne Tools	DDR3L_160	Sb_x16 × ? 🔀 Sign In						
			DQ[15.0] are referenced to VREFDQ.						
ß	DQS, LDQS# I/O Lower byte data strobe: Output with read data. Edge-aligned with read Input with write data. Center-aligned to write data.								
	DQS, UDQS#	I/O	Upper byte data strobe: Output with read data. Edge-aligned with read Input with write data. DQS is center-aligned to write data.						
0	V <sub>DD</sub>	Supply	Power supply: 1.35V, 1.283–1.45V.						
	V <sub>DDQ</sub>	Supply	DQ power supply: 1.35V, 1.283-1.45V.						
	V <sub>REFCA</sub>	Supply	<b>Reference voltage for control, command, and address:</b> V <sub>REFCA</sub> must I maintained at all times (including self refresh) for proper device operation						
	VREFDQ Supply Reference voltage for data: VREFDQ must be maintained at all times (errefresh) for proper device operation.								
	V <sub>SS</sub>	Supply	Ground.						
	V <sub>SSQ</sub>	Supply	DQ ground: Isolated on the device for improved noise immunity.						
	ZQ[1:0] Reference External reference ball for output drive calibration: This lower byte to an external 240Ω resistor (RZQ), which is tied to V <sub>SSQ</sub> .								
	NC – <b>No connect:</b> These balls should be left unconnected (the ball has no the DRAM or to other balls).								
	8.50 x 11.00 in <								

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#### Non – Power Aware IBIS Example

[IBIS \	/er]	3.2				
[File N	Name]	base.i	bs			
[File H	Rev]	1.1				
[Compor	nent]	Memo	ory			
[Manufa	acturer]	SiSc	oft.			
[Packag	ge]					
R_pkg		265.4	m	174.	.5m	406.4m
L_pkg		1.568	BnH	1.04	l7nH	2.378nH
C_pkg		0.371	pF	0.26	54pF	0.568pF
1						
[Pin]	signal_	name	model_n	ame	Data Bo	ook Information
1	DM1		DM		Rails a	are VDD and VSS
11	VDD		POWER		DC Powe	er Supply 1.2V 1.14-1.26V
12	VSS		GND		Ground	
1						
[Model]	I	DQM				
Model_t	суре	Input				
Vinl =	860.000	mV				
Vinh =	1060.00	OmV				
C_comp			1.100p	F	1.000pF	1.200pF
[Voltag	ge Range	]	1.2000	V	1.1400V	1.2600V
[Tempe]	cature R	ange]	50.0		110.0	0.0
[End]						



## Adding [Pin Mapping] Section Makes Model "Power Aware"

VDD

NC

[Pin]	signal_name	model_name		Data Book Information
1	DM1	DM		Rails are VDD and VSS
11	VDD	POWER		DC Power Supply 1.2V 1.14-1.26V
12	VSS	GND		Ground
[Pin M	apping] pulldor	vn_ref pullup_r	ef	<pre>gnd_clamp_ref power_clamp_ref ext_ref</pre>
1	VSS	VDD		

The names in the [Pin Mapping] section are not signal\_names, they are bus\_labels. The following is equivalent to the above section. Making bus\_labels the same as signal\_name is the common method used in the industry.

[Pin	Mapping]	pulldown_ref pull	<pre>lup_ref gnd_clamp_ref power_clamp_ref ext_ref</pre>
1	хуz	def	
11	NC	def	
12	xyz	NC	

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NC

VSS

# Bus\_label Indirection is Problematic IBIS CHK Reports No Errors:

[Pin]	signal_name	model_name		Data Book Information
1	VDD	POWER	L	DC Supply 1.2V 1.14-1.26V
2	VDDQ	POWER		DC Supply 1.2V 1.14-1.26V
3	VDDQ	GND		DC Supply 1.2V 1.14-1.26V
4	VPP	POWER		DC Supply -1.2 +/1 0.1V
6	VSS	GND		Ground
7	VSS	POWER		Ground
10	DM1	DM		Rails are VDD VSS

[Pin Mapping] pulldown ref pullup ref gnd clamp ref power clamp ref ext ref

1	NC	PWR
2	NC	PWR
3	GRND	NC
4	NC	PWR
6	GRND	NC
7	NC	PWR
10	GRND	PWR

- Signal\_names VDDQ and VSS are both POWER and GND?
- Bus\_label GRND shorts VDDQ and VSS
- Bus\_label PWR shorts VDD, VDDQ, VPP, and VSS



### **Enhancements to IBIS**

#### New Rules

- All pins with the same signal\_name must have the same model\_name
- All POWER and GND pins with the same bus\_label must have the same signal\_name
- New [Pin Mapping] Option
  - New sub-parameter Signal\_names\_are\_bus\_labels
  - If set, then bus\_label defaults to signal\_name on POWER and GND pins
  - Can still partition pins, pads and buffers with the same signal\_name into sub-groups using bus\_labels



### Signal\_names\_are\_bus\_labels Implies:

[Pin]	signa	l_name	model_r	name	Data Book Information
1	VDD		POWER		DC Supply 1.2V 1.14-1.26V
2	VDDQ		POWER		DC Supply 1.2V 1.14-1.26V
3	VDDQ		POWER		DC Supply 1.2V 1.14-1.26V
4	VPP		POWER		DC Supply -1.2 +/- 0.1V
6	VSS		GND		Ground
7	VSS		GND		Ground
10	DM1		DM		Rails are VDD VSS
[Pin Ma	pping]	pulldown	_ref pul	lup_ref	f gnd_clamp_ref power_clamp_ref ext_ref
1		NC		VDD	
2		NC		VDDQ	
3		NC		VDDQ	
4		NC		VPP	
6		VSS		NC	
7		VSS		NC	
10		VSS		VDD	



# When using Signal\_names\_are\_bus\_labels, POWER and GND Pins not Required in [Pin Mapping]

[Pin]	signal_name	model_name	Data Book Information
1	VDD	POWER	DC Supply 1.2V 1.14-1.26V
2	VDDQ	POWER	DC Supply 1.2V 1.14-1.26V
3	VDDQ	POWER	DC Supply 1.2V 1.14-1.26V
4	VPP	POWER	DC Supply -1.2 +/1 0.1V
6	VSS	GND	Ground
7	VSS	GND	Ground
10	DM1	DM	Rails are VDD VSS

[Pin Mapping] pulldown\_ref pullup\_ref gnd\_clamp\_ref power\_clamp\_ref ext\_ref Signal\_names\_are\_bus\_labels

10 VSS VDD



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### Summary

- Signal\_name defined as "Data Book Name" has consequences for power aware IBIS files and Power Deliver Networks.
- New rules are required to make [Pin Mapping] useable.
- Signal\_names\_are\_bus\_labels is a major simplification to [Pin Mapping]. I have not seen any [Pin Mapping] section that uses bus\_labels other than signal\_name.
  - Can still group pins, buffer supply terminals and die pads within a signal\_name into bus\_labels.

