Simulate IBIS Data with Free Spice

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Agenda:

- Motivations & Goals
- IBIS data in Spice: Schematic, Implementation & Correlation
  - Review: Ramp based
  - New: Waveform based
    - Icct & Composite current
- Summary
- Future work
- Q & A

Motivation:

- Enable EDA vendor neutral IBIS release
- Enable SI analysis with free simulators
  - Spice3f5 based: NGSpice, ElSpice etc
  - They do NOT have IBIS implementation
- Explicit IBIS algorithms implementation
  - Behavioral modeling in spice
  - Using stock simulators, published algorithms
  - Minimum programming required

Goals:

- Run on Spice3f5 based simulator
  - Using mainly: ASRC source (Arbitrary Source)
    - A generalized non-linear dependent source, detailed in next slide
- Support up to IBIS V5.1 model
  - Ramp, IV/VT Waveform
  - Icct/Composite current
- Very good correlation

Background: ASRC

5.1 Bxxxx: Nonlinear dependent source (ASRC)

5.1.1 Syntax and usage

General form:

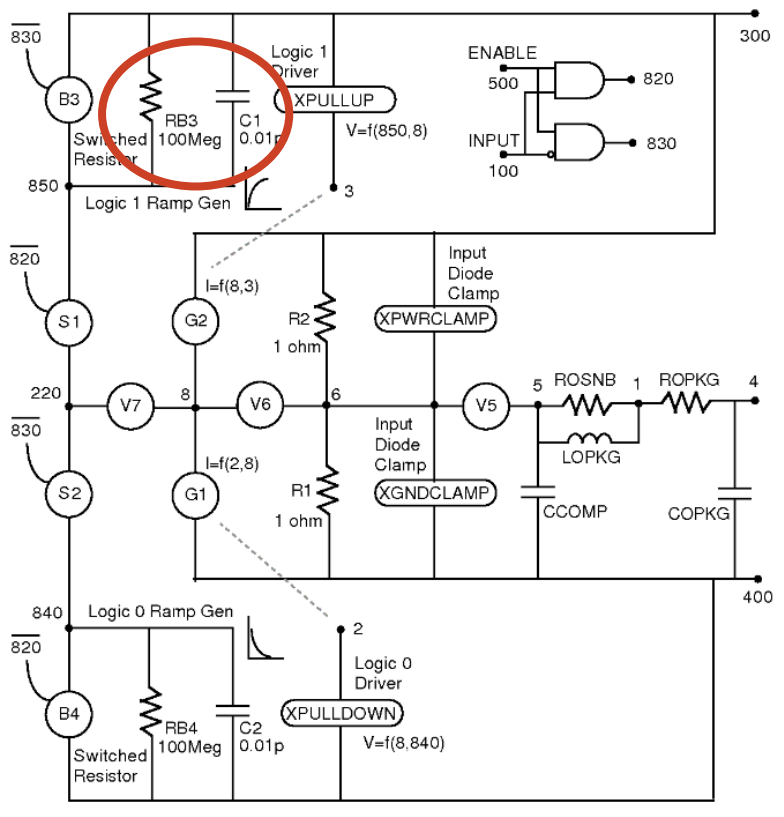
```
BXXXXXXX n+ n- <i=expr> <v=expr> <tc1=value> <tc2=value>
+ <temp=value> <dtemp=value>
```

Examples:

```
B1 0 1 I=cos(v(1))+sin(v(2))
B2 0 1 V=ln(cos(log(v(1,2)^2))) -v(3)^4+v(2)^v(1)
B3 3 4 I=17
B4 3 4 V=exp(pi^i(vdd))
B5 2 0 V = V(1) < {Vlow} ? {Vlow} : V(1) > {Vhigh} ? {Vhigh} : V(1)
```

“time” (simulation time) can also be a variable... **[Ref.1]**

Ramp based: [Schematic]



[Ref.2]

Ramp based: [Implementation]

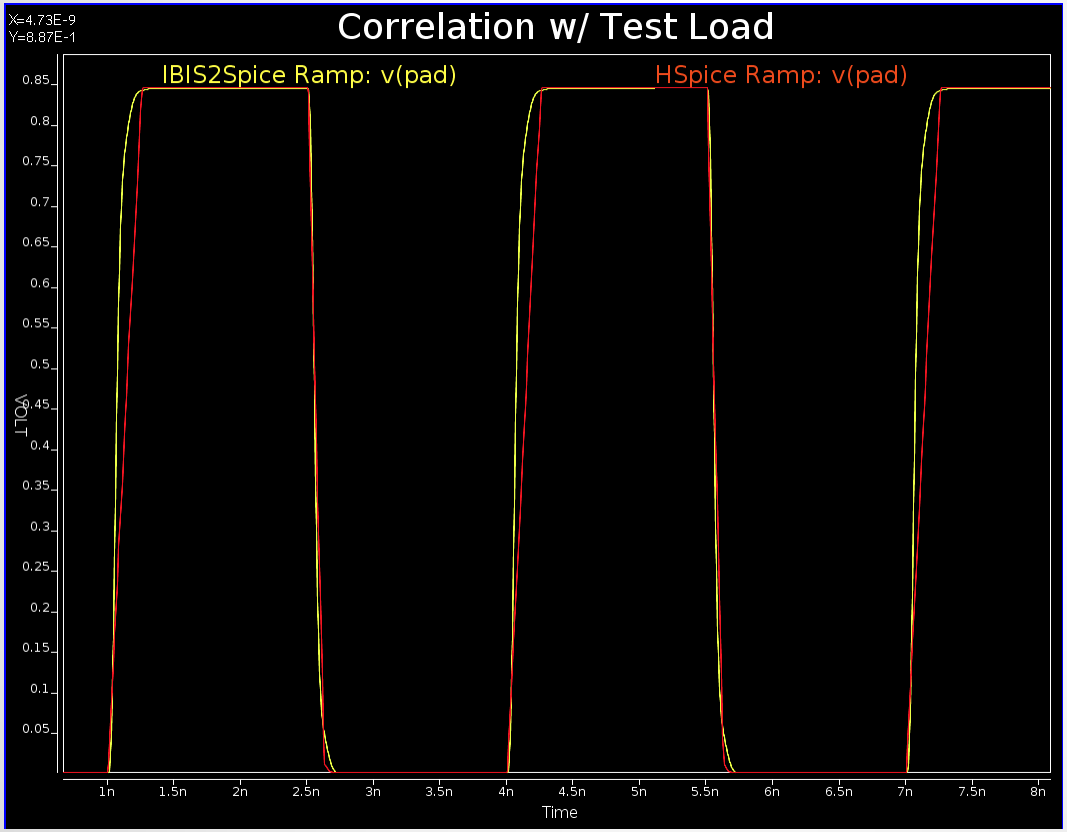
```
* RAMP RATE CONTROL
* RISERMP = 3.0382E4 = 508.001mV/154.343ps
* FALLRMP = 2.8194E4 = 491.237mV/138.500ps

B3 NVCC N850 I= V(N830) > 0.5 ? 0 : V(NVCC, N850) / 2.8194E4
B4 N840 NVSS I= V(N820) > 0.5 ? 0 : V(N840, NVSS) / 3.0382E4
```

```
* PU BRANCH
.SUBCKT DQ_34_1066_PULLUP_MIN 3 4 1 2
B1 3 4 V =
+ (V(1,2) < -1.5000E0)? 5.4653E-3:
+ (V(1,2) < -1.4700E0)? 1.4682E-2 * V(1,2) + 2.7488E-2:
+ (V(1,2) < -1.4650E0)? 1.5490E-2 * V(1,2) + 2.8676E-2:
```

```
* PC BRANCH
.SUBCKT DQ_34_1066_POWER_CLAMP_MIN 3 4 1 2
B1 3 4 I =
+ (V(1,2) < -1.5000E0)? 1.0467E-1:
+ (V(1,2) < -1.4950E0)? -1.7193E-1 * V(1,2) - 1.5323E-1:
+ (V(1,2) < -1.4900E0)? -1.7084E-1 * V(1,2) - 1.5160E-1:
```

[Ref.3]

Ramp based: [Correlation]



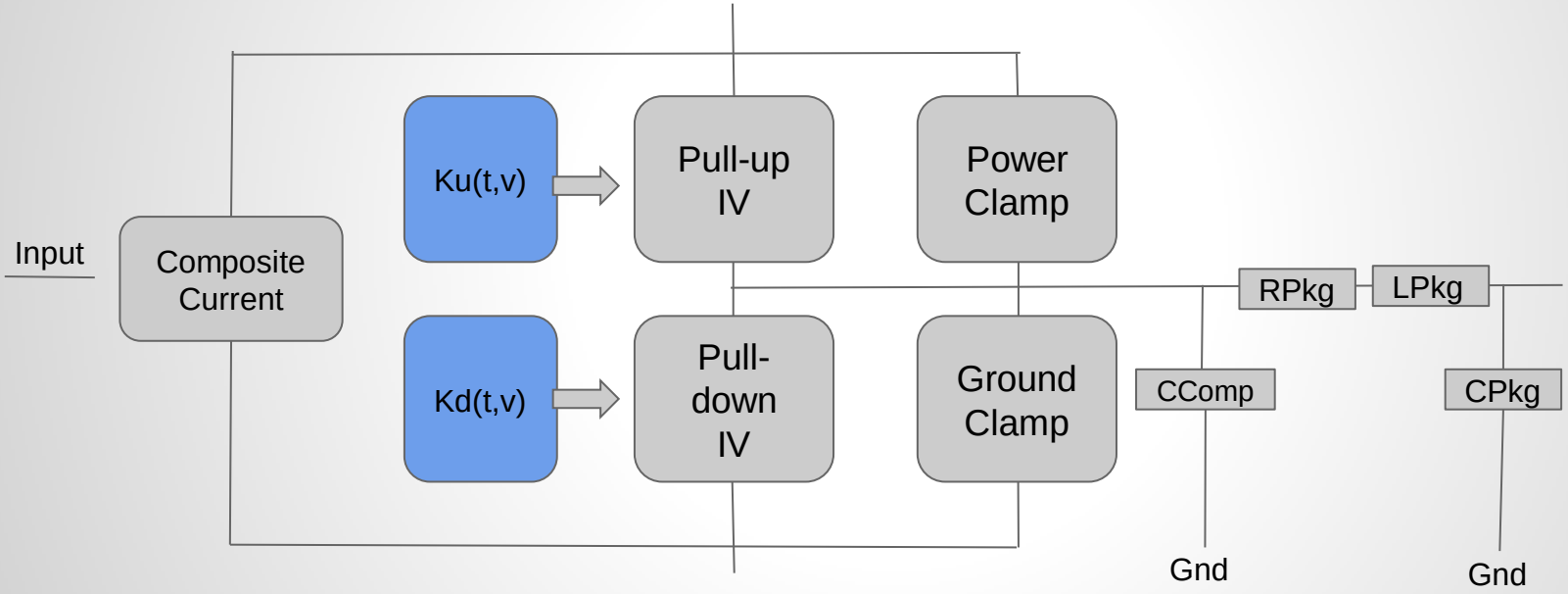
Observations:

Tune w/ RC constants
Speed is good
First order estimate only

Drawing current is way off

Waveform based: [Schematic]

“Stock” IBIS building block implemented explicitly in .subckt



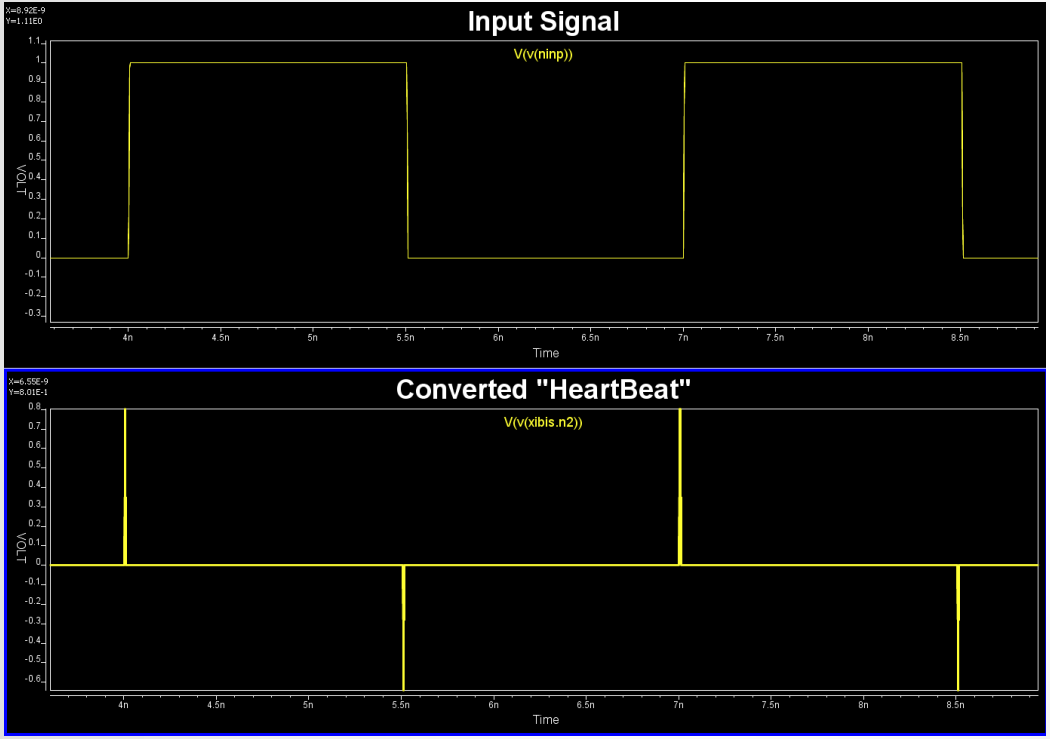
Waveform based: [Implementation]

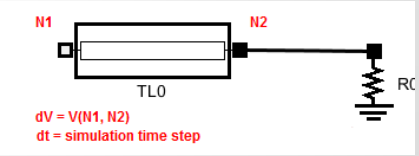
- Retrieve “t” of Ku(t)/Kd(t)/Icc(t) etc
  - Convert input signal to “heart beat” signals
  - Convert signal using “time” variable
  - Convert to “elapsed time” using delay element (T-Line)

- Pre-compute Ku(t, v) R/F, Kd(t, v) R/F
  - Published paper [Ref.4], or Ku/Kd from spice [Ref.5]
  - Assemble all blocks with ASRCs in the subckt

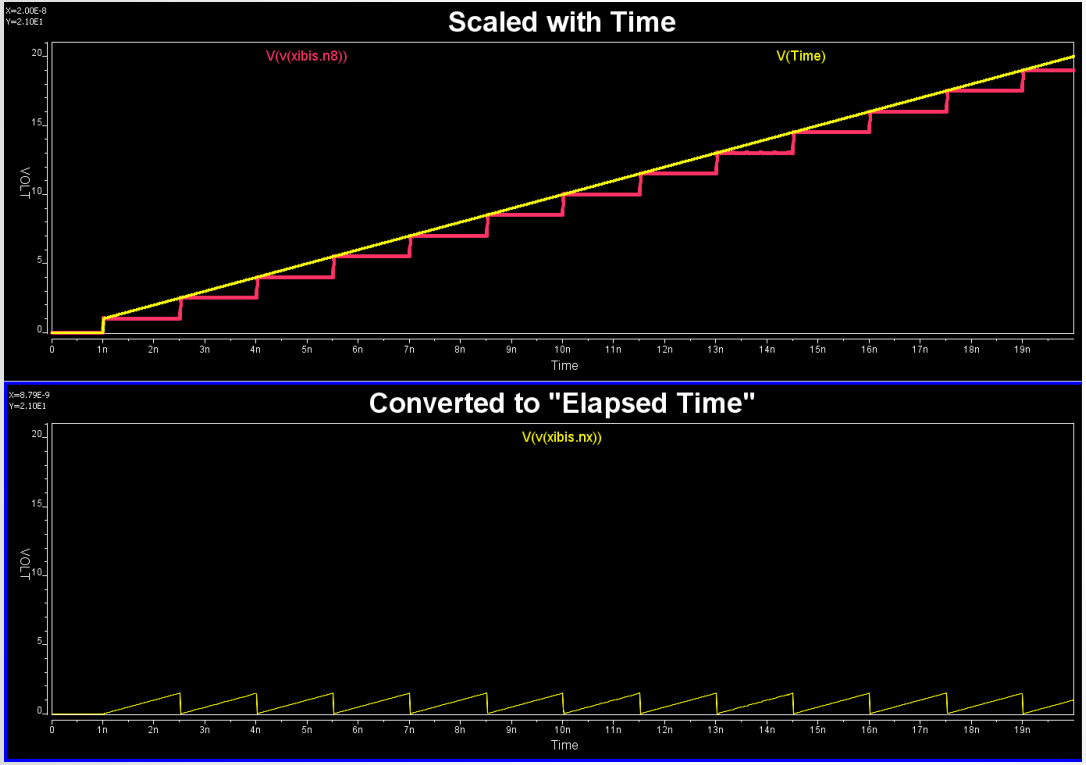
- Glitches removal with limiters

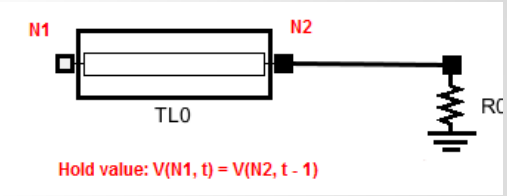
Waveform based: [Implementation]





Waveform based: [Implementation]





t - value hold

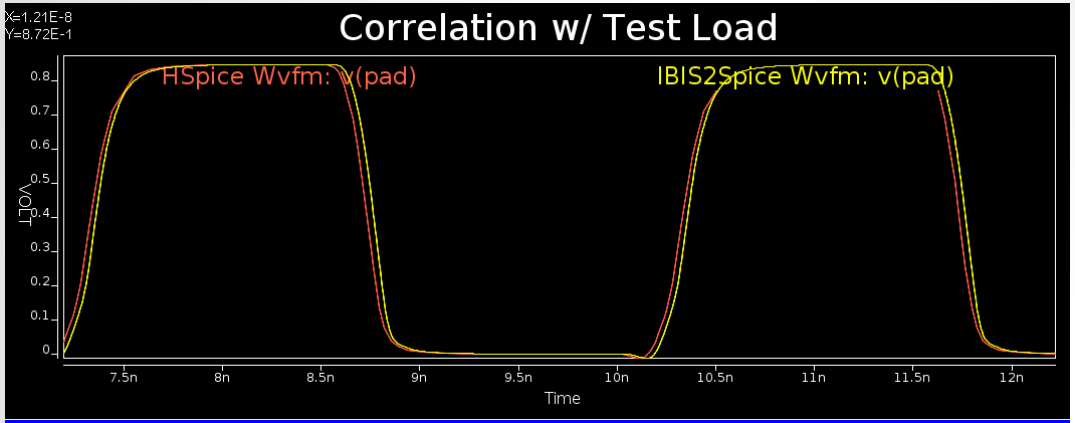
Waveform based: [Implementation]

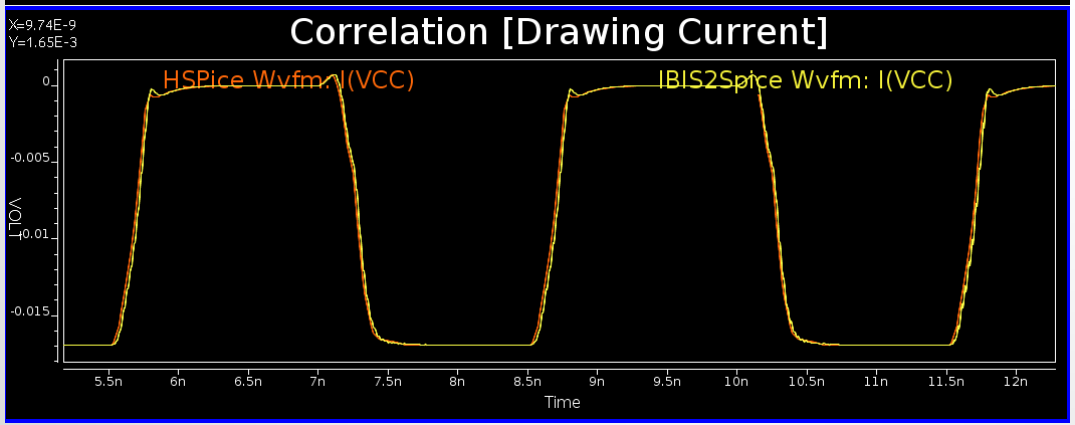
```
* KU COEF RISE
.SUBCKT DQ_34_1066_MIN_KU_R 3 4 1 2
B1 3 4 V =
+ (V(1,2) < 0.0000E0)? 0.0000E0:
+ (V(1,2) < 8.2500E-3)? -4.0355E-1 * V(1,2) + 0.0000E0:
+ (V(1,2) < 1.6500E-2)? -9.6844E-2 * V(1,2) - 2.5303E-3:
```

```
* PU/PD/PC/GC BRANCH
XASRC_PU NDIE NVCC NVCC NDIE NKUX DQ_34_1066_PULLUP_MIN
XASRC_PD NDIE NVSS NDIE NVSS NKDX DQ_34_1066_PULLDOWN_MIN
XASRC_PC NDIE NVCC NVCC NDIE      DQ_34_1066_POWER_CLAMP_MIN
XASRC_GC NDIE NVSS NDIE NVSS      DQ_34_1066_GND_CLAMP_MIN
```

```
* PU BRANCH
.SUBCKT DQ_34_1066_PULLUP_MIN 3 4 1 2 5
B1 3 4 I = V(5) * (
+ (V(1,2) < -1.5000E0)? 5.4653E-3:
+ (V(1,2) < -1.4700E0)? 1.4682E-2 * V(1,2) + 2.7488E-2:
+ (V(1,2) < -1.4650E0)? 1.5490E-2 * V(1,2) + 2.8676E-2:
```

Waveform based: [Correlation]





Observations:

Good correlation:

- V(t)
- I(t)

No need for tuning

- Simulation speed limited by delay element

Summary:

- Templates/Flows developed for:
  - Simulating IBIS model data with free spice
    - Systematic implementation can be done in modeling tool
    - Can also be done easily with some scripting for quick validation
  - Choices between speed vs accuracies:
    - Ramp based model simulates very fast
    - Waveform based correlates very good
      - Limiter is t-line based delay element
    - Can support Icct and composite current as well
      - Since we have “elapsed time” info already...

Future work:

- Add delay support in spice's "E" element
  - ease requirement of t-line based delay
  - will improve simulation performance significantly

- ASRC for multi-dimensional table
  - compensational circuit for true-differential model
  - pattern dependent Icct compensation
  - be part of [External Model] in IBIS

References:

1. http://ngspice.sourceforge.net/docs/ngspice-manual.pdf
2. https://groups.google.com/forum/#!topic/comp.arch.fpga/xP62ggOFQ0M
3. http://www.spisim.com/products/spilite-free-si-snp-ibis-tool/
4. Extraction of Transient Behavioral Model of Digital I/O Buffers from IBIS
   Peivand Tehrani et. al, 1996 Electronic Components and Technology Conference.
1. General K-table Extraction with Spice, Bob Ross, IBIS Summit, Designcon 2015

Q & A

SPISIM is an InSync member.