# General K-table Extraction Proposal Using SPICE

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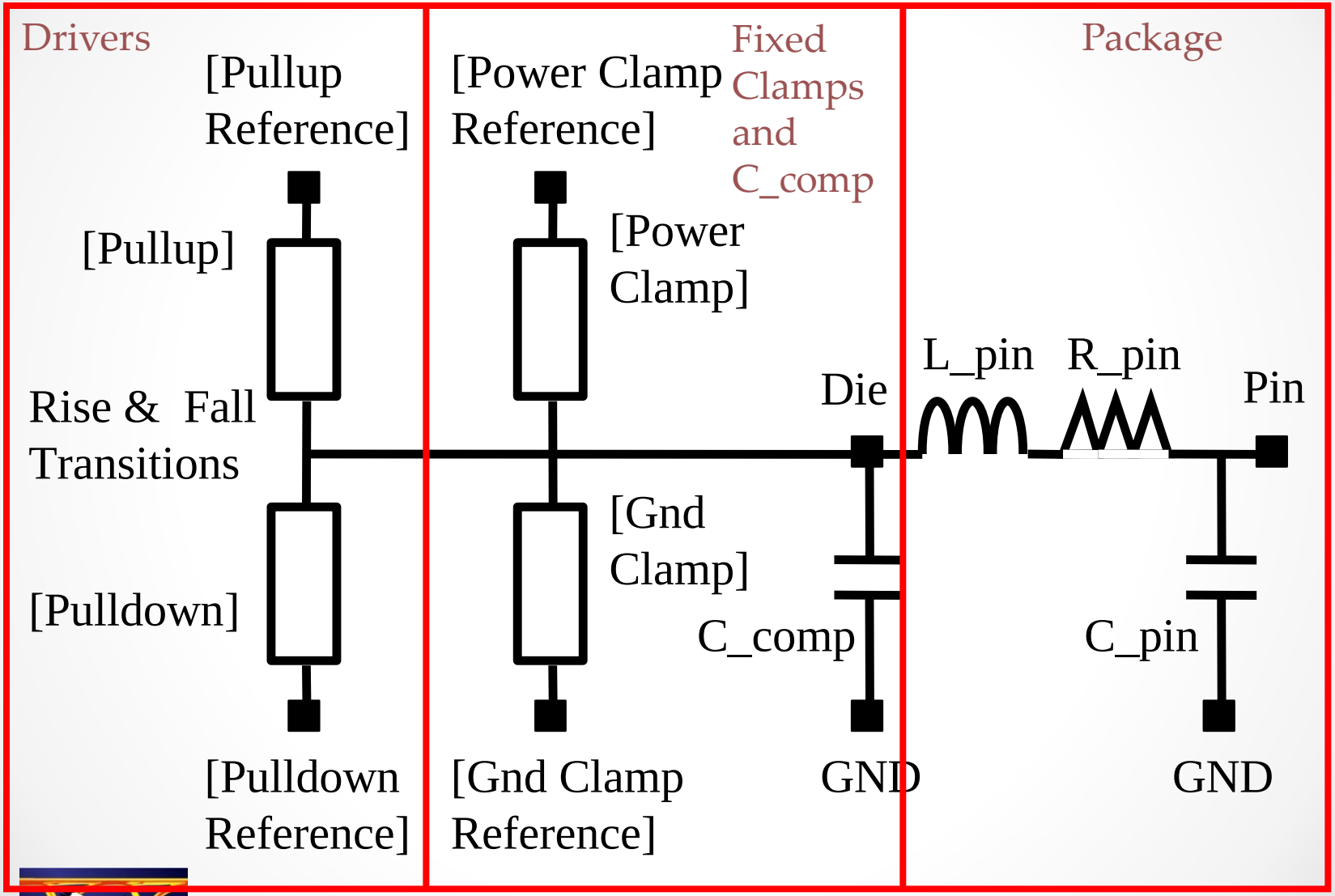
# Outline

- Overview
- Standard IBIS Model
- C_comp Variations
- Generalized K-table [Kpu(t), Kpd(t)] Extraction for Standard IBIS Model
- Proposed K-table Extraction Process with Extended C_comp model (and other blocks)
- Concluding Comments
- References from www.eda.org/ibis/summits/ on related material

# Overview

- Standard IBIS uses a fixed value of C_comp, as seen in the standard reference model
- A more detailed C_comp is needed for high-speed analysis as modelled by IBIS-ISS or by S-parameters
- Interconnect BIRD proposal defines general On-die and Package blocks
- Generalized method to extract and compensate for more detailed structures is proposed
- Limitations remain in a more detailed model

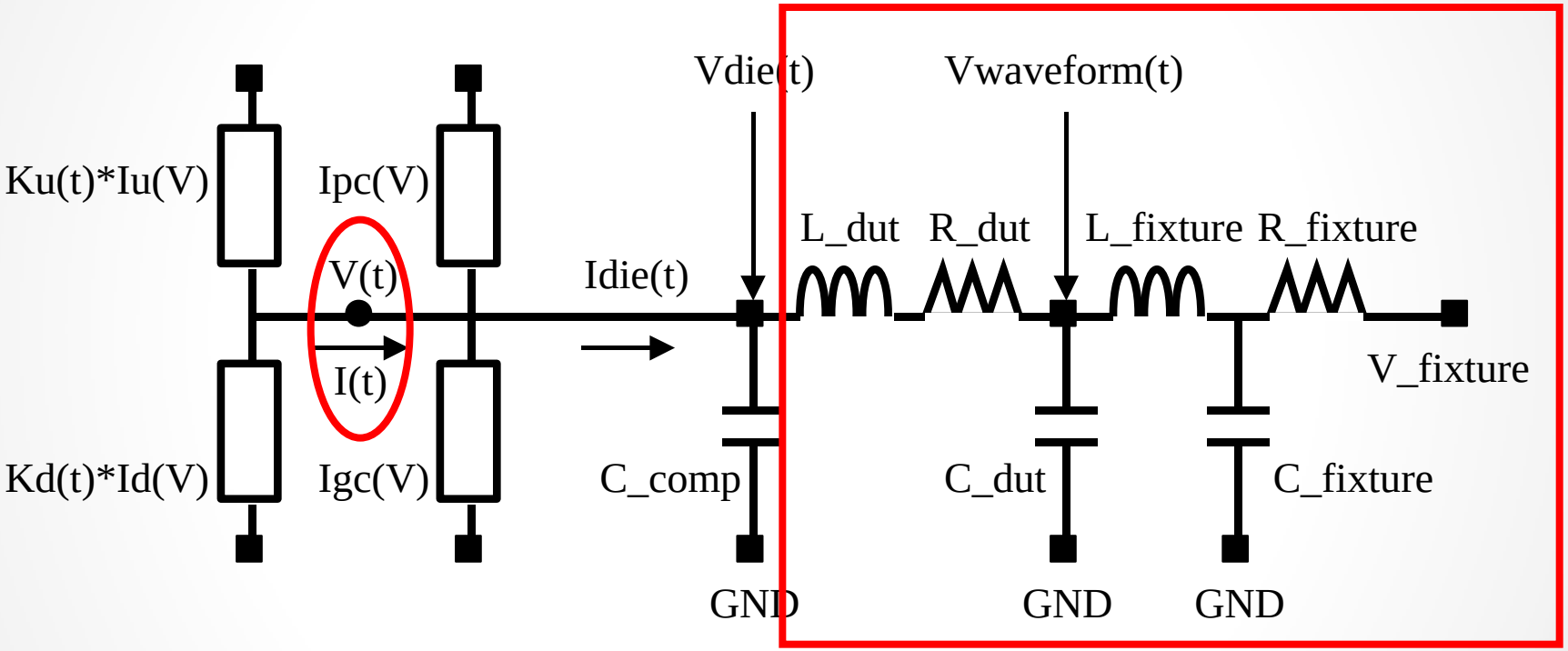
# Standard IBIS Model



# C_comp Variations

- Voltage (device physics)
- Temperature (device physics)
- Input versus I/O mode (suggest using Input model)
- Frequency (C_comp might be a simplified reactance model at a measured frequency for a more complex structure, e.g., C with several parallel R-C's)
- Power connections (between all power terminals)
- State dependent (low-to-high versus high-to-low)
- Range (corners different than [Model] corners)
- A more complex C_comp still has constant values

# Generalized V-T Extraction Load (with L/R/C_dut)




**V(t) and I(t) can be calculated from load information**

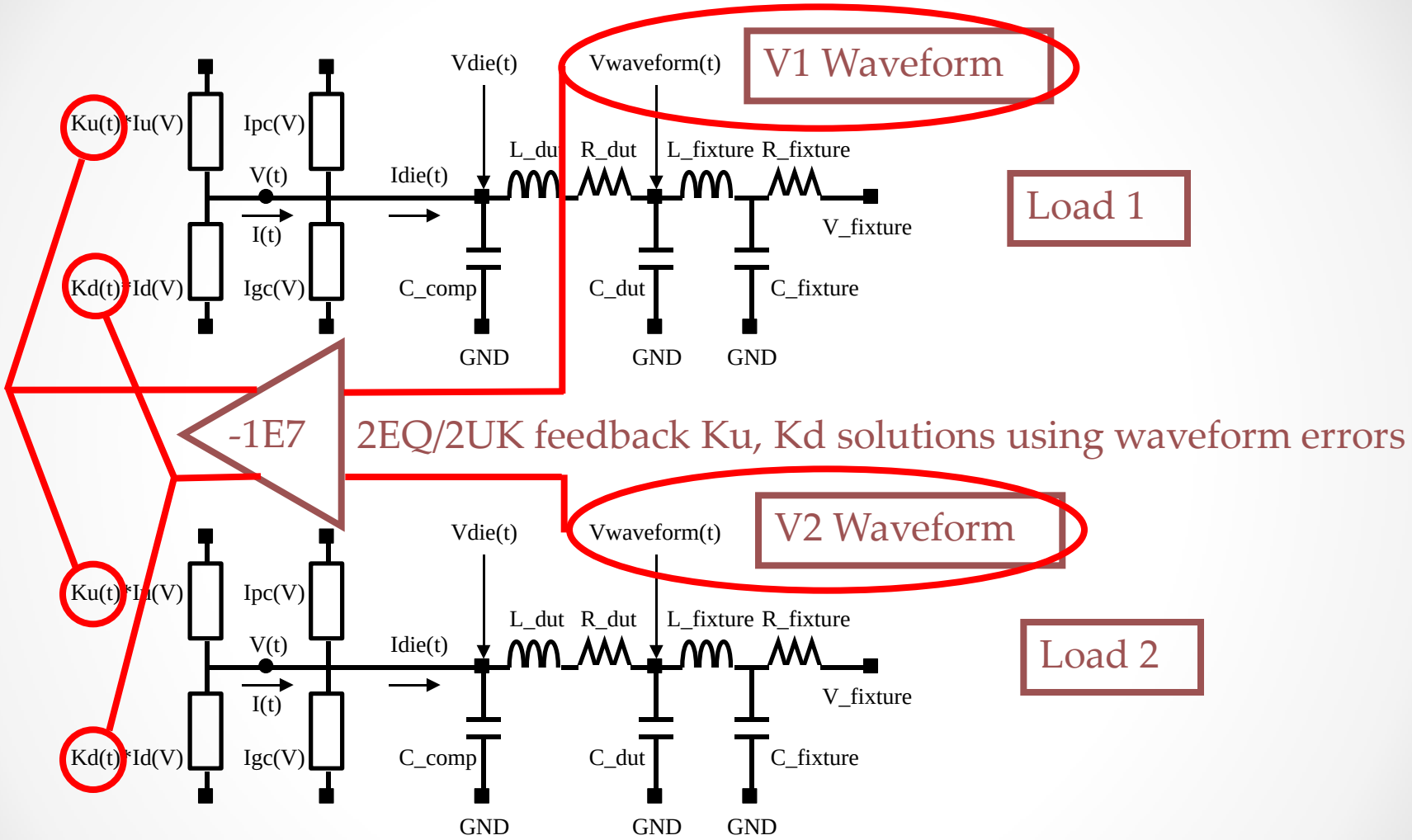
# Direct V(t), I(t) Solution

- Xuefeng Chen, Asian IBIS Summit (China), September 11, 2007: V(t), I(t) can be extracted directly for L/R/C/V_fixture from given information by applying i=L*dv(t)/dt and v=C*di(t)/dt
- This can be extended to include L/R/C_dut (where L/R/C_dut replaces the L/R/C_pin values at the measured pin)
- Then the Ku(t) and Kd(t) tables can be extracted using the 2-equations/2-unknowns (2EQ/2UK) method for rising waveform or falling waveform extractions

# Indirect Prototype Solution Next

- Originally used to investigate C_comp, L/R/C_dut and general L/R/C/V_fixture cases for K-table extraction
- Calculates simultaneously K-tables [Kur(t), Kdr(t) or Kuf(t), Kdf(t)] for rising waveforms or falling waveforms based on two *_fixture based loads with corresponding V-T waveforms
- Note, a 2EQ/2UK solution for the equations given later involve a determinate [I(VDET) in net-list] and SPICE based calculated K-table multiplier solutions [I(VKUR), and (I(VKDR)] as a function of both the PU and PD tables
- This can also be used for I(VKUF) and I(VKDF) multiplier table generation

# SPICE Prototype for Ku(t), Kd(t)



# Partial SPICE Circuit Showing 2EQ/2UK K-Table Extraction

```
*
* FEEDBACK TABLE ADJUSTMENT ............................. VVV
GDET    NDET  GND  CUR='(I(VDN2)*I(VUP1)-I(VDN1)*I(VUP2))/(1E7)'
VDET    NDET  GND  0
*
GKUR    NKU   GND
+ CUR='((V(IN2)-V(PIN2))*I(VDN1)-(V(IN1)-V(PIN1))*I(VDN2))/I(VDET)'
VKUR    NKU   GND  0
*
GKDR    NKD   GND
+ CUR='((V(IN1)-V(PIN1))*I(VUP2)-(V(IN2)-V(PIN2))*I(VUP1))/I(VDET)'
VKDR    NKD   GND  0
*
```

Kur

Kdr

$$I_1(t) = Ku(t)*Iu(V_1(t)) + Kd(t)*Id(V_1(t))$$

$$I_2(t) = Ku(t)*Iu(V_2(t)) + Kd(t)*Id(V_2(t))$$

# Comments

- The –1E7 negative feedback block is really a 2EQ/2UK block applied to the difference between the measured waveform and calculated waveform multiplied by a large value to provide negative "gradient" feedback
- This forces convergence to the correct Ku(t) and Kd(t) solution to match simultaneously both measured and calculated waveforms
- Method does not always converge – 2EQ/2UK block approximation is not an exact negative "gradient", and/or numerical issues arise
- Note, this process must be done in a vendor-specific SPICE that supports tables (versus IBIS-ISS)

# SPICE Numerical Comments

- I-V tables entered as G elements (VCCS)
- V-T tables entered as PWL voltage sources
- Voltage rails can be entered
- SPICE does interpolation
  - Higher resolution time steps for extraction than in V-T tables
  - G table currents are found by interpolation
- I-V and V-T tables are also automatically extrapolated from final value
- SPICE allows setting convergence criteria for more detailed interpolation curve fitting (e.g. spline)
- K-tables printed out for Kur(t), Kdr(t) and separately for Kuf(t), Kdf(t)

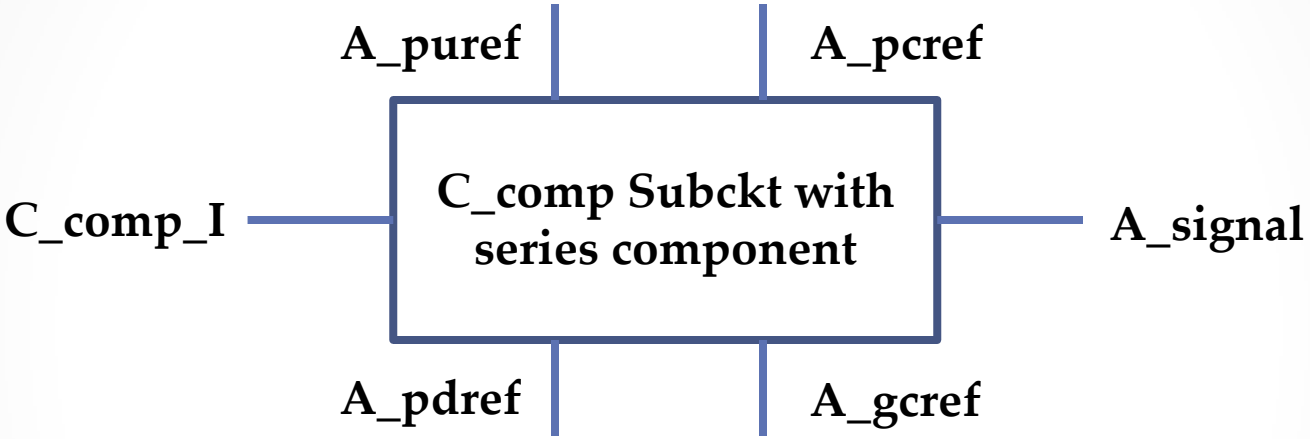
# Part of SPICE Encoded IBIS Prototype for Simulation

```
* HIGH SIDE
XUP     OUT1   VCC   NU1           PULLUP
VUP     NU1    VCC   0
GUP     OUT1   VCC   CUR='-I(VUP)*(I(VKUR)*I(VON)+I(VKUF)*(1-I(VON)))'
XPC     OUT1   VCC                 POWER_CLAMP
*
* LOW SIDE
XDN     OUT1   GRD   ND1           PULLDOWN
VDN     ND1    GRD   0
GDN     OUT1   GRD   CUR='-I(VDN)*(I(VKDR)*I(VON)+I(VKDF)*(1-I(VON)))'
XGC     OUT1   GNDC                GND_CLAMP
*
* C_COMP AND DUT PACKAGE
XCAP    OUT1   GRD                 C_COMP
XPKG    OUT1   GRD   PIN1          PACKAGE
*
* LOAD
TLOAD   PIN1   GRD   PIN9    GRD   Z0=50 TD=1N
RLOAD   PIN9   GND   50G
*
* VOLTAGE CONTROL (AMPLITUDE (0 TO 1), PULSE WIDTH & PERIOD)
VPULSE STEP   GRD   0   PULSE (1 0 0P 1P 1P 5N 10N)
```

Kur, Kdr

Kuf, Kdf

# General Single-ended C_comp Subckt Model

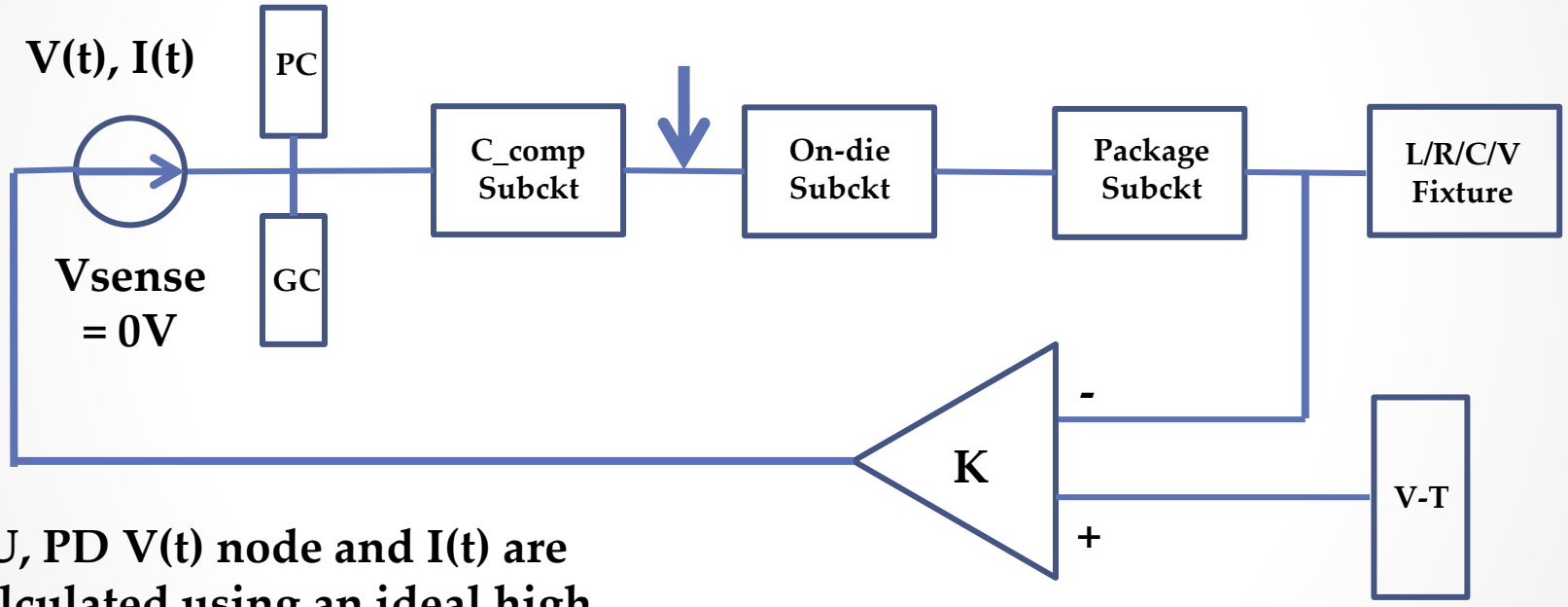



- Notation and details under development
- C_comp_I (if needed) attaches to internal buffer
- A_signal is C_comp Subckt output
- A_signal to C_comp_I resistance needs to be de-embedded from I-V tables
- Model can be extended for differential connections

# Revised, Generalized Extraction Steps Based on SPICE

- Get source data: For L/R/C/V_fixture combinations, find V(T), I-V tables and encode in SPICE using VCCS and V(t) PWL elements
- Create SPICE blocks: C_comp, On-die, Package blocks (if used) that will be assumed in the model
- Extract K-tables: Kur(t), Kdr(t) and Kuf(t), Kdf(t), and use for internal model
- Generate New V-T tables at C_comp A_signal node
  - Use simple R/V_fixture loads
  - V-T tables using R/V_fixture at C_comp A_signal node and I-V tables become new compensated IBIS model to generate correct K-tables

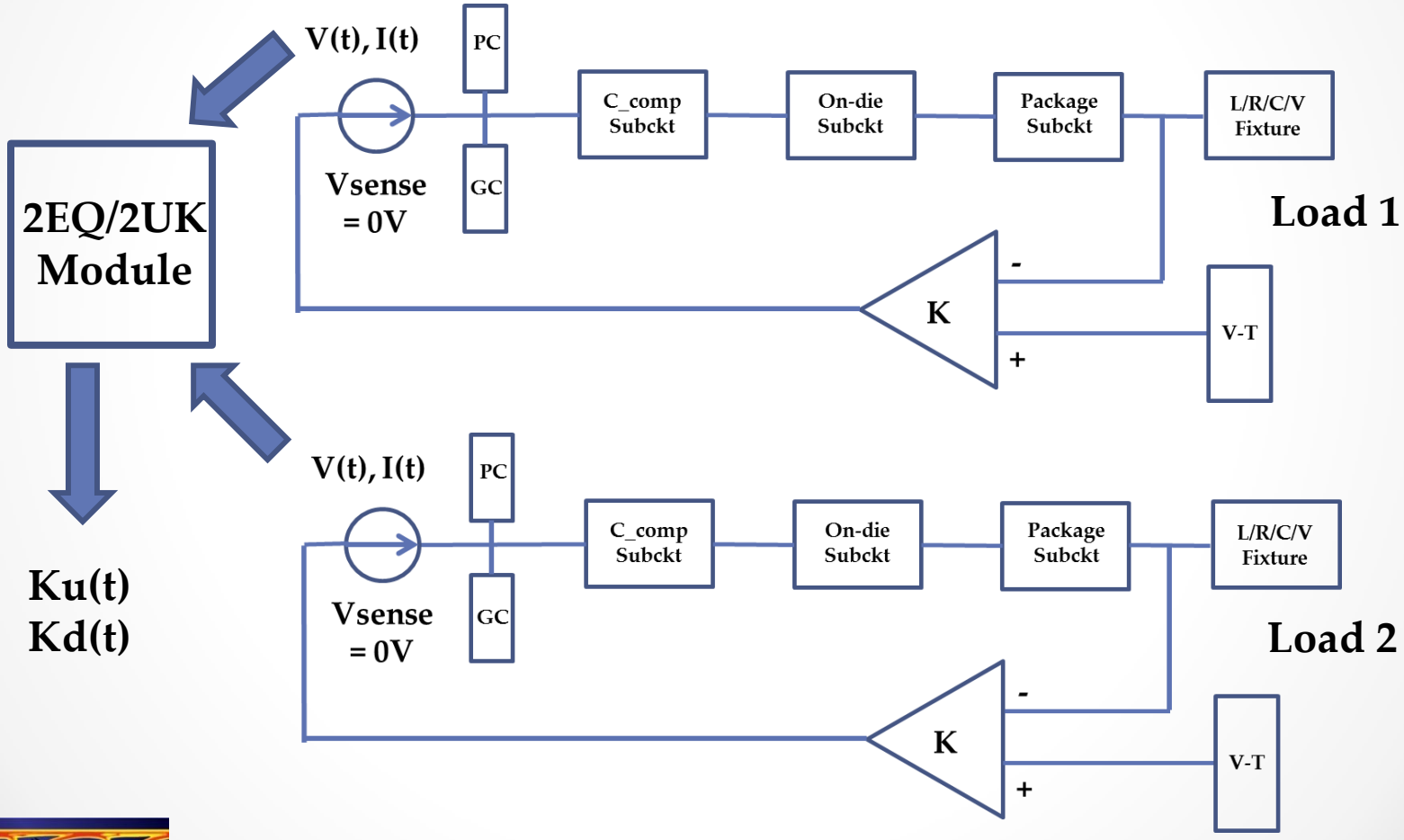
# SPICE Extraction of V(t), I(t) Setup and C_comp A_signal Node



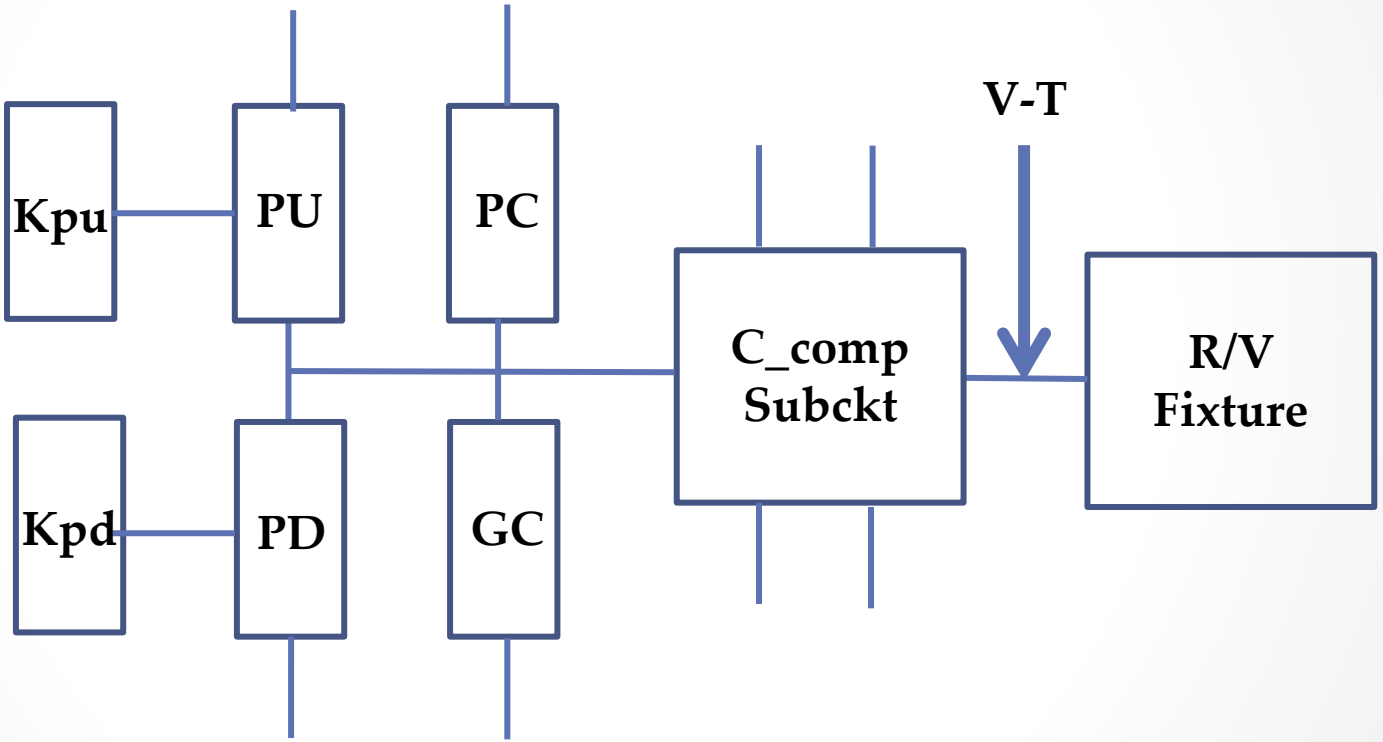

**PU, PD V(t) node and I(t) are calculated using an ideal high gain (e.g., K=1e7) operational amplifier**

**V-T table (originally extracted at the Fixture) is now a PWL driver**

# 2EQ/2UK SPICE Setup to Generate Ku(t), Kd(t) Tables



# Generate New V-T Waveforms at C_comp A_signal Node (if needed)



# EDA Tool Options

- Use the originally extracted [Kur(t), Kdr(t)] and [Kuf(t), Kdf(t)] tables as drivers and along with the original PU, PD, GC, PC, and C_comp subckt
- Or use PU, PD, GC, PC, C_comp subckt and NEW V-T tables for simple R/V_fixture values (if changed) and let EDA tool derive NEW K-tables that include C_comp subckt, but without Package or On-die blocks (for example, the previous slide)
  - EDA tool responsible for de-embedding C_comp subckt
  - Model providers would issue this simplified model

# Conclusions

- SPICE feedback based extraction method proposed
  - Does not depend on internal circuit details
  - Also supports On-Die and Package blocks
  - Could be implemented by mathematical code in tools
- EDA tools must add de-embedding of general C_comp subckt for V-T data given at the A_signal node
- Note, any "series" resistance needs to be de-embedded from the I-V tables

- Some IBIS Summit references related to this presentation are given next regarding 2EQ/2UK algorithms, C_comp modeling, de-embedding, and other approaches

# K-table Algorithm and 2EQ/2UK Extraction

- Chen, Xuefeng
  - IBIS Algorithm Including Reactive Loads (September 11, 2007) - Shows how 2EQ/2UK algorithm is solved with reactive fixture loads
  - Study of Solving IBIS Single VT (November 11, 2008) - Single VT case solutions evaluated
- Muranyi, Arpad
  - A VHDL-AMS Buffer Model Using IBIS V3.2 Data (June 5, 23, 2003) - A VHDL-AMS implementation and testing of 2EQ/2UK method
- Ross, Bob
  - Introduction & Model Processing Algorithms (October 15, 1998) - Introduction of 1-waveform, 2-waveform extraction
  - Improving IBIS ECL Algorithms (December 6, 2005) - The 2EQ/2UK algorithm is adjusted using CCVS tables
  - IBIS Algorithms Revisited (June 5, 23, 2003) - K-tables described and 2EQ/2UK method extraction method proposed
  - IBIS Die V-T Tables from Part or Board Measurements (February 2, 2004) - Approximate de-embedding of package and board model
- Schutt-Aine, Jose, etal.
  - IBIS Modeling Using Latency Insertion Method (LIM) (May 16, 2012) – LIM method for simulation and K-T table extraction improvement

# C_comp Models and Extraction

- Mirmak, Michael
  - Issues with C_comp and Differential Multi-stage IBIS Models (April 5, 2004) – Driver Schedule double counting and complex C_comp
  - Multi-Element C_comp Modeling (October 4, 2004) – Extended C_comp model and differential C_comp
  - IBIS in the Frequency Domain (July 25, 2006) – Review and discussion of extended C_comp and frequency domain impedance models
- Muranyi, Arpad
  - High Accuracy Behavioral Modeling for Frequency and Time Domain Simulations (June 21, 2001) – Pole-zero extraction of complex impedance
- Giacotto, Luca
  - Buffer Impedance Modeling (March 8, 2002) - Pole-zero and extended C_comp extraction
  - Buffer Impedance and Quality Issues (June 13, 2002) – Pole-zero extraction as a function of bias proposal

# Miscellaneous De-embedding

- Ross, Bob
  - IBIS Die V-T Tables from Part or Board Measurements (February 2, 2004) – Approximate de-embedding of package and board model
  - C_comp and Buffer Scaling Observations (February 9, 2006) – C_fixture compensation for Driver Schedule C_comp rules
  - Capacitance Compensation (February 5, 2009) – De-embedding method for C_comp and C_fixture method for Driver Schedule

# Sampling of Other Approaches

- Zhu, Ting, etc.
  - Surrogate Model-based High-speed IO Macromodel (June 5, 2012) – Continuous equation-based PVT extraction
- Comberiate, Tom, etc.
  - Using X-Parameters to Generate IBIS Models (May 15, 2013) – IBIS Model generation from X-parameters
- Stievano, Igor, etc.
  - Thevinin's Theorem Revisited (May 15, 2015) – Thevenin voltage based structure and extraction
  - IC Macromodels from On-the-fly Transient Responses (May 10, 2006) – Non-linear macromodeling via parametric identification of logic gates [M(pi)log]
- Dghais, Wael, etc.
  - Table-Based Extraction for Modeling Driver's Output Admittance (May 15, 2013) – Least squares I-Q model extraction and voltage dependent capacitance effects state