Memory Packaging Technology & Modeling

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Outline

- Packaging Tradeoffs
- DRAM packaging
- NAND/MCP/NOR packaging
- Package Modeling

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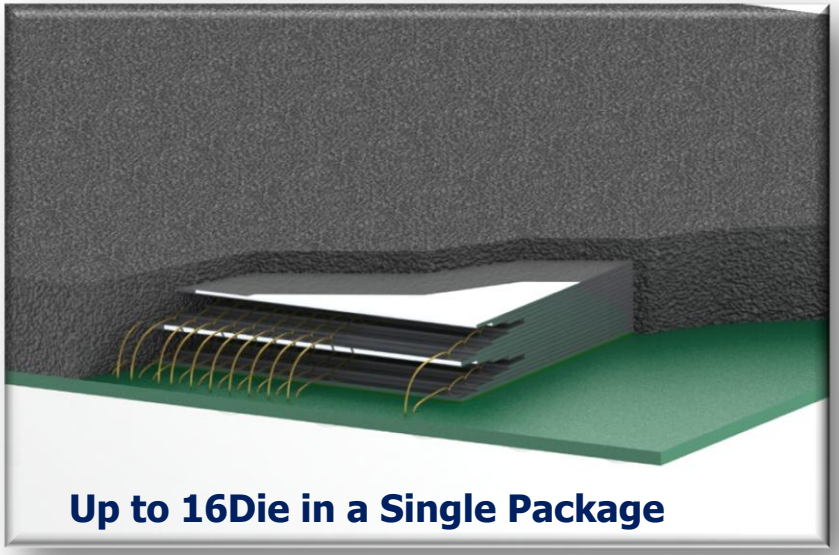
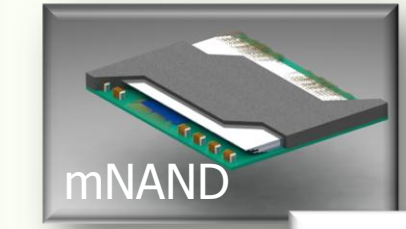
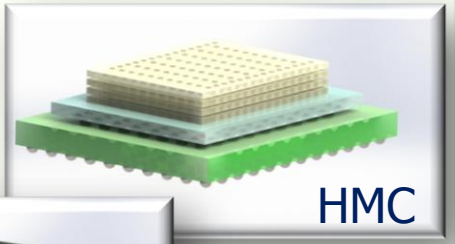
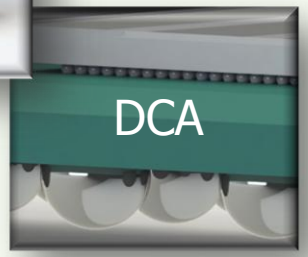
Memory Packaging Tradeoffs



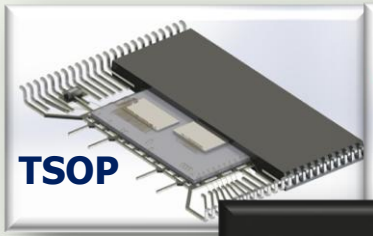


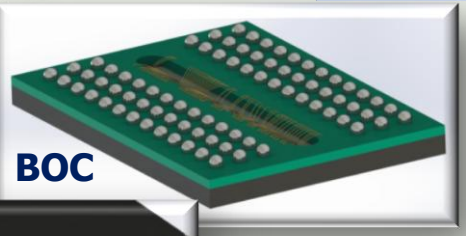




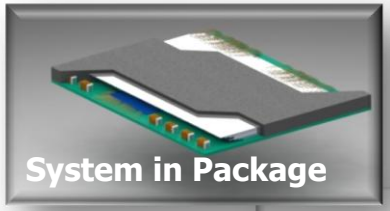
Density | **Performance**

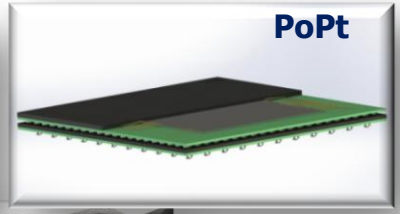
Cost | **Custom**

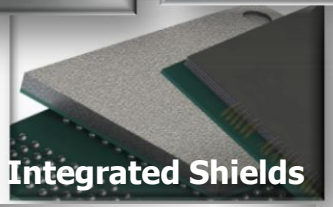




CiP → SiP







2D → 3D

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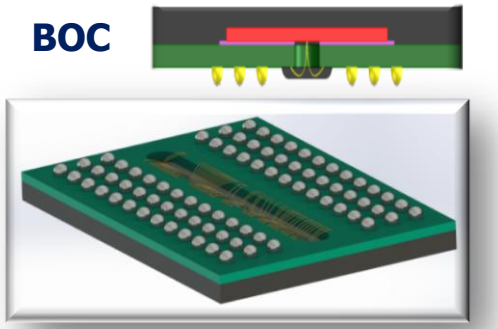
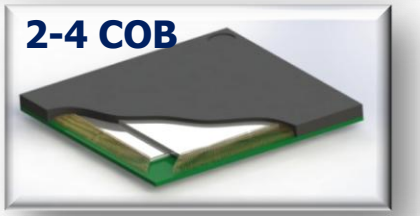
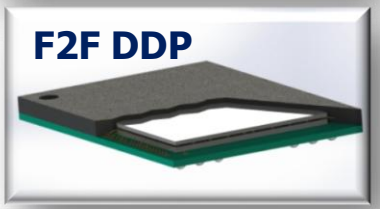
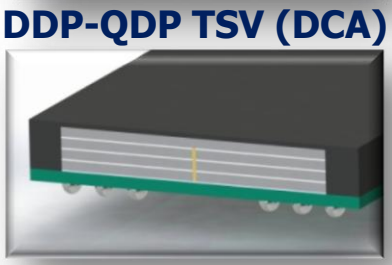
DRAM Packaging Terminology

- Number of identical die in package:
  - 1=SDP, 2=DDP, 3=3DP, 4=QDP
- FBGA BOC – Board On Chip
  - For SDPs
- FBGA COB – Chip on Board
  - For DDP+
- Stacking Technologies:
  - RDL – Re-Distribution Layer, routes edge to center of die
  - 2-4 COB – Bondwire (BW) to each die edge, RDL to center
  - F2F DDP – 1 BW, 1 RDL, 2 die connected (Face-to-Face)
  - DCA – Direct Chip Attach – no BWs
  - TSV – Through Silicon Via – in Hybrid Memory Cube (HMC)









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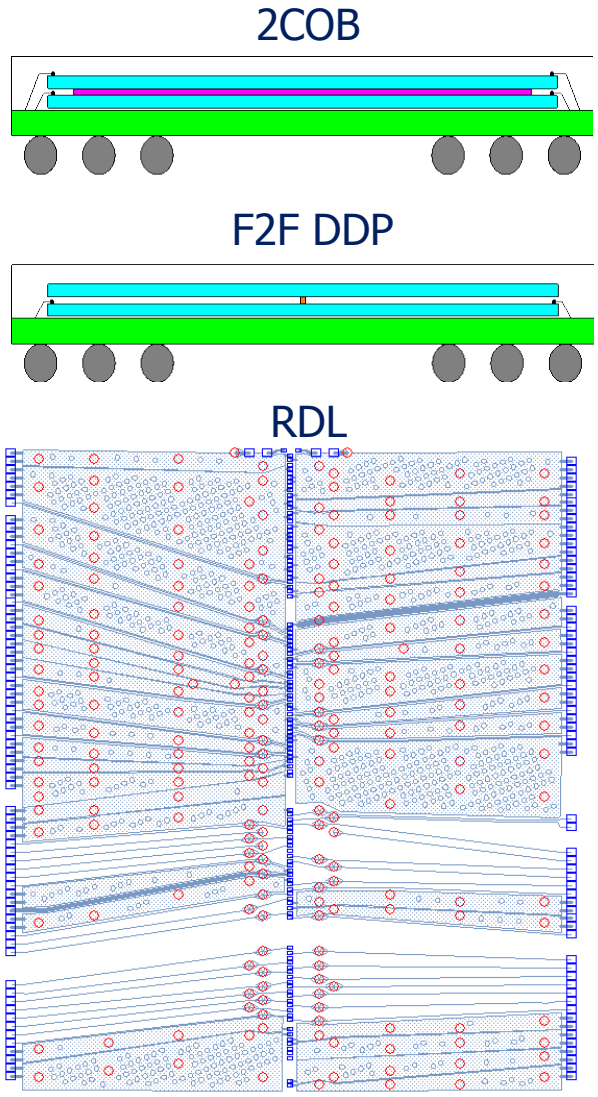
RDL in Stacked DRAM

- RDL metal is added on top of a finished die (1 or 2 layers)
  - Added Resistance
  - Lossy T-line like characteristics
- 2COB – lower speeds
  - RDL routes from edge to center
  - Long RDL for each die (long stubs)
- F2F DDP – faster speeds
  - Long RDL on bottom die
  - Short RDL on flipped top die (short stubs)



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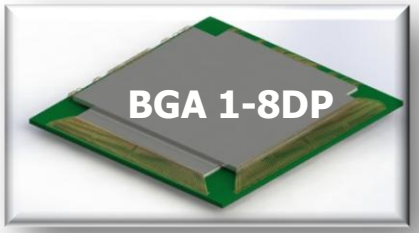
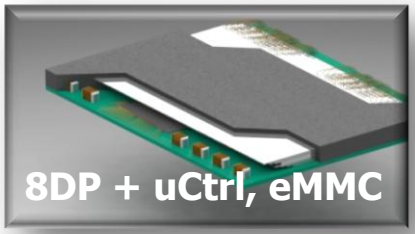
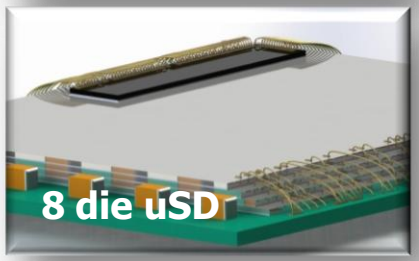
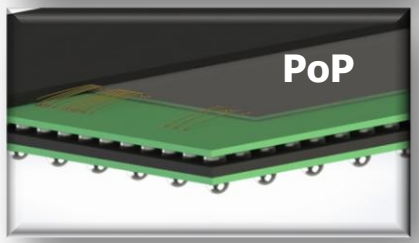
NAND/MCP/NOR Packaging Terminology

- Number of die in package:
  - 8=8DP, 16=16DP
- MCP – Multi Chip Package (combos of LPDRAM, NAND, NOR)
- eMMC – Embedded NAND with MultiMediaCard controller
- uSD – Micro SD card format
- PoP – Package on Package
- PoPt – PoP, top package of PoP stack
- WLCSP – Wafer Level Chip Scale Package
- uCuS – Microcontroller under stack

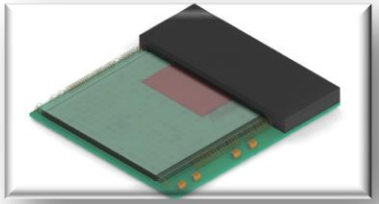


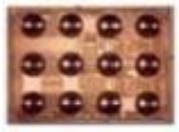






8 Die uCuS





WLCSP

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Package Modeling - Current

- SDP modeling formats
  - [Pin] RLC, [Package Model] – coupled matrices
  - Full package, coupled SPICE for DDR4
  - S-param , .s4p, .s12p, .sxxp for HMC SerDes packages
- Stacked package modeling formats
  - EBD – lossless, uncoupled, but models forks/splits
  - SPICE – lossy, uncoupled/coupled

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Package Modeling - Future

- SDP modeling formats
  - Increased use of SPICE (IBIS-ISS) for packages
  - Inclusion of on-die PDN models – SPICE (IBIS-ISS) format
  - Increased use of S-param format for SerDes, high speed packages
  - Mixed formats, IBIS-ISS + S-param + [Pin]
  - Pre-layout models: full byte lane (coupled) and single data bit (uncoupled) S-params
- Stacked package modeling formats
  - EMD – coupled/uncoupled models in IBIS-ISS format
    - Identical or mixed die types

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