Rantings of an IBIS Minimalist

Ken Willis
Product Engineering Director – High Speed Analysis Products
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Agenda

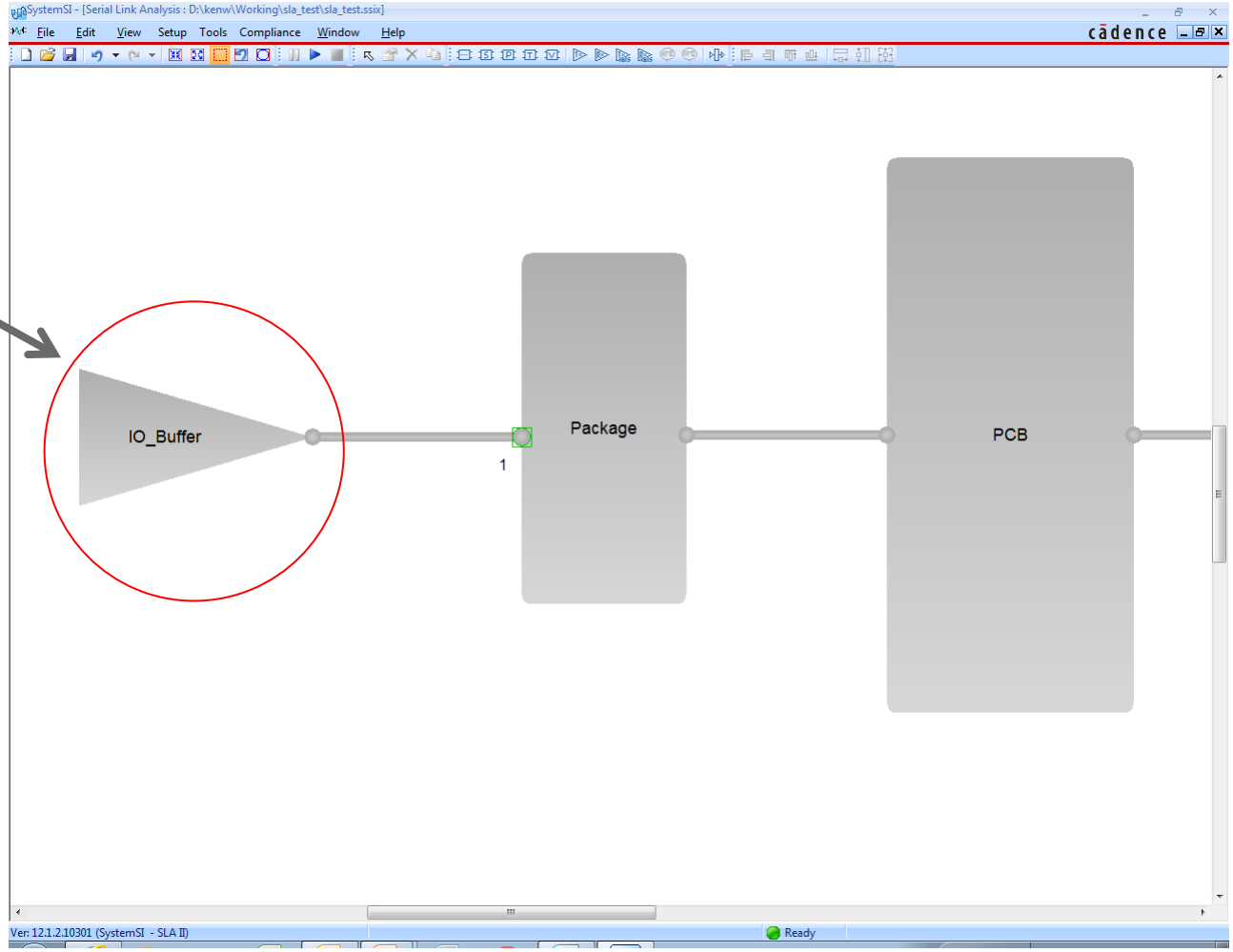
- In the beginning …
- Then what happened?
- What did we learn in 20 years?
- How should we handle interconnect?
- What is still missing?

In the Beginning …

- Donald Telian (Intel) visited Cadence in 1993, to drum up support for a new standard called “IBIS”
- It meant “I/O Buffer Information Sheet”
- The focus was on:
  - Replacing proprietary transistor-level IO models with industry standard IO models
  - Providing a huge simulation speed-up, enabling much more system simulation to be performed
- Lumped package parasitics were OK
- Power was considered ideal

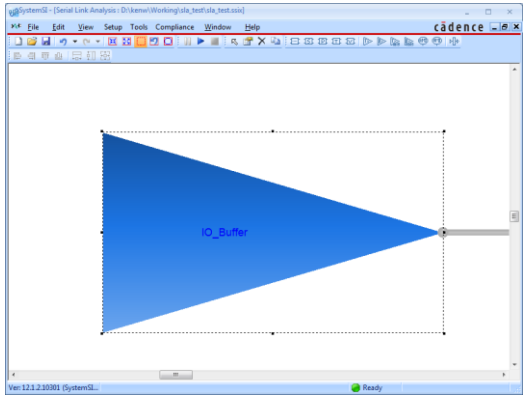
Original IBIS Focus

- Model the IO buffer!
- EDA tools could splice together multiple Spice interconnect models to complete the topology

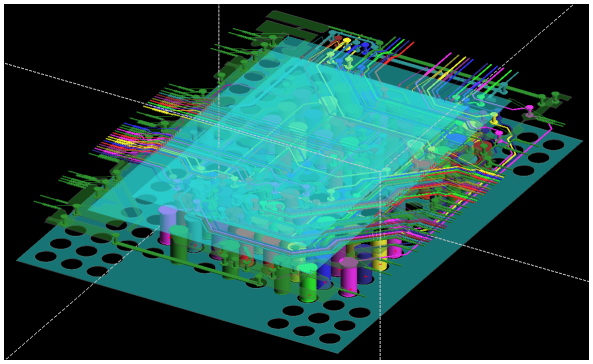


Original Line of Demarcation for IBIS's Focus

- IO Buffer



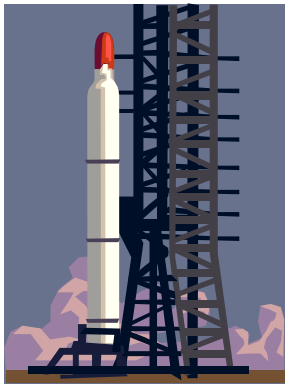
- Interconnect



IBIS spec domain

EDA tool domain

Then what happened?



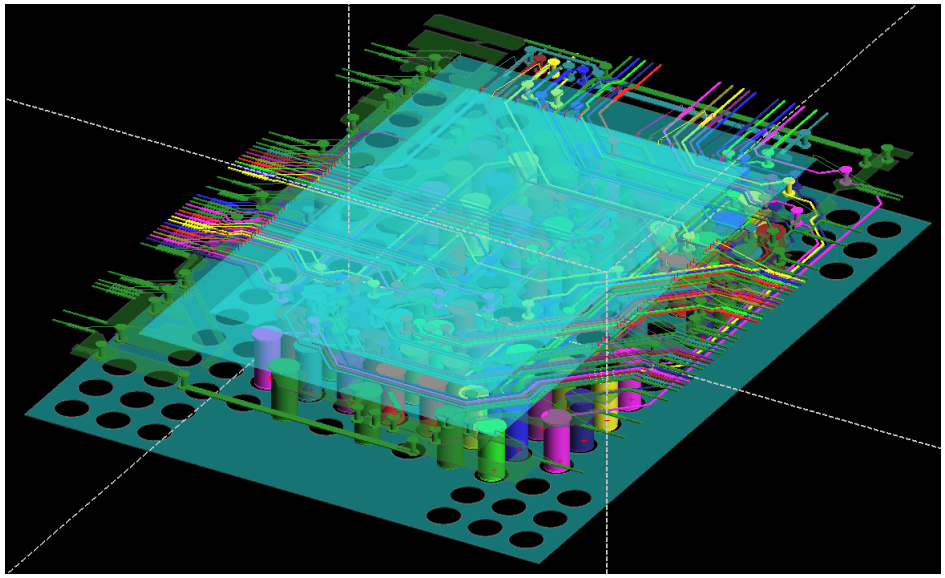
- Data rates went up … and up … and up
- IO buffer keywords were added to handle the new complexities
- We decided to model entire PCB signal paths (not power) with “EBD”
- Lumped package parasitics became distributed “Package Models” with IBIS-specified formats
- It turned out that some IO buffers didn’t fit the IBIS cookie cutter template so well, and [External Model] was born, so you could use Spice subcircuits
  - Key lesson here is “keyword explosion” vs. “general syntax”
- Packages became more and more custom, and were sometimes better represented with Spice subcircuits as [External Circuit]s
- Non-ideal power effects made it necessary to include on-die parasitics for some applications, leading to more [External Circuit]s
- Algorithmic modeling was invented to handle adaptive equalization
- Defined “ISS” so we could just use Spice to model anything custom

What did we learn in 20 years?

- Totally achieved the original focus:
  - Replaced proprietary transistor-level IO models with industry-standard IBIS
  - Got a huge simulation speed-up, simulation coverage skyrocketed
- You can standardize a small subcircuit if you can hard-code its top-level terminals
  - Ex. in out power ground for an IO buffer
- Sometimes you just have to invent something new (but it is rare)
  - Ex. algorithmic modeling for adaptive SerDes EQ
- Standardizing interconnect modeling is pretty difficult:
  - Arbitrary number of terminals
  - Hard to hard-code that
- As complexity goes up, keyword-driven specification breaks down, and we flank back to general Spice syntax

How should we handle interconnect?

- You need an interconnect model to simulate a whole driver-receiver path
- Interconnect can come from 2 main places:
  - Your physical layout (if you have it), using EDA extraction tools
  - From a supplier (internal or external)
- Do we need to invent a new format for interconnect modeling?



The Rant Page

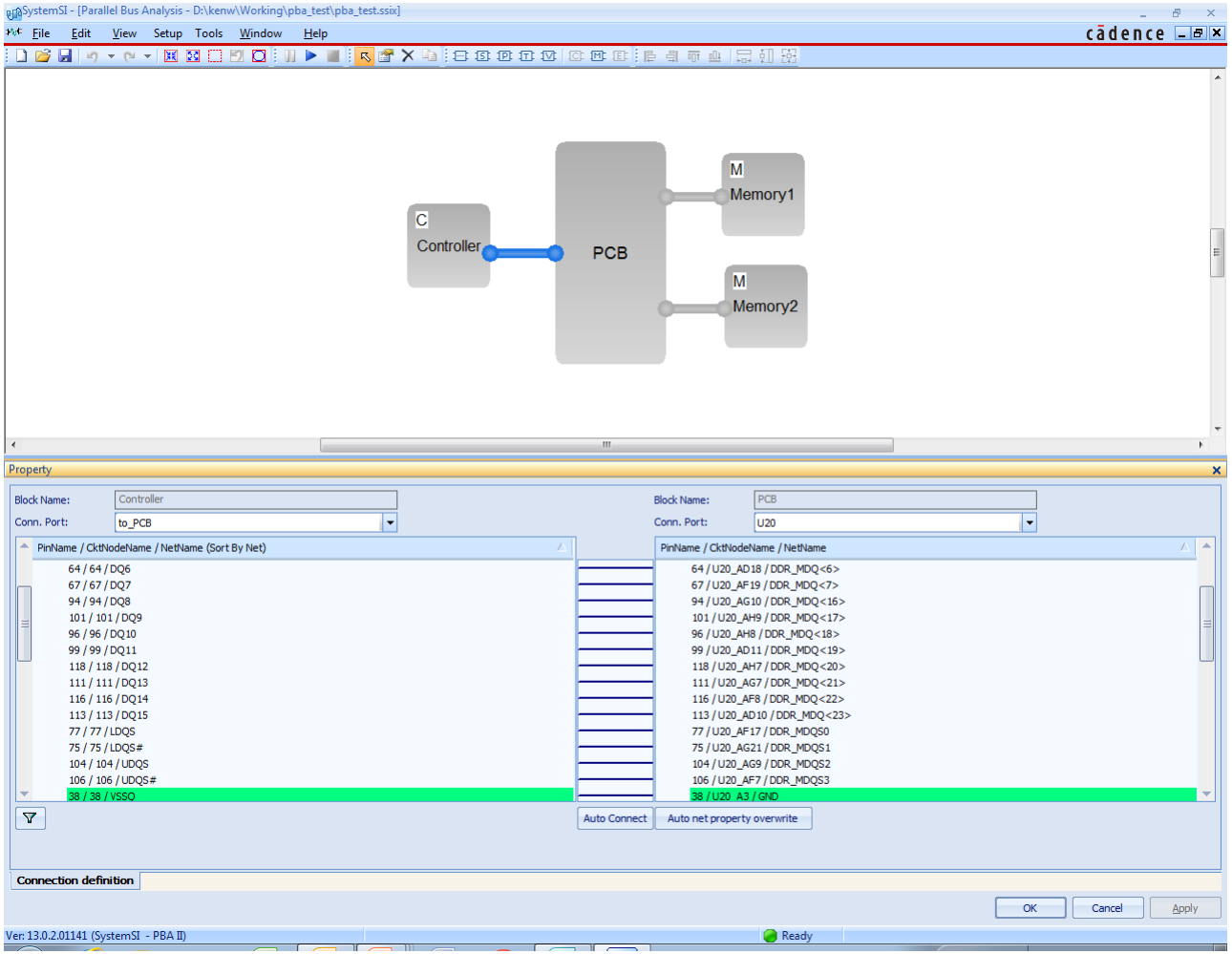
[Begin Rant]

- NO!!!!!!! This is a solved problem!
- Interconnect model format is NOT some new thing we need to invent!
  - We have modeled complex custom PCB interconnect in EDA tools for decades!
  - Why are packages/interposers/RDL any different?
  - You can model any interconnect in Spice!
  - Now it is even standardized as “ISS”!

[End Rant]

What is Still Missing in IBIS?

- A standard, convenient way to define connectivity between big interconnect Spice subcircuits



One Approach is MCP – Model Connection Protocol

- “Connection” refers to a group of subcircuit terminals
- Classifies terminals by signal, power, or ground
- Allows simple description
  - Pin name
  - Subcircuit terminal name
  - Signal name
- Makes it easy to hook one subcircuit to another

```
* [MCP Begin]
* [Connection] BGA
* [Connection Type]
* [Power Nets]
* [Ground Nets]
* Lumped(38) U20_A3 GND
* [Signal Nets]
* 101 U20_AH9 DDR_MDQ<17>
* 104 U20_AG9 DDR_MDQS2
```

If IBIS doesn’t want to use MCP (welcome to it), let’s define something better

Summary

- Let the “I/O Buffer Information Sheet” be for I/O Buffers!
- Don’t dilute its focus by trying to make it a standard for modeling arbitrary interconnect as well
- Today’s systems have complex interconnect, which can be modeled with Spice subcircuits
  - same with yesterday’s systems b.t.w.
- It is a complete waste of time inventing any new interconnect modeling format inside IBIS!
- All that is missing is a standard way to define connectivity between Spice interconnect subcircuits
  - This is essentially a mapping table
  - We have certainly solved bigger challenges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