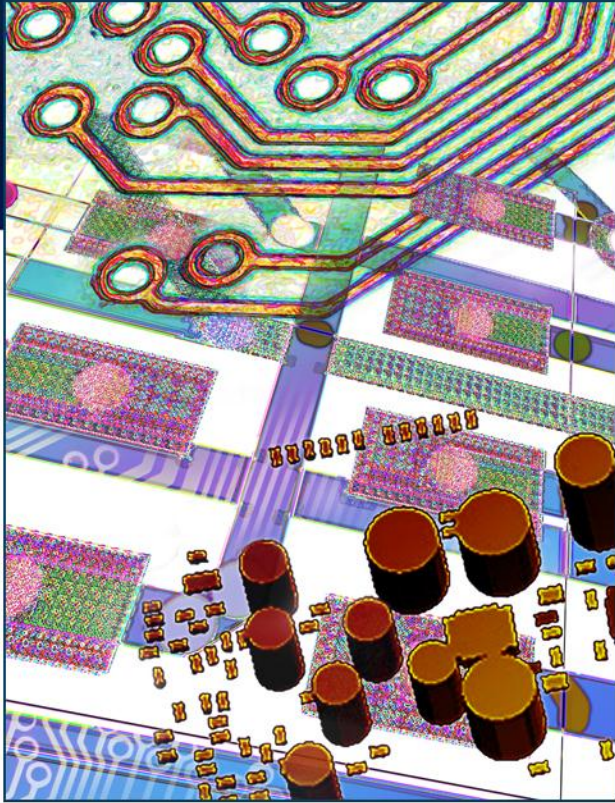# IBIS Package Modeling Proposal with [External Circuit]

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Introduction

- ■ The existing package modeling features in the IBIS specification are way outdated and desperately need improvements

- ■ Several proposals have been submitted in recent years and are currently being evaluated/discussed in the ATM Task Group

  - • BIRD 125.1   Make IBIS-ISS Available for Package Modeling
  - • BIRD 145.3   Cascading IBIS I/O buffers with [External Circuit]s
  - • BIRD 163   Instantiating and Connecting [External Circuit] Package Models with [Circuit Call]
  - • BIRD 164   Allowing Package Models to be defined in [External Circuit]
  - • BIRD 165   Parameter Passing Improvements for [External Circuit]s
  - • BIRD ???   SiSoft's EBD/EMD proposal
  - • BIRD ???   SiSoft's package modeling proposal

- ■ This presentation will focus on BIRDs 163-164 to familiarize the audience with one of the latest (and greatest ☺) proposals

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The basic idea

- The main idea is to make use of the [External Circuit] keyword for package modeling

- [External Circuit] was available for on-die interconnect modeling since its introduction in IBIS v4.1 (January 2004)

- There is practically no difference between an on-die interconnect and a package model, so why not use [External Circuit] for both?

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Why is [External Circuit] not popular?

- [External Circuit] existed in the IBIS specification for ten years, yet it hasn't been widely used so far

Why?

- Currently, [External Circuit] cannot be cascaded with [Model]
  - if someone wanted to model an on-die interconnect with [External Circuit] today, they would also need to use an [External Circuit] model for the buffer
- But buffer modeling in [External Circuit] is a challenging task
  - need to use Verilog-A(MS), VHDL-A(MS) or Berkeley-SPICE
- Berkeley-SPICE does not support T-line or S-parameter models
- Consequently, [External Circuit] is not very useful in real life as it stands in the current IBIS specification

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Major improvements in IBIS v6.0

- IBIS-ISS was added as a new language option to [External Circuit] (and [External Model]) in IBIS v6.0 (September 2013)

  — IBIS-ISS offers many useful capabilities which were previously not available

  — W-element, S-parameter, etc…

- IBIS v6.0 also introduced parameter passing into [External Circuit] (and [External Model])

The last obstacle

- There is nothing in the IBIS specification that prevents [External Circuit] from being used for package modeling, other than a small statement in Table 11 (pg. 90)
  - "References enhanced descriptions of ***structures on the die***, including digital and/or analog, active and/or passive circuits"

- ***The IBIS specification doesn't allow [Model] and [External Circuit] to be cascaded***

  - most people would like to keep using [Model] for buffers
  - but there is a great need for on-die interconnect and improved package modeling in IBIS
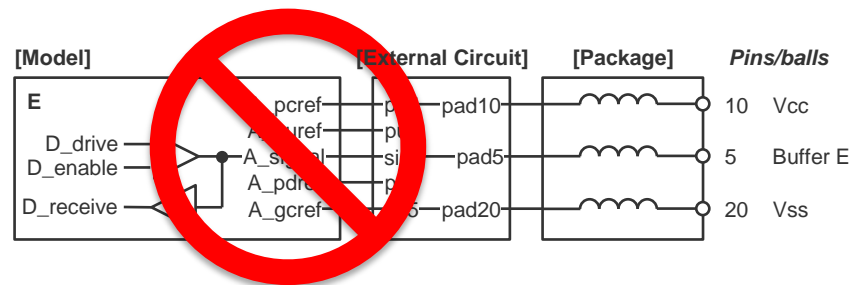
- BIRD 145 proposed a method to cascade [Model] with [External Circuit]
  - requires a [Model Call] keyword for every single instance of a [Model], making .ibs files potentially very large

The purpose of BIRD 165

- BIRD 165 proposes to extend the parameter passing mechanism from [External Circuit] to [Circuit Call]

  — same syntax as in IBIS v6.0 for [External Circuit], except it can be placed under [Circuit Call] as well

- This would allow independent parameter values to be passed into each instance of the same [External Circuit]

- It is not directly related to BIRDs 163 and 164, but it improves the flexibility of package and on-die interconnect modeling by allowing independent parameter values to be passed into the different instances of the same IBIS-ISS package and on-die interconnect models

The purpose of BIRD 164

- BIRD 164 proposes to change the statement in Table 11 (pg. 90) so that [External Circuit]s wouldn't be limited to describe only "structures on the die"

  change:

  — "References enhanced descriptions of ***structures on the die***, including digital and/or analog, active and/or passive circuits"

  to:

  — "References enhanced descriptions of ***structures on the die or package*** including digital and/or analog, active and/or passive circuits"

- In addition, it proposes a subparameter for [External Circuit] to be able mark an [External Circuit] as a package model

  — When this subparameter is present, the package model using [External Circuit] will supersede any other package model definition for the component

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The purpose of BIRD 163

- BIRD 163 deals with instantiating [External Circuit] package models, and proposes new syntax and rules for connecting any [External Circuit] instances to each other or to buffer models described by the [Model] keyword

- Note that the [Model] instantiation from the [Pin] keyword is *not* changed in this proposal

- Also, nothing is changed for [External Model]s inside [Model]

- BIRD 163 is fairly big because Section 6.3 needs to be modified is numerous places, but the concept in the proposal is relatively simple and straightforward

How does the proposal work?

Left diagram

[Model]

D
- D_drive
- D_enable
- D_receive
- A_pcref
- A_puref
- A_signal
- A_pdref
- A_gcref

implicit pad 1
implicit pad 4
implicit pad 2

[Package]

Pins/balls
- 1 Vcc1
- 4 Buffer D
- 2 Vss1

[External Circuit]

PKG

[Model]

E
- D_drive
- D_enable
- D_receive
- A_pcref
- A_puref
- A_signal
- A_pdref
- A_gcref

- pcref:5 → pc5
- puref:5 → pu5
- signal:5 → pad5
- pdref:5 → pd5
- gcref:5 → gc5

- pin10 → 10 Vcc2
- pin5 → 5 Buffer E
- pin20 → 20 Vss2

Right code listing
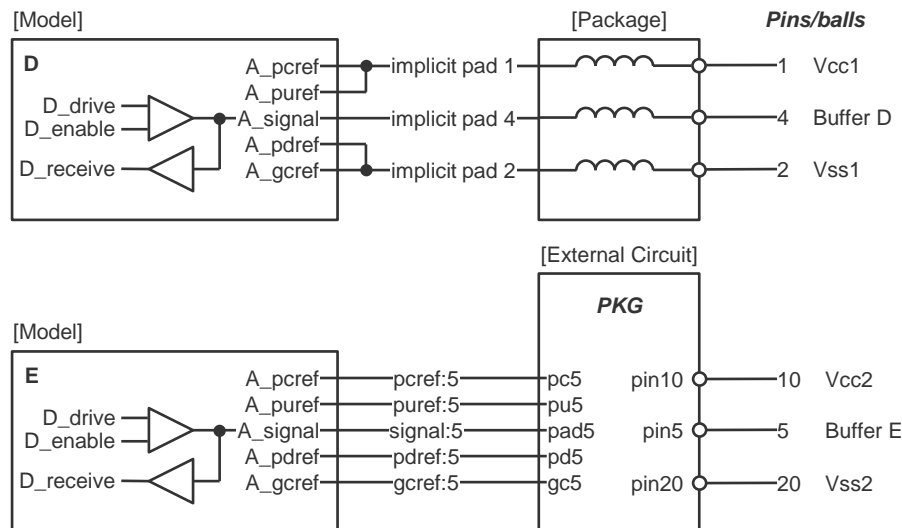
```
[Pin]    signal_name     model_name     R_pin    L_pin    C_pin
1        Vcc1            POWER
2        Vss1            GND
4        Buffer_D        MyBufferModel
5        Buffer_E        MyBufferModel
10       Vcc2            POWER
20       Vss2            GND
...
|
|************************************************************
| Instantiating external circuit PKG
|
[Circuit call]  PKG
Port_map  pin10 10         | Connection to pin 10
Port_map  pin5  5          | Connection to pin 5
Port_map  pin20 20         | Connection to pin 20
Port_map  gc5   gcref:5    | to A_pcref on [Model] of pin 5
Port_map  pd5   puref:5    | to A_puref on [Model] of pin 5
Port_map  pad5  signal:5   | to A_signal on [Model] of pin 5
Port_map  pu5   pdref:5    | to A_pdref on [Model] of pin 5
Port_map  pc5   gcref:5    | to A_gcref on [Model] of pin 5
[End circuit call]
|************************************************************
| Defining the external circuit for PKG
|
[External Circuit]  PKG
Language  IBIS-ISS
Corner  Typ  PackageModelFile.sp  PKG_subcircuitName
Ports  pin10  pin5  pin20  gc5  pd5  pad5  pu5  pc5
[End External Circuit]
|************************************************************
[Model]  MyBufferModel
Model_type  I/O
...
```

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Adding an on-die interconnect model

[Model]

E

D_drive
D_enable
D_receive

A_pcref — pcref:5 — pc5 — pad10
A_puref — puref:5 — pu5
A_signal — signal:5 — sig5 — pad5
A_pdref — pdref:5 — pd5
A_gcref — gcref:5 — gc5 — pad20

[External Circuit]
DIE

[External Circuit]
PKG

Pins/balls

pad10 pin10 — 10   Vcc2
a

pad5   pin5 — 5   Buffer E
b

pad20 pin20 — 20   Vss2
c
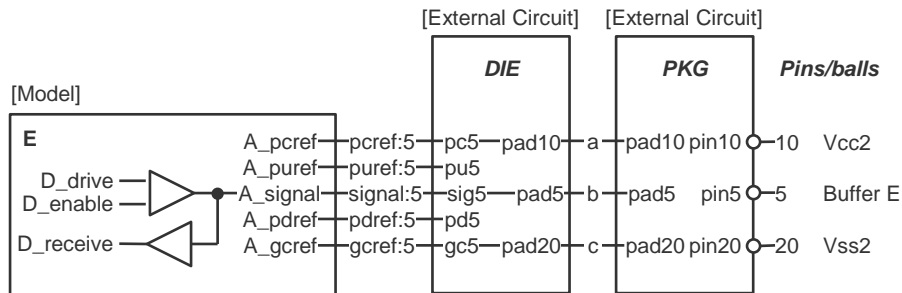
```
[Pin]   signal_name    model_name     R_pin    L_pin    C_pin
5       Buffer_E       MyBufferModel
10      Vcc2           POWER
20      Vss2           GND
...
|
[Node Declarations] | Must appear before [Circuit Call]
a   b   c
|*************************************************************
| Instantiating external circuit PKG
|
[Circuit call]  PKG
Port_map  pin10 10        | Connection to pin 10
Port_map  pin5  5         | Connection to pin 5
Port_map  pin20 20        | Connection to pin 20
Port_map  pad20 c         | Connection to explicit pad c
Port_map  pad5  b         | Connection to explicit pad b
Port_map  pad10 a         | Connection to explicit pad a
[End circuit call]
```

```
|**********************************************************
| Instantiating external circuit DIE
|
[Circuit call]  DIE
Port_map  pad10 a          | Connection to explicit pad a
Port_map  pad5  b          | Connection to explicit pad b
Port_map  pad20 c          | Connection to explicit pad c
Port_map  gc5   gcref:5    | to A_pcref on [Model] of pin 5
Port_map  pd5   puref:5    | to A_puref on [Model] of pin 5
Port_map  sig5  signal:5   | to A_signal on [Model] of pin 5
Port_map  pu5   pdref:5    | to A_pdref on [Model] of pin 5
Port_map  pc5   gcref:5    | to A_gcref on [Model] of pin 5
[End circuit call]
|**********************************************************
| Defining the external circuit for PKG
|
[External Circuit]  PKG
Language  IBIS-ISS
Corner  Typ  PackageModelFile.sp  PKG_subcircuitName
Ports  pin10  pin5  pin20  pad20  pad5  pad10
[End External Circuit]
|
| Defining the external circuit for DIE
|
[External Circuit]  DIE
Language  IBIS-ISS
Corner  Typ  PackageModelFile.sp  PKG_subcircuitName
Ports  pad10  pad5  pin20  gc5  pd5  sig5  pu5  pc5
[End External Circuit]
|**********************************************************
[Model]  MyBufferModel
Model_type  I/O
...
```

Thank you

Questions?

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