IBIS Open Forum Minutes

Meeting Date: **January 31, 2014**
Meeting Location: **DesignCon IBIS Summit, Santa Clara, CA, USA**

VOTING MEMBERS AND 2014 PARTICIPANTS

Agilent Technologies	Radek Biernacki*, Nilesh Kamdar*, Colin Warwick*, Graham Riley*, Pegah Alavi*, Fangyi Rao*, Heidi Barnes*
Altera	David Banas*, Kundan Chand*, Hsinho Wu*
ANSYS	(Steve Pytel)
Applied Simulation Technology	Fred Balistreri*, Norio Matsui*
Cadence Design Systems	Ambrish Varma*, Brad Brim*, Joy Li*, Kumar Keshavan*, Ken Willis*, Yingxin Sun*, Joshua Luo*, John Phillips*
Ericsson	Anders Ekholm*, Zilwan Mahmod*
Foxconn Technology Group	(Sogo Hsu)
Huawei Technologies	Jinjun Li*, Xiaoqing Dong*
IBM	Adge Hawes*
Infineon Technologies AG	(Christian Sporrer)
Intel Corporation	Michael Mirmak*, Jon Powell*, Riaz Naseer* Udy Shrivastava*, Mustafa Yousuf*, Jimmy Johnson*
IO Methodology	Lance Wang*, Michelle Coombs*
LSI	Xingdong Dai
Maxim Integrated Products	Hassan Rafat*
Mentor Graphics	Arpad Muranyi*, John Angulo, Fadi Deek*
Micron Technology	Randy Wolff*
Signal Integrity Software	Mike LaBonte*, Walter Katz*, Todd Westerhoff*, Michael Steinberger*
Synopsys	Ted Mido*, Scott Wedge*
Teraspeed Consulting Group	Bob Ross*, Tom Dagostino*, Scott McMorrow*
Toshiba	(Yasumasa Kondo)
Xilinx	Ravindra Gali*
Zuken	Michael Schaeder*, Amir Wallrabenstein*, Griff Derryberry*

OTHER PARTICIPANTS IN 2014

ECL Advantage	Thomas Iddings*
Hewlett Packard	Ting Zhu*
KEI Systems	Shinichi Maeda*
Lattice Semiconductor	Xu Jiang*
Mellanok Technologies	Piers Dawe*
Pangeya	Edgar Aguirre*
Proficient Design	Kishor Patel*
SAE International	Chris Denham*
Vitesse	Siris Tsang*

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
February 21, 2014	205 475 958	IBIS

For teleconference dial-in information, use the password at the following website:

https://ciscosales.webex.com/ciscosales/j.php?J=205475958

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

OFFICIAL OPENING

The IBIS Open Forum Summit was held in Santa Clara, California at the Santa Clara Convention Center during the 2014 DesignCon conference. About 59 people representing 26 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.eda.org/ibis/summits/jan14/

Michael Mirmak welcomed everyone to the Summit, opening the meeting at 8:30AM. He thanked the sponsors including Agilent Technologies for providing the food as well as DesignCon. Michael asked all the participants to introduce themselves. There was a large cross section of model users and developers. Many people had worked with IBIS since its founding in 1995.

CHAIR'S STATUS REPORT

Michael Mirmak, Intel

Michael Mirmak began by noting the events and progress in 2013. IBIS has moved to a new parent organization, SAE International. IBIS 6.0 is approved and the parser development is in progress. IBIS Summits in Asia and Europe continue. Arpad Muranyi noted that rejections of many BIRDs were due to rewrites to combine concepts into new BIRDs. Michael continued by showing how long versions of IBIS have lived before they were updated. Most versions have lived for more than a year. Moving to a 6-month release cycle will require quicker updates. 10 BIRDs are currently open and most are package related. Michael detailed the requirements needed to move to a 6-month release schedule. He also asked if the next version of IBIS should be 6.1, 7.0 or a date-based version number. The question is directly related to parser funding requirements. A proposal is to move to a combined membership and parser contribution model in 2015. This would align with moving to a new version numbering. He also proposed making the next version 6.1 with focus on IBIS-ISS parsing. Our focus for the first half of 2014 is package modeling.

Arpad noted that 6.0 is already over 6 months old since it was approved in May of 2013. Jon Powell noted that the parser originally was funded through license sales. Bob Ross added that in the beginning, there was an option for combined membership and parser contribution for one year. Michael Schaeder noted that his software would probably only incorporate IBIS changes in an update once a year. Kumar Keshavan felt that it would be difficult to set a hard rule on release cycle due to the complexity of changes for some releases. Scott Wedge added that his company works on a 9 month release schedule. Ken Willis said for his company that they usually have one major and one minor release per year. A 6-month schedule is too quick, but a one year release sounds good. Ted Mido noted that customers typically ask about IBIS support in software releases after a new IBIS specification is released.

RANTINGS OF AN IBIS MINIMALIST
Ken Willis, Cadence Design Systems

Ken Willis began by describing the beginnings of IBIS in 1993. The focus was on replacing transistor level IO models. Lumped packages were ok and power was ideal. The focus of IBIS was the IO buffer and interconnect modeling was the domain of the EDA tool. Then, data rates increased, keywords were added for new complexities, EBD was added and new package model options were added. [External Model] was added, non-ideal power models were added and algorithmic modeling was invented. In 20 years, IBIS has achieved the original focus.

Ken went on to say that inventing new things such as AMI is worth it. Standardizing interconnect modeling is difficult. As complexity goes up, keyword driven specifications break down. Ken asked how we should handle interconnect modeling. Ken ranted by saying that an interconnect modeling format is not something new we need to invent. What is missing in IBIS is a standard, convenient way to define connectivity between big interconnect Spice subcircuits. He showed Model Connection Protocol as an example of connection syntax. He would like to see a focus on defining a standard way to define connectivity between subcircuits.

Walter Katz agreed that IBIS-ISS is the best way to model interconnects. The problem is in defining the connections of these subcircuits.

SAE INTERNATIONAL INTRODUCTION

Chris Denham, SAE International

Chris Denham began by describing SAE International. It is a technical organization with focus on aerospace, commercial vehicles and automotive standards. SAE was formed in 1905. The TechAmerica standards program and IBIS were integrated into SAE in 2013. IBIS is a part of the SAE Industry Technologies Consortia (ITC). ITC provides all the legal, administrative and accounting services to IBIS. IBIS is considered a technical committee and the IBIS charter defines the scope, committee purpose and the program of work. Committee membership levels include leadership, member, liaison and mailing list. SAE Standards Works is a workflow and collaboration tool used by all SAE technical committees. Chris showed a screenshot of the Standards Works tool. Resources on the site include the organization and operating guide. Other documents on the site can include the last 5 years of meetings minutes.

Adge Hawes asked if the SAE change has led to a fee change for membership. Michael Mirmak responded that this has not changed; however, invoices are handled by the new organization. Scott Wedge asked about the relationships of SAE to other organizations. Chris responded that SAE does have relationships with many other international organizations. Ambrish Varma asked if IBIS was under the aerospace organization within SAE. Chris confirmed that this is true, but there is discussion about moving it to the same level in the hierarchy as the aerospace organization.

IBIS-ATM TASK GROUP REPORT
Arpad Muranyi, Mentor Graphics

Arpad Muranyi began by listing all the BIRDs integrated into IBIS 6.0 in 2013. BIRD155.2 was approved since the IBIS 6.0 release. BIRDs in progress are focused on package modeling, but there are also BIRDs on AMI Touchstone models, back-channel support, AMI parameter passing, parameterization of [Driver Schedule] and support for incomplete and buffer-only [Component] descriptions.

IBIS PACKAGE MODELING PROPOSAL WITH [EXTERNAL CIRCUIT]
Arpad Muranyi*, Ambrish Varma**, Mentor Graphics*, Cadence Design Systems**

Arpad Muranyi began by noting that existing package modeling features in IBIS are very outdated. Several proposals are being evaluated and discussed in the IBIS ATM task group. Arpad discussed BIRD proposals 163-165. [External Circuit] is made available for package modeling, like it has been available for on-die interconnect modeling. [External Circuit] has not been popular, because it cannot be cascaded with [Model]. In IBIS 6.0, IBIS-ISS was added as a new language option for [External Circuit], and parameter passing into [External Circuit] was also added. Only one small statement in IBIS prevents use of [External Circuit] for package modeling. Also, the IBIS specification does not allow [Model] and [External Circuit] to be cascaded.

BIRD165 proposes extending parameter passing mechanisms for [External Circuit] to [Circuit Call]. This allows independent parameter values to be passed into each instance of the same [External Circuit]. BIRD164 proposes changing a statement in Table 11 to support [External Circuit] package models as well as adding a subparameter for [External Circuit] to mark its use for package modeling. BIRD163 describes all the new syntax and rules required for cascading

[Model]s with [External Circuit]. Arpad showed two examples of a package model connecting to a [Model] and a package model cascaded with an on-die interconnect model connecting to a [Model].

Anders Ekholm asked how the power connections to the buffer are handled. Arpad clarified that there is a rule about [Pin Mapping] that prevents problems of contention between two package models connecting to the same buffer's power terminals.

Walter Katz asked how the Corner subparameter is used with package models, since typ/min/max has different context with package modeling. Arpad said that the rules for [External Circuit] are not changed for definitions of Corner cases.

Randy Wolff asked if there would be any contention between two [External Circuit] package models within the same IBIS file related to different [Pin] lists. Arpad noted that [Circuit Call] exists under the [Pin] level, so this prevents any contention.

Mike LaBonte noted it would be good to continue the colon syntax such as 'pin:10' to prevent confusion. Adge Hawes asked if more than 3 corner cases of package models could be defined. Arpad described how parameter passing could be used to define unlimited corners. Mike LaBonte asked how multiple package models could be used. Would the tool allow selection of them? Arpad clarified that the BIRD does not allow for this, but the idea could be entertained.

IBIS PACKAGE PROPOSAL

Walter Katz, Signal Integrity Software (SiSoft)

Walter Katz began by noting the evolution of EMD, IBIS-ISS and the package modeling proposal he has been writing. Many decisions have been made in the ATM task group about what types of packages will be supported within the IBIS file and others that will be supported in EMD. Signal pins must have a one-to-one correspondence between pin, pad and buffer, meaning that MCPs must be supported in EMD. Walter went on to describe some defined syntax such as a new keyword [Begin Package Model]. The proposal supports IBIS-ISS and Touchstone directly. Parameter passing is defined, including some typing such as for delay and crosstalk. Enhanced parameter formats are defined, mostly for support of DOE simulation. Subparameters are used to describe port connections as well as sparse port connections to large S-parameter files. Walter defined signal port naming rules for package models connecting to specific models as well as those connecting to IO types such as FEXT/NEXT models. There are separate rules for supply port naming. Rules are defined for terminating unused ports of S-parameter models when sparse port connections are used.

Walter presented a list of functionality supported in his proposal. The next step is to evaluate this proposal along with the alternative (BIRDs 163-165). Which proposals solve IC vendor and user problems including functionality, ease of writing models and IBIS files, and ease of parsing IBIS files and models?

Lance Wang asked about naming rules for ports when you have mixed inputs and outputs in the model. Walter confirmed that the syntax defines whether a model might connect to an input pin, an output pin, or both. This is important for FEXT/NEXT simulation.

Michael Mirmak asked if this proposal gets rid of existing IBIS syntax such as [Pin] and [Pin Mapping]. Walter said that existing IBIS syntax, including [Pin Mapping] and [External Circuit], does not address existing issues. He confirmed that the existing [Pin] section is not changed. Todd Westerhoff commented that the SiSoft viewpoint looks to create simpler syntax to make models easier to write.

IBIS-AMI VALIDATION

Zilwan Mahmod and Anders Ekholm, Ericsson

Zilwan began by describing design goals he has with IBIS AMI analysis. IBIS AMI models must be validated, as correct and validated models are needed. Certification is the first step a model must go through to check that the model behavior is reasonable. Zilwan presented a long checklist of items to verify. To do active correlation, the PCB model in simulation must be adjusted to match the real channel characteristics as seen in measurements. S-parameters from measurement can be used in the correlation exercise, but the PCB models need to be adjusted for later use in post-layout simulation. TX active validation is feasible, but RX active validation is not, because measurements at the decision point are not possible.

Zilwan's experience shows that many models fail certification for various reasons such as syntax errors, run time errors, simulated DC levels that don't match measured DC levels, idealized analog models, etc.

A question was asked about how the waveforms are correlated. Zilwan responded that this is done visually. Mike Steinberger commented that a figure-of-merit (FOM) could be used. Colin Warwick asked how long for simulation time is reasonable. Zilwan responded that 2-3 minutes per million bits is reasonable. Some models take 30 minutes or more, and this is unacceptable. A question was asked about what is desired to correlate on an RX. Mike Steinberger suggested that starting with eye height and eye width would be useful. Todd Westerhoff noted that some RX designs include internal eye measurement capabilities, and access to this data would be useful. Scott McMorrow noted that you first have to have ways to calibrate the internal RX measurement tool, and these methods don't exist and/or aren't standardized.

AN ADVANCED BEHAVIORAL BUFFER MODEL WITH OVER-CLOCKING SOLUTION

Yingxin Sun, Joy Li and Joshua Luo, Cadence Design Systems

Joshua Luo began by describing the mechanisms related to overclocking of IBIS models. A simulator that does not properly window V-T data will give incorrect results, sometimes showing missing bits. V-T windowing works well for IBIS 4.2 models. However, for IBIS 5.0 models that include I-T data, using the same V-T windowing algorithm will cut off the pre-driver current seen in the [Composite Current] I-T data. Joshua proposed an advanced over-clocking solution, where a pre-driver stage was added to the driver stage. With this model, the [Composite Current] could be broken into two portions, the contribution from the driver and the contribution from the pre-driver. The proposed over-clocking solution could be implemented into an advanced IBIS simulator to automatically handle the windowing of both V-T and I-T data. With this solution, very good correlation was seen between IBIS and the original transistor model for real SSO simulation, even under over-clocking scenarios.

David Banas asked how the advanced buffer model was created. Brad Brim clarified that macromodel syntax was used to combine a B-element and other circuit elements within one subcircuit, linked into a simulator using [External Model]. Scott McMorrow pointed out that the power aware modeling assumes that the pre-driver is insensitive to supply noise. Measurements could be made on a real device to create a better model than Spice.

Lance Wang noted that Cadence has presented this information several times before. He asked if Cadence would be willing to donate the technology to the IBIS community to improve all model simulations. Brad Brim noted that this idea has been considered.

Walter Katz talked about a different method for power design at the board level, where only the frequency spectrum of the current for the chip is provided. Brad noted that this could be a practical approach, but current approaches require SSO simulation using the methods described.

BUILD YOUR OWN IBISCHK

Bob Ross* and Mike LaBonte**, Teraspeed Consulting Group*, SiSoft**

Bob Ross began by describing reasons why someone might want to own the ibischk source code. Some bugs in the code are not fixed immediately, so companies may want to fix the code on their own. Companies may want to make custom modifications. Also, ibischk might need to be compiled to support specific Linux versions. Source code licenses are available for $2500. License sales pay for new ibischk development. Owners of source code will help improve ibischk6. ibischk6 code will be available around May 15, 2014.

Bob noted that a quality assurance test suite is included with the source code. Adge Hawes asked if it has ever been considered to go open source on the source code. Michael Schaeder noted that it would have to be a LGPL license. David Banas commented that the code might not get updated when needed if we weren't relying on a contractor, but instead relying on volunteers.

MEMORY PACKAGING TECHNOLOGY & MODELING

Randy Wolff, Micron Technology

Randy Wolff began by noting that he was presenting information on memory packaging technology to aid in current discussions on package modeling improvements in IBIS. He presented the package design tradeoffs including density, performance, cost and customization. He went on to describe DRAM packaging terminology for single die and stacked die solutions. DRAM packaging solutions trend towards reduced parasitics for higher speed and stacked solutions. RDL is a technology used in memory stacks, and Randy considers it part of the package and not specifically on-die interconnect.

Randy continued by defining terminology used in NAND, NOR and MCP packaging solutions. He identified packaging trends in NAND, NOR, wireless and embedded applications. Micron's current package modeling solutions for single-die packages include use of IBIS package models, fully-coupled Spice models with higher bandwidths, and S-parameter models for DDR4

and SerDes products. Stacked packages are modeled with IBIS EBD as well as some lossy, uncoupled Spice models.

Future package modeling solutions need to include IBIS-ISS, on-die PDN modeling with IBIS-ISS, mixed formats, and various S-parameter solutions for modeling SerDes links including single data lane, victim/aggressor models, and FEXT/NEXT models.

Bob Ross asked if Micron supported one of the package modeling proposals presented earlier. Randy responded that he was not ready to support a specific proposal yet, but any proposal needed to cover the package modeling solutions he presented. A combination of the best of each proposal might be good.

OPEN DISCUSSION

Brad Brim asked about support of power aware IBIS models from IC vendors. Brad is not seeing many companies create IBIS power aware models, yet there are many SSO simulation presentations talking about IBIS 5.0 models. Randy Wolff noted that his company is providing and supporting these models. Michael Mirmak noted that discussions about power problems are being talked about in parallel interfaces but not SerDes interfaces. Mike Steinberger noted that power issues cannot be ignored in SerDes systems. Arpad Muranyi added that discussions in the IBIS ATM task group have talked about adding power effects into AMI as jitter contributions. Mike S. noted that the IC designer and the system designer together have all the information they need, but they are not in the same company typically. Fangyi Rao commented that the SerDes vendor needs to specify the power to jitter relationship. Brad asked what the system designer needs. Fangyi responded that spectral plots of power noise are good. Model specific parameters could be used to model these effects today. The system designer provides a model of power noise to the AMI model, which converts it to jitter.

Mike LaBonte commented that we might get models of VRMs if they are standardized in something like IBIS.

Tom Dagostino asked why there is a limitation in IBIS for a one-input one-output situation. He has a clock buffer with one input and four outputs for a SerDes application. Mike S. noted that the repeater solution in IBIS 6.0 was only for repeaters, not a broadcast part. Tom added that the customer wanted to model the additive jitter from the clock tree. Mike S. noted that this group has not looked at modeling this effect.

Brad commented that customers are asking for IBIS format Spice package models right now. Why can't we have a solution that provides this right now, and add on the pre-layout type package models later on? Arpad noted that his syntax could be adjusted fairly easily to do what Walter's syntax is providing, essentially providing a way to build up models more easily. Arpad is wondering if the better approach is to leave behind old syntax and start new or modify existing syntax to limit changes in the software. Mike S. described the need to re-factor any software at some point in its lifecycle. Arpad noted that it is difficult to ask model makers to relearn everything. Mike S. suggested that we should look at both proposals and see if there are good things in both that can be used, but some syntax may have outlived its usefulness. Bob pointed out that there are lots of requested changes in the proposals, and the parser would take a long time to be completed. A reduced set of options might be needed. Mike S. suggested that Arpad and Walter combine efforts to compromise on a solution that reduces the

pain of changes. Michael took an AR to find someone to mediate discussions between the two parties.

CONCLUDING ITEMS

Michael Mirmak thanked the sponsor Agilent Technologies, the presenters, organizers and attendees.

The meeting concluded at approximately 4:30 PM.

NEXT MEETING

The next IBIS Open Forum teleconference will be held February 21, 2014 from 8:00 a.m. to 10:00 a.m. US Pacific Time.

==========

NOTES

IBIS CHAIR: Michael Mirmak (916) 356-4261, Fax (916) 377-3788
michael.mirmak@intel.com
Data Center Platform Applications Engineering
Intel Corporation
FM5-239
1900 Prairie City Rd.,
Folsom, CA 95630

VICE CHAIR: Lance Wang (978) 633-3388
lwang@iometh.com
President/CEO, IO Methodology, Inc.
PO Box 2099
Acton, MA 01720

SECRETARY: Randy Wolff (208) 363-1764, Fax: (208) 368-3475
rrwolff@micron.com
Principal Engineer, Modeling Group Lead, Micron Technology, Inc.
8000 S. Federal Way
Mail Stop: 01-711
Boise, ID 83707-0006

LIBRARIAN: Anders Ekholm (46) 10 714 27 58, Fax: (46) 8 757 23 40
ibis-librarian@eda.org
Digital Modules Design, PDU Base Stations, Ericsson AB
BU Network
Färögatan 6
164 80 Stockholm, Sweden

WEBMASTER: Mike LaBonte

mikelabonte@eda.org
IBIS-AMI Modeling Specialist, Signal Integrity Software
6 Clock Tower Place
Maynard, MA 01754

POSTMASTER: Mike LaBonte
mikelabonte@eda.org
IBIS-AMI Modeling Specialist, Signal Integrity Software
6 Clock Tower Place
Maynard, MA 01754

This meeting was conducted in accordance with ANSI guidance.

The following e-mail addresses are used:

majordomo@eda.org

In the body, for the IBIS Open Forum Reflector:
subscribe ibis <your e-mail address>

In the body, for the IBIS Users' Group Reflector:
subscribe ibis-users <your e-mail address>

Help and other commands:
help

ibis-request@eda.org

To join, change, or drop from either or both:
IBIS Open Forum Reflector (ibis@eda.org)
IBIS Users' Group Reflector (ibis-users@eda.org)
State your request.

ibis-info@eda.org

To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the IBIS Open Forum as a full Member.

ibis@eda.org

To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

ibis-users@eda.org

To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda.org

To report ibischk parser BUGs as well as tschk2 parser BUGs. The BUG Report Form

for ibischk resides along with reported BUGs at:

http://www.eda.org/ibis/bugs/ibischk/
http://www.eda.org/ibis/bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.eda.org/ibis/tschk_bugs/
http://www.eda.org/ibis/tschk_bugs/bugform.txt

icm-bug@eda.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/ibis/icm_bugs/
http://www.eda.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda.org/ibis/bugs/s2ibis/bugs2i.txt
http://www.eda.org/ibis/bugs/s2ibis2/bugs2i2.txt
http://www.eda.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eda.org/ibis

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda.org/ibis/directory.html

Other trademarks, brands and names are the property of their respective owners.

IBIS – SAE STANDARDS BALLOT VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

Organization	Interest Category	Standards Ballot Voting Status	November 22, 2013	December 6, 2013	January 10, 2014	January 31, 2014
Agilent Technologies	User	Active	X	X	X	X
Altera	Producer	Inactive	-	-	-	X
ANSYS	User	Inactive	X	-	-	-
Applied Simulation Technology	User	Inactive	-	-	-	X
Cadence Design Systems	User	Active	X	X	X	X
Ericsson	Producer	Inactive	X	-	-	X
Foxconn Technology Group	Producer	Inactive	-	-	-	-
Huawei Technologies	Producer	Inactive	-	-	-	X
IBM	Producer	Active	-	X	X	X
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Intel Corp.	Producer	Active	X	-	X	X
IO Methodology	User	Active	-	-	X	X
LSI	Producer	Inactive	-	-	X	-
Maxim Integrated Products	Producer	Inactive	-	-	-	X
Mentor Graphics	User	Active	-	X	X	X
Micron Technology	Producer	Active	-	X	X	X
Signal Integrity Software	User	Active	-	X	X	X
Synopsys	User	Inactive	-	-	-	X
Teraspeed Consulting	General Interest	Active	-	X	X	X
Toshiba	Producer	Inactive	X	-	-	-
Xilinx	Producer	Inactive	-	-	-	X
Zuken	User	Inactive	X	-	-	X

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

INTEREST CATEGORIES ASSOCIATED WITH SAE BALLOT VOTING ARE:

- USERS - MEMBERS THAT UTILIZE ELECTRONIC EQUIPMENT TO PROVIDE SERVICES TO AN END USER.
- PRODUCERS - MEMBERS THAT SUPPLY ELECTRONIC EQUIPMENT.
- GENERAL INTEREST - MEMBERS ARE NEITHER PRODUCERS NOR USERS. THIS CATEGORY INCLUDES, BUT IS NOT LIMITED TO, GOVERNMENT, REGULATORY AGENCIES (STATE AND FEDERAL), RESEARCHERS, OTHER ORGANIZATIONS AND ASSOCIATIONS, AND/OR CONSUMERS.