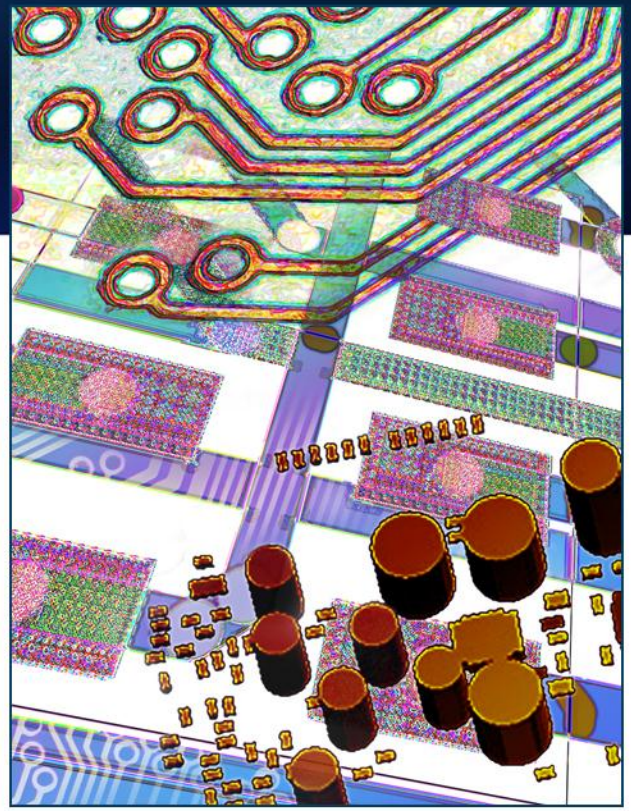
What's Wrong with IBIS?



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Background

- We have spent a huge amount of time discussing the analog modeling proposals without reaching a conclusion yet
- The stalemate seems to be caused by two types of issues:
  1) different interpretations of fundamental IBIS concepts
     - it is hard to come to an agreement on a proposed feature and/or its syntax when we disagree on what the input of [Model] is, see:

     http://www.vhdl.org/pub/ibis/macromodel_wip/archive/20130108/arpadmuranyi/Analog%20Modeling%20Discussion/AnalogModelingDiscussion.pdf
  2) "Keep and Tweak" vs. "Invent and Leave Behind"
     - we don't want to discard the huge IBIS infrastructure as there are lots of IBIS models and EDA tools out there
     - proposals (BIRDs) with the "minimalist" change philosophy don't seem to be popular - "gobbledygook"
     - proposals with larger changes raise deprecation questions
- Stated or not, recent discussions indicate that we seem to favor a more fundamental overhaul of the specification

Two main categories of improvements

- Analog buffer modeling
  - a burning need for AMI
  - highly desirable for legacy simulations also
  - would be nice to find a solution that works in both areas
- Package and on-die interconnect modeling
  - the IBIS package features are basically not used in "decent" models
  - a burning need for all types of simulations
  - on-die interconnect modeling is becoming important in high speed SerDes (AMI) and stacked die simulations
- Both areas suffer from issues with *content* and *usage*
  - data inside the [Model] or [Package] keywords
  - connectivity information in the [Pin], [Pin Mapping], etc… keywords
  - simulation flow issues affecting EDA vendor and/or model maker

What's wrong with [Model]?

- Inherently single ended
- No support for on-die interconnect
  - [Model] is assumed to be connected directly to the die pad
  - power distribution with [Pin Mapping] is very limited and ugly
  - there is no [Pad] keyword to support forks in the package
- No support for stacked die
  - only one [Model] can be instantiated from the [Pin] keyword
- No support for scaling or parameterization
  - sweep or "what if" simulations are only possible through [Model Selector]
- A constant valued C_comp is not sufficient
- [External Model] and [External Circuit] not popular
  - the *-AMS languages didn't take off
  - the instantiation/connection syntax is not friendly
- No support for pre vs. post layout modeling
  - simulating without exact pin names and/or package/interconnect models

What's wrong with [Package]?

- RLC just doesn't cut it any more
  - no frequency dependencies
  - no dielectric losses (G)
- No coupling with multi-segment traces
- Only single segment traces are possible with coupled RLC matrices
- Assumes one-to-one pin-to-pad mapping
- No support for stacked die
- No support for pre vs. post layout modeling

How can we address all these issues?

- [External Model] and [External Circuit] were introduced to IBIS to provide a solution for the shortcomings of [Model] but didn't deliver the promise we hoped for
- IBIS-ISS (or IBIS-BSS later) as new language(s) could solve many problems, *but not all of the problems*
- The more improvements we add to the existing IBIS keywords, the more complicated and messy they get
- *The best choice seems to be to "start over" with a cleaner and better syntax*
- We need to do this in a "parallel" fashion with a careful plan which allows for incremental transition to the new syntax
  - make small, short term improvements while working on "new IBIS"
- Don't throw out the baby with the bath water...
  - retain the good stuff

Conclusion / Call for action

- None of the existing proposals or BIRDs address all of the problems in IBIS individually or collectively
- We can't continue making inflexible, application specific and "patchwork" style improvements indefinitely
  - *this would guarantee that we would always be lagging the industry*
- Let's make a conscious decision for a planned effort to create an improved and flexible IBIS specification
  - *general purpose solutions last longer because of their flexibility*

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