Interconnect Task Group Status Update

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IBIS Summit at DesignCon

Santa Clara, California

January 31, 2013

Background

- The Interconnect Task Group was suspended in July 2011 after IBIS-ISS work was completed
  - Time slot was used for Editorial TG meetings (IBIS 5.1)
  - IBIS 5.1 was released in August 2012
  - Interconnect work restarted in September 2012
- Problem: IBIS package modeling insufficient
  - Per-pin or per-component lumped RLC
  - Single-section coupled model (no AC losses)
  - Multi-section distributed single-line model (no AC losses)

How to update IBIS to accommodate
today's industry package modeling needs?

How to integrate IBIS, IBIS-ISS and Touchstone
to cover industry interconnects more broadly?

General Needs

- Proposals being discussed are intended to address modeling requirements for various interconnect types
  - Packages
  - Multi-chip modules
  - Connectors
  - Interposers
  - Sockets
  - Cables
  - On-Die interconnect descriptions

- Key issues include
  - Backward compatibility?
  - Compatibility with other industry group approaches (e.g., Si2)?
  - Differences between interconnects for traditional IBIS and IBIS-AMI?
  - Ambiguities in the structure of [Model] exist & affect packaging?

Thanks to Walter Katz for the type list!

Presentations & Proposals

- Documents available on http://www.eda.org/ibis/interconnect_wip/

- Problem description
  - Background and proposals from Arpad Muranyi, Mentor Graphics
  - www.eda.org/ibis/interconnect_wip/PackageModeling_NewDirections.pdf

- Electronic Module Description (EMD) Specification, Draft 0
  - Proposal from Walter Katz, Signal Integrity Software (SiSoft)
  - www.eda.org/ibis/interconnect_wip/EMD.docx
  - Several other proposals available showing EMD in specific applications

Upcoming Work

- Analysis of Si2 specification proposals
  - Now under 60 day closed comment period
  - Expected for public disclosure late February
  - www.si2.org

- Resolve (with ATM) nature of [Model] stimulus
  - This is critical to IBIS-AMI interoperability
  - The nature of [Model] affects how analog device information is allocated among package, on-die interconnect and buffer sections

- EMD and any other proposals can be evaluated once these are complete

Your feedback is encouraged!
Thanks to our participants and contributors!