

Interconnect Modeling Status

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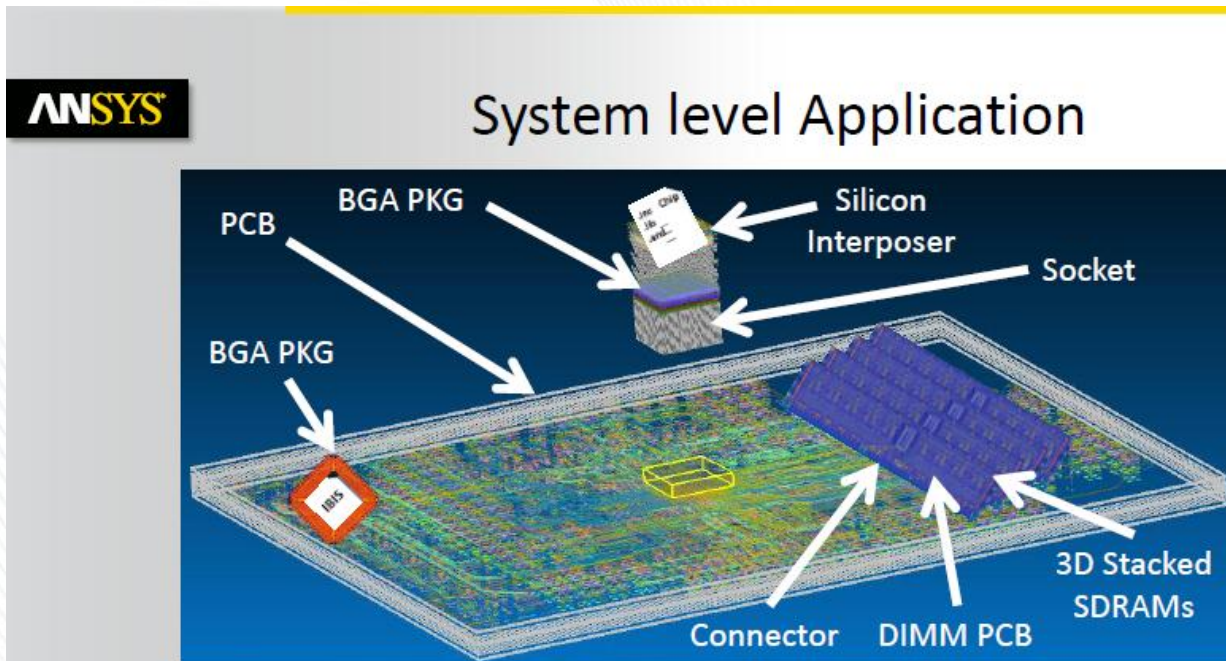
Overview

- History of Presentations
- Assumption is that the EMD concepts can satisfy the needs of the IBIS community from Die to Die
- On-Die Models
- IBIS 5.1 Limitation
- The IC Vendor Needs to Partition the 5.1 Buffer into a IBIS-ISS or Tstonefile On-Die Interconnect and a Different 6.0 Buffer
- Conclusion

History of Presentations

- IBIS EMD Pre vs Post, Requirements
 - http://www.eda.org/ibis/interconnect_wip/IBIS_EMD_12-05-2012.pdf
- Package EBD/EMD
 - http://www.eda.org/ibis/adhoc/interconnect/Package_EBD_EMD.pptx
- Electronic Module Description Specification, Draft 0
 - <http://www.eda.org/ibis/adhoc/interconnect/EMD.docx>
- Die-to-Die Connections in EMD
 - <http://www.eda.org/ibis/adhoc/interconnect/Die2Die.pdf>
- MCI and EMD ...
 - LINK TBD

IBIS EMD Pre vs Post, Requirements



- IBIS: Commonly used for DDR simulations
 - DDR4, Wide I/O, Hybrid Memory Cube, ...
- IBIS-AMI: Commonly used for SERDES simulations
 - PCIe, SATA, SAS, HDMI, USB, ...

One Package Interconnect View

Pins

Pads

A1 DQ1

A2 DQ2

A3 DQ3

A4 DQ4

A5 DQ5

B1 VDD

B2 VDD

B3 VDD

D.DQ1

D.DQ2

D.DQ3

D.DQ4

D.DQ5

D1.VDD

D2.VDD

D3.VDD

D4.VDD

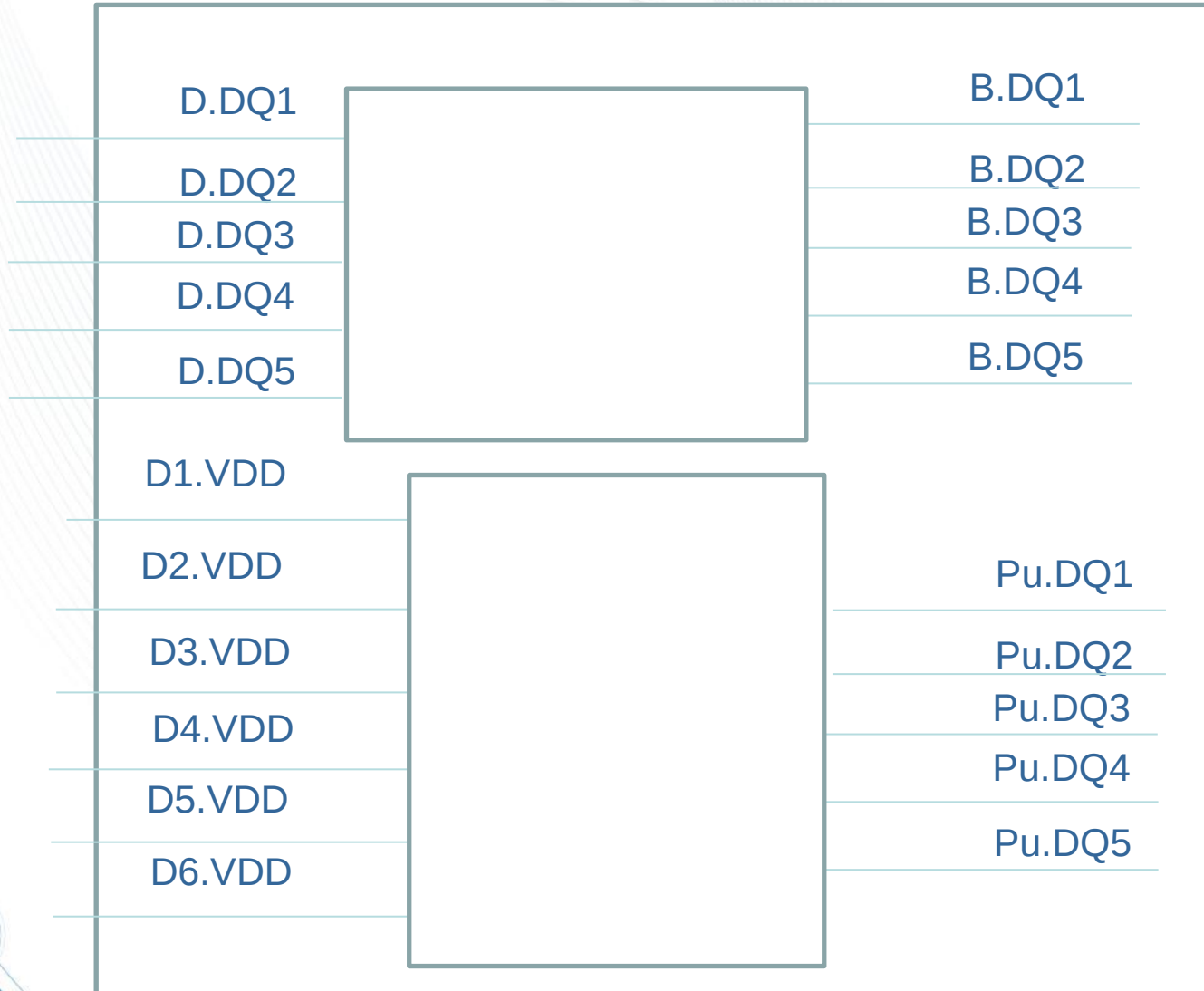
D5.VDD

D6.VDD

One Die Interconnect View

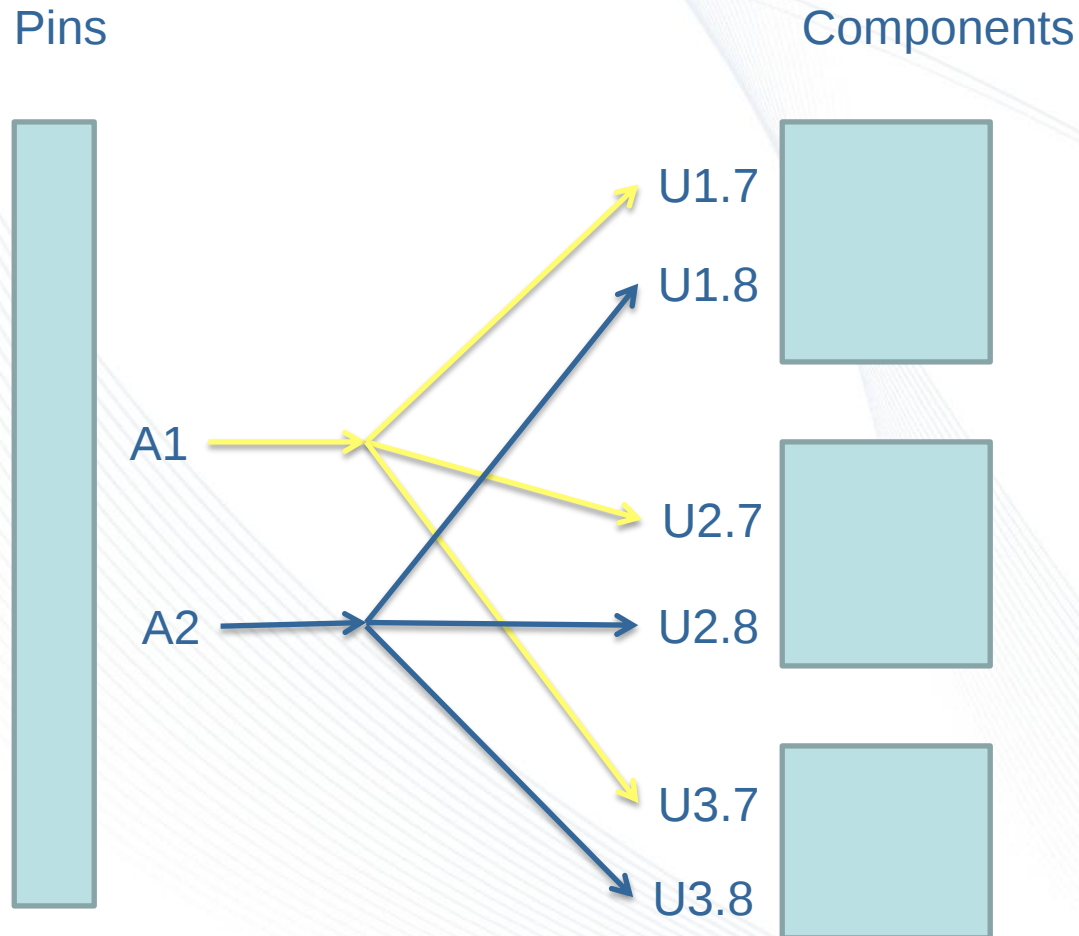
Pads

Buffers



Electronic Module Description (EMD)

MCM is a Package with Multiple Die



Connector is an EMD

Side A Pins

Side B Pins



EMD using Parameter Tree Format

(Example

(IBIS_Ver 6.0)

(File_name Example.emd)

(Module

(Name Example)

(Manufacturer SiSoft)

(Number_Of_Pins 2)

(Pins

(A1 XYZ)

(A2 DEF))

(Extended_Nets

(XYZ A1 U1.7 U2.7 U3.7)

(DEF A2 U1.8 U2.8 U3.8))

(IBIS-ISS_Package Example.ipkg)

(Reference_Designator_Map

(U1 memory.ibs memory)

(U2 memory.ibs memory)

(U3 memory.ibs memory))

))

Example.ipkg

(XYZ

(File Example.iss) (Subckt XYZ)

(Model_Ports

(1 (Pin_name A1))

(2 (Pin_name 7) (Ref_des U1))

(3 (Pin_name 7) (Ref_des U2))

(4 (Pin_name 7) (Ref_des U3))

)

)

(DEF

(File Example.iss) (Subckt DEF)

(Model_Ports

(1 (Pin_name A2))

(2 (Pin_name 8) (Ref_des U1))

(3 (Pin_name 8) (Ref_des U2))

(4 (Pin_name 8) (Ref_des U3))

)

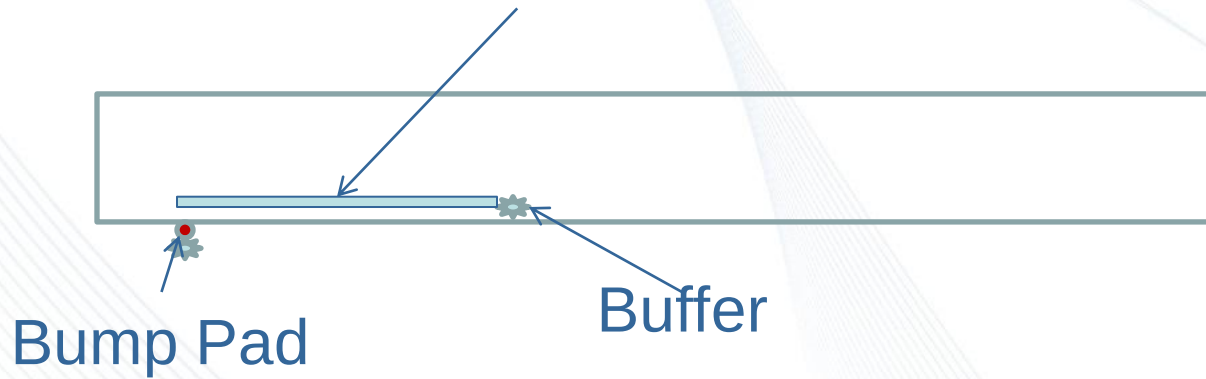
)

Connector EMD Parameter Tree

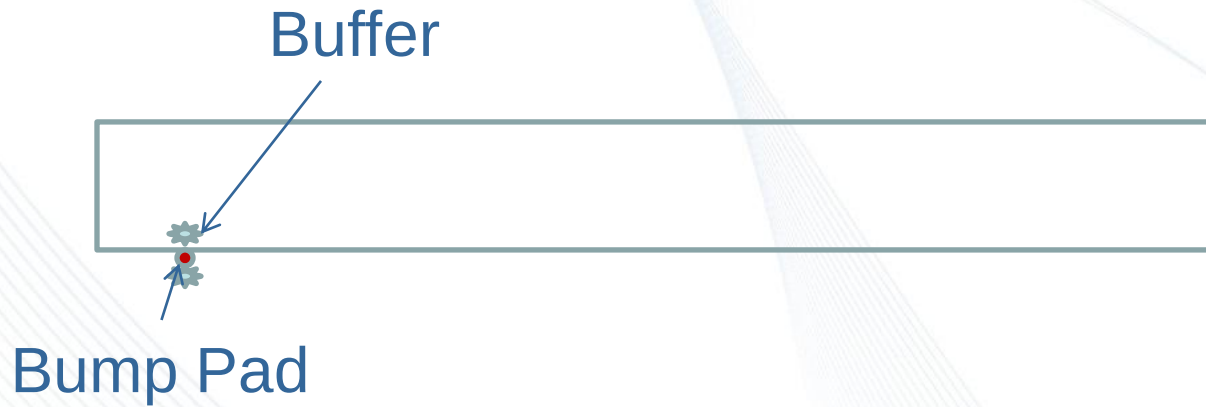
```
(Connector (IBIS_Ver 6.0) (File_name Connector.emd)
  (Module Connector (Number_Of_Pins 4)
    (Pin_List (A.A1 A1) (A.A2 A2) (B.A1 A1) (B.A2
      (Extended_Nets (A1 A.A1 B.A1) (A2 A.A2 B.A2))
      (Package
        (Full
          (Tstonefile
            Corner(typ.s4p min.s4p max.s4p))
          (Model_Ports
            (1 (Pin_name A.A1))
            (2 (Pin_name B.A1))
            (3 (Pin_name A.A2))
            (4 (Pin_name B.A2))
          )
        )
      )
    )
  )
)
```

On-Die Models

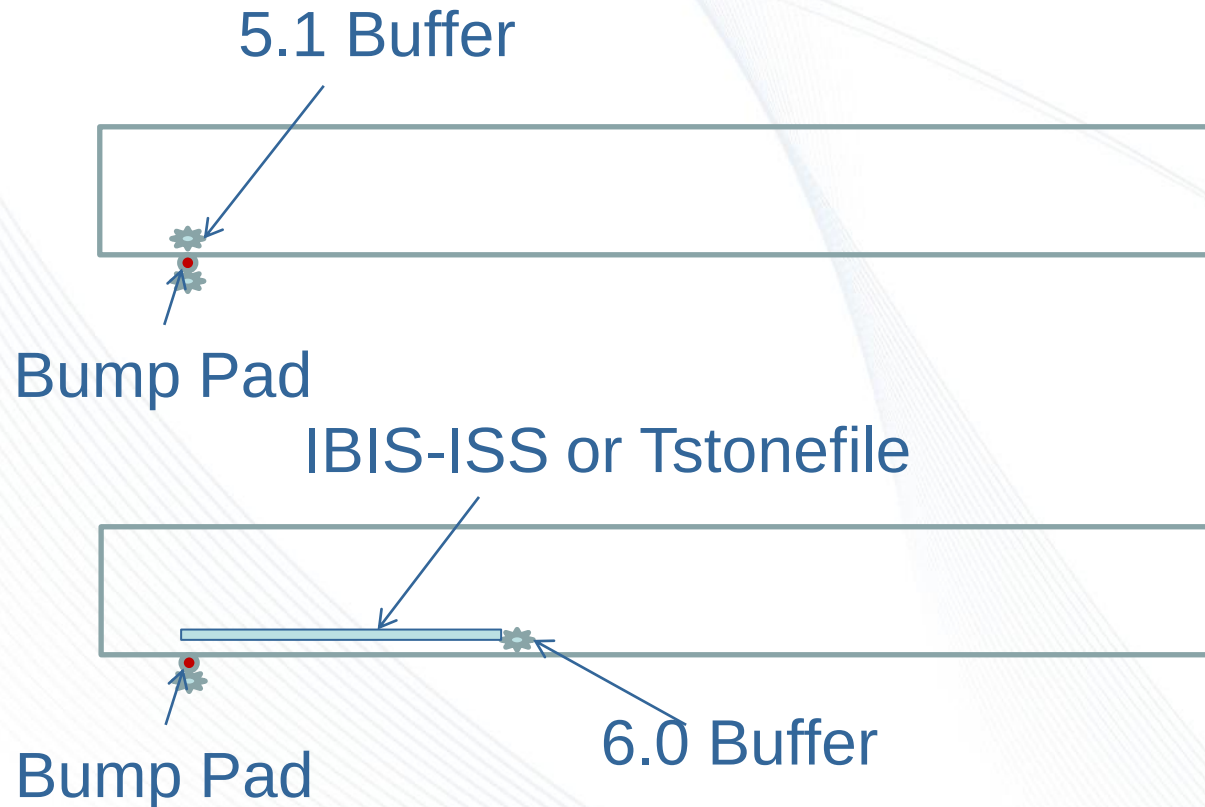
On-Die Interconnect (RDL or T-coil)



IBIS 5.1 Limitation



The IC Vendor Needs to Partition the 5.1 Buffer into a IBIS-ISS or Tstonefile On-Die Interconnect and a Different 6.0 Buffer



For Non AMI Modeling

- The IC Vendor will most likely partition the On-Die Interconnect and Buffer at a point where he can use a Legacy IBIS [Model] and a Tstonefile for the On-Die Interconnect
- The Legacy IBIS [Model] has no constraints
 - C_comp will be smaller because it does not include the capacitance in the On-Die Interconnect
 - IV curves will be different because they do on include the resistance in the On-Die Interconnect

For AMI Modeling ...

- The current trend is for IC Vendors to combine the on-die interconnect and buffer reactive load into a single s4p. This is not currently supported by IBIS, but is supported by a number of EDA tools through non-standard interfaces.

Conclusion

- There are proposals being discussed that address the following interconnect modeling requirements
 - Packages
 - Multichip Modules
 - Connectors
 - Interposers
 - Sockets
 - Cables
 - On-Die Interconnect
- There are proposals being discussed that address broadband AMI analog model requirements
- The devil is in the details