

# ***IBIS Modeling Experiences***

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## ***Modeling LVDS***

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- **Different methods available**
  - IBIS Modeling of LVDS Buffers, Hazem Hegazy and Mohammed Korany, Mentor Graphics
- **Not every method works for every LVDS device**
  - Different output structures
  - Use method that best works for your circuit topology



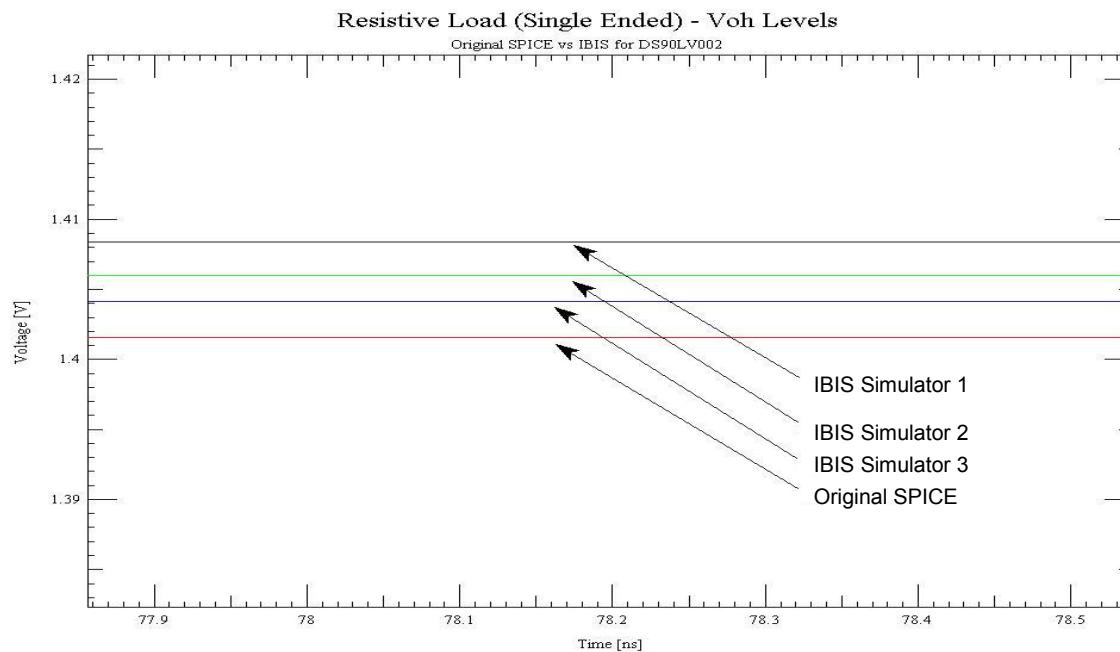
## ***IBIS Simulators***

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- **Different simulators can give different results**
  - Each simulator uses it's own algorithm to process IBIS files
- **Some things supported in one tool, while not in another**
  - Internal termination



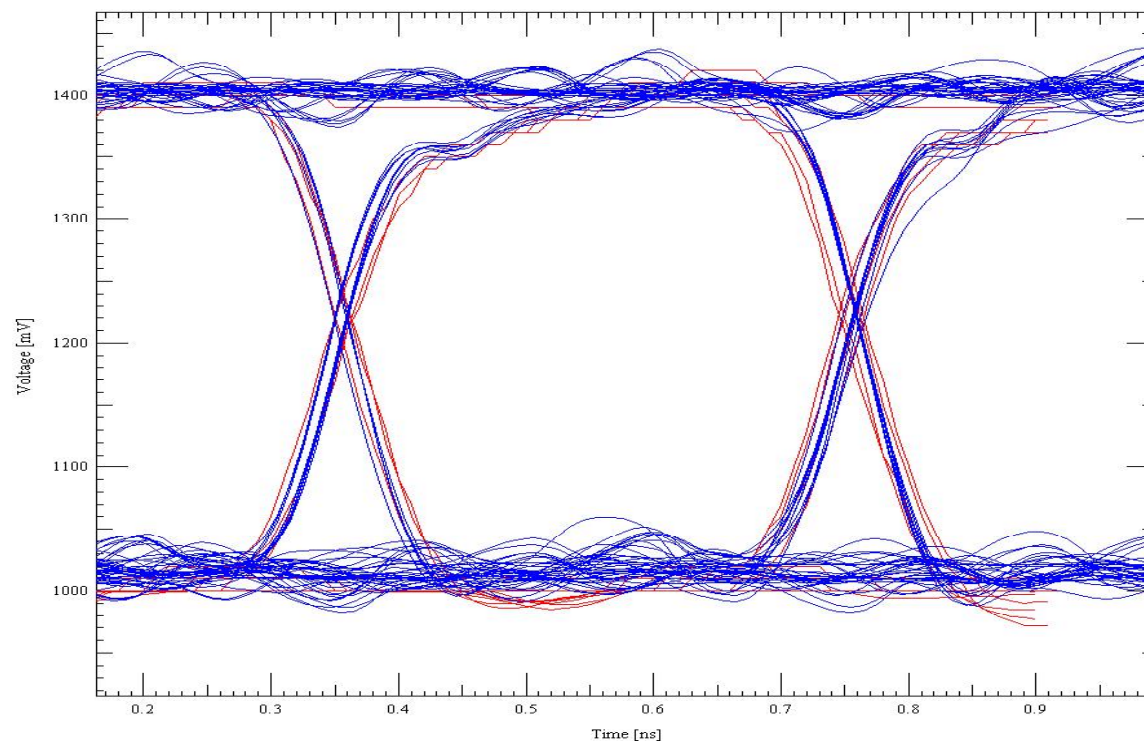
# Differences Between Simulators





## **IBIS @ 2.5 Gbps**

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## ***Some Issues of the Model Maker***

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- **Model works in one tool, but not in another one**
- **The “feared” AC and DC mismatch warning**
- **Simulation does not look the same as bench measurement**



## ***Packaging***

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- **Lumped RLC at 2.5 Gbps?**
- **IBIS supports advance packaging**
  - Can include full RLC matrix w/coupling
- **Most IBIS simulators don't support advance packaging**
  - Often have to create separate package model specific to simulation tool



## ***Accuracy***

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- **Working on providing Accuracy Report for every new IBIS file created**
  - Most model makers validate model before releasing, need to document and distribute
  - Base on old Accuracy Specification and new Quality Group work
- **How do you validate a model that will be used in multiple tools?**
  - Pick a metric and go with it
  - Goal of 90%, shoot for 95%





## **VHDL-AMS**

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- **Is VHDL-AMS the future of IBIS?**
- **Recently passed Bird will include use of external VHDL-AMS models**
- **VHDL-AMS superset of VHDL that allows advanced behavioral modeling**
  - **Ex. Use equations to describe buffer**



## ***National Semiconductor Modeling Resource Webpage***

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- **Coming Soon!**
- **New webpage dedicated to IBIS and modeling issues**
  - [www.national.com/appinfo/lvds/ibis\\_home](http://www.national.com/appinfo/lvds/ibis_home)