Report on EIAJ IMIC Standard

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IBIS Summit

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Electronic Industries Association of Japan (EIAJ)
Technical Standardization Committee on Semiconductor Devices
I/O Interface Model Project Group
Technical Standardization Committee on Semiconductor Packages
Electrical Characterization of Semiconductor Packages Project Group

IMIC Progress

1. Three evaluations

2. Advanced Package Modeling

3. EMI Model Standard

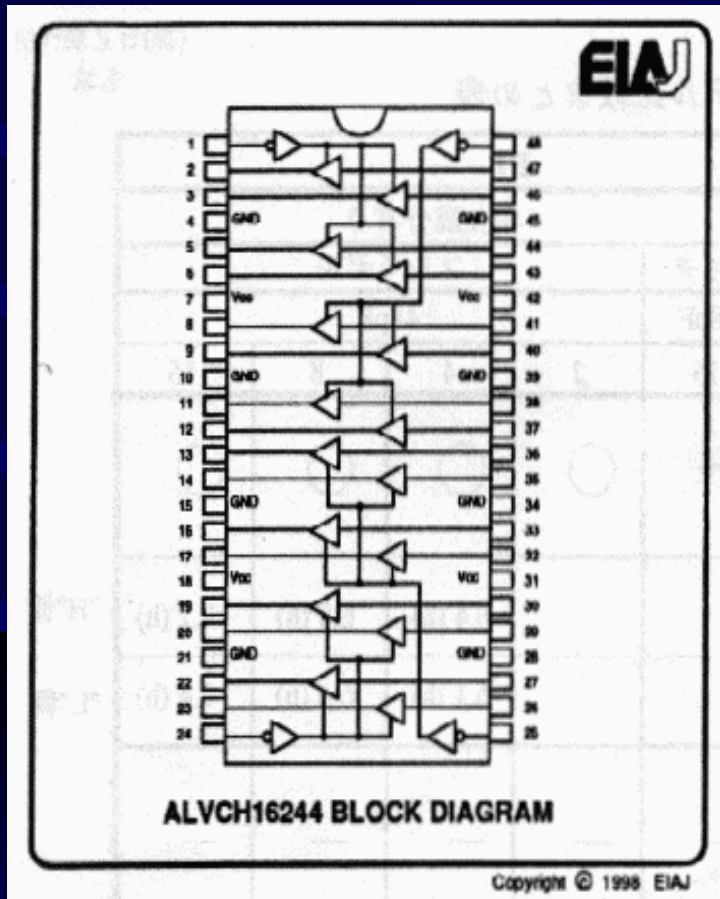4. New Activities

1. Three Evaluations

Three Evaluations

ALVCH16244 (Hitachi)

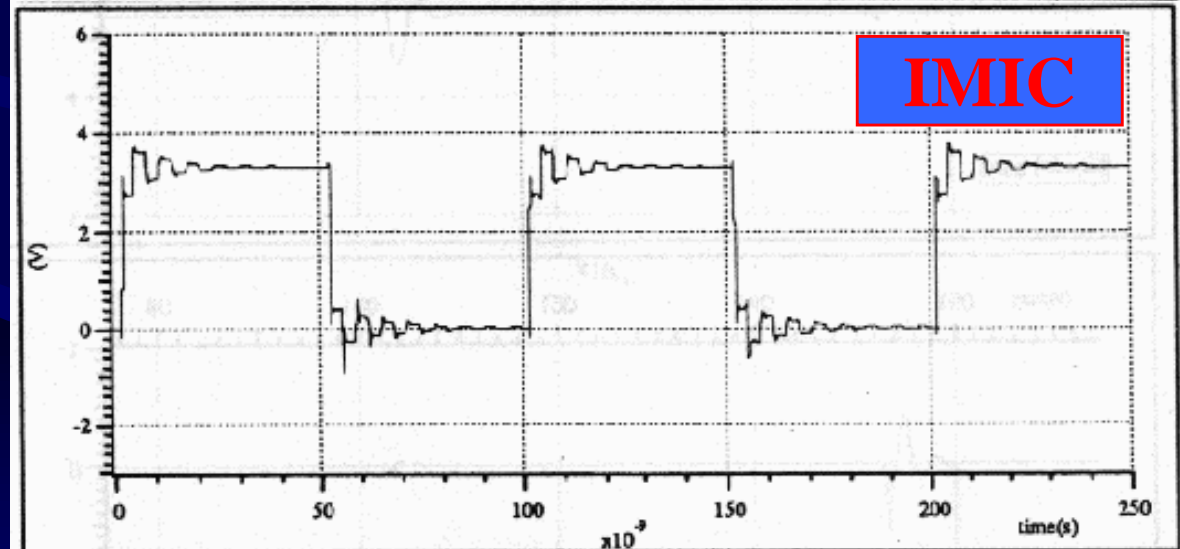74LCX245 (Motorola)
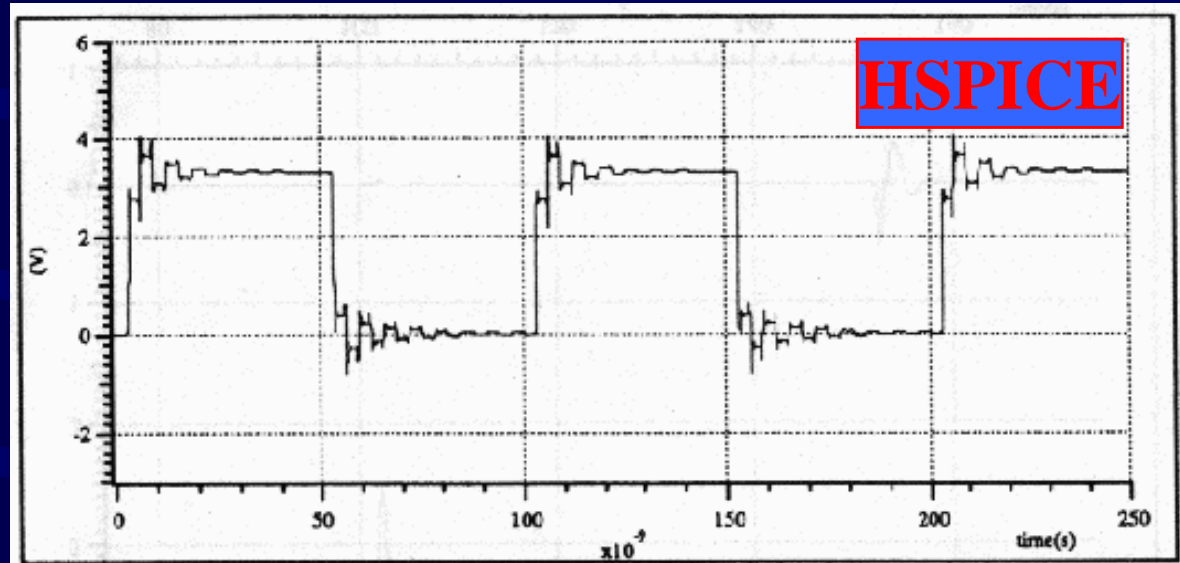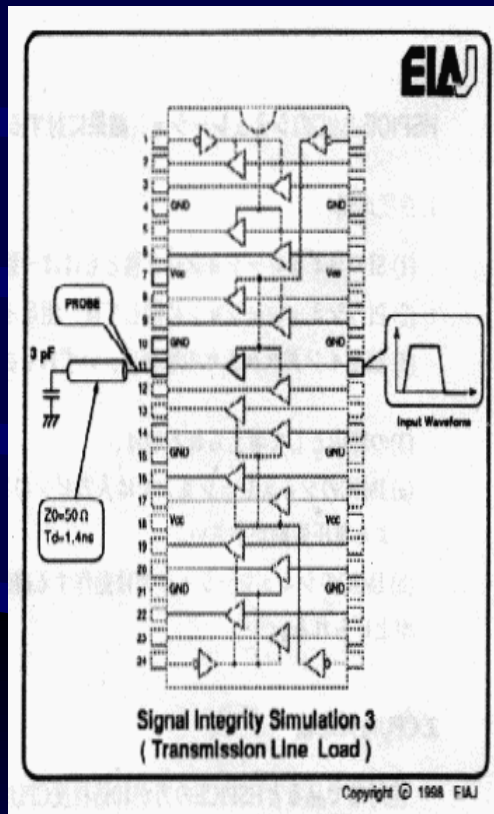
16233.cbt (TI)

1.1 Accuracy

ALVCH16244

ALVCH16244 BLOCK DIAGRAM

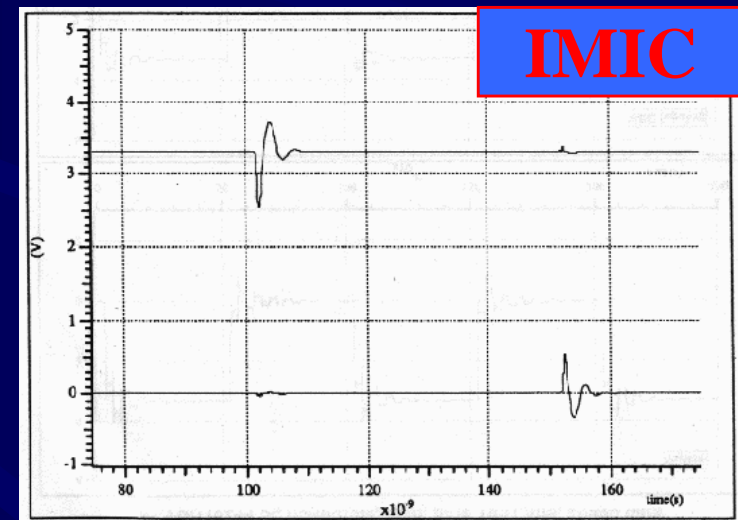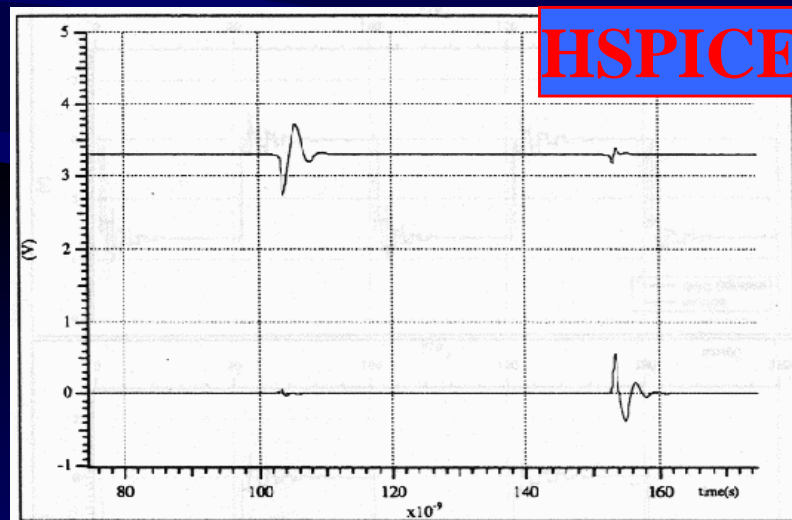**Transistor Level Model**
+
Package Model

HSPICE (Full Transistor Model)

IMIC (Pre-stage plus I/O Buffer)
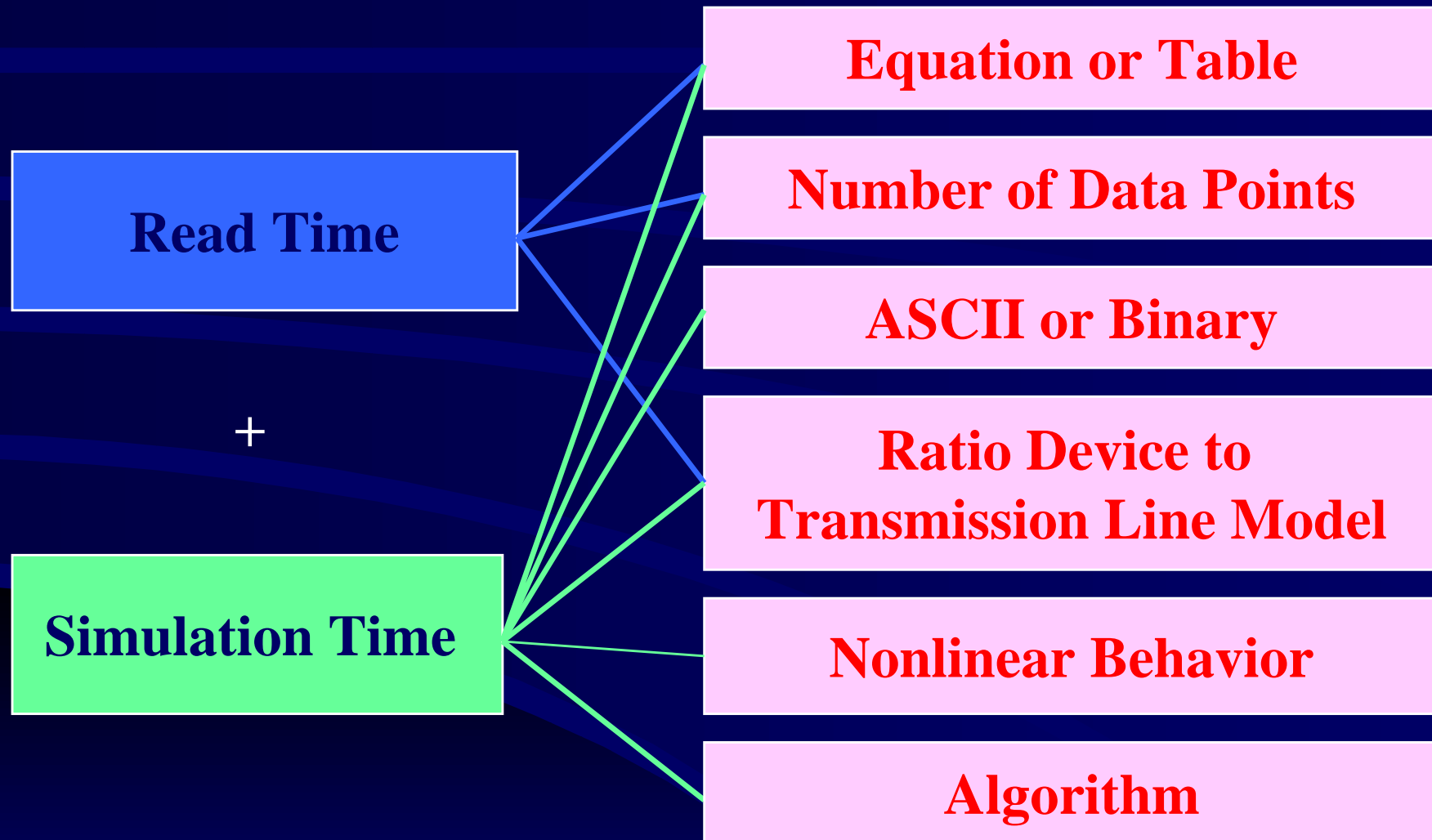
Reflection by Transmission Line

HSPICE

IMIC

Signal Integrity Simulation 3
(Transmission Line Load)

15 Simultaneous Switching Noise

Power Integrity Simulation 4
(15 buffers switching noise)

Measurement

15入力変化

HSPICE

IMIC

1.2 Speed

Speed

Read Time

+

Simulation Time

- Equation or Table
- Number of Data Points
- ASCII or Binary
- Ratio Device to Transmission Line Model
- Nonlinear Behavior
- Algorithm
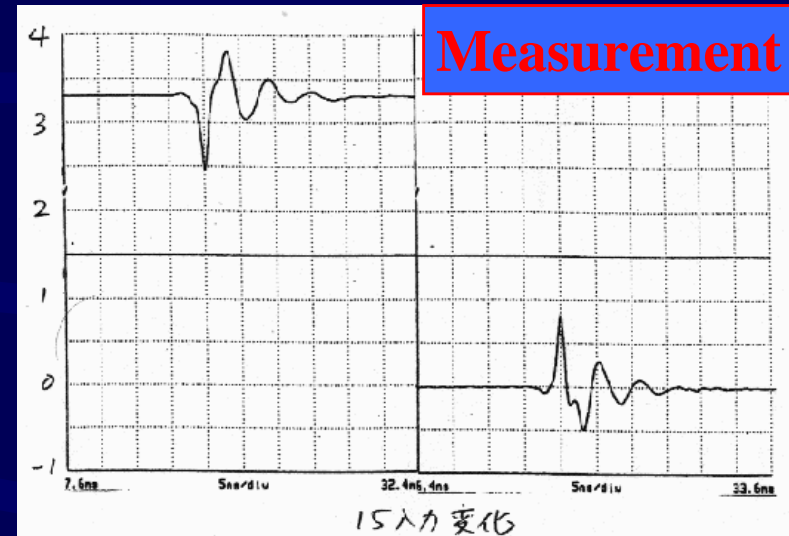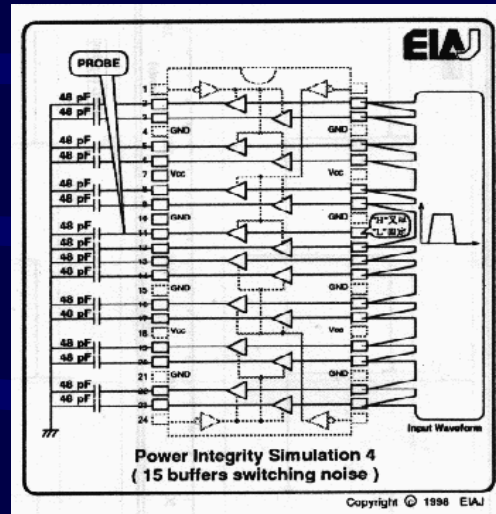
Ratio of Device to Transmission

to be reduced

Equation

Table (IMIC)

Total CPU Time

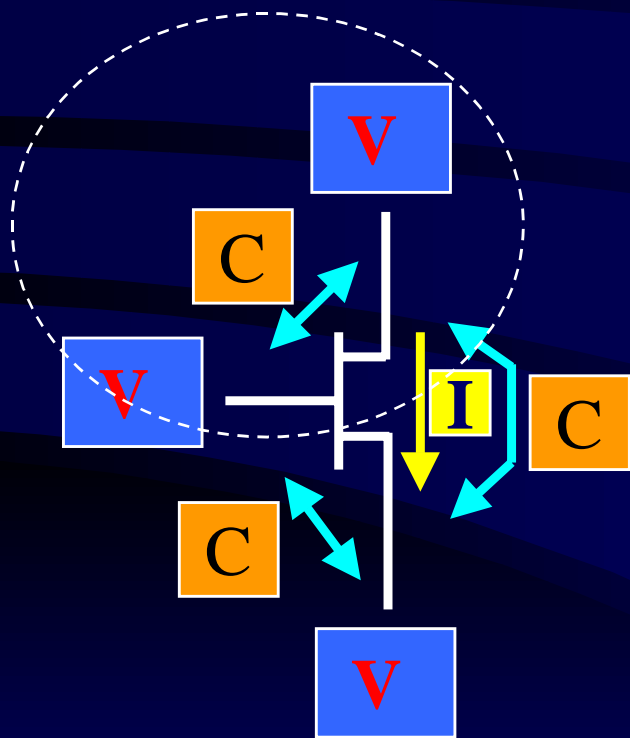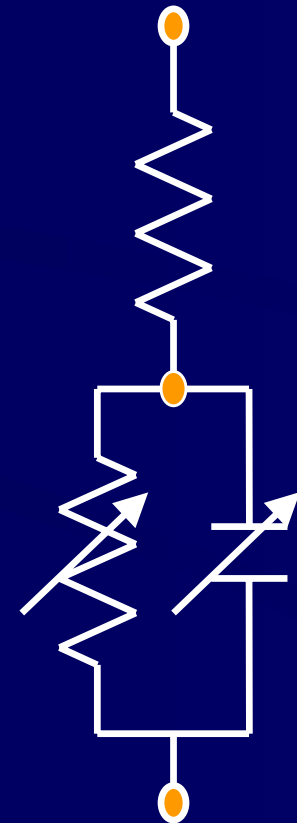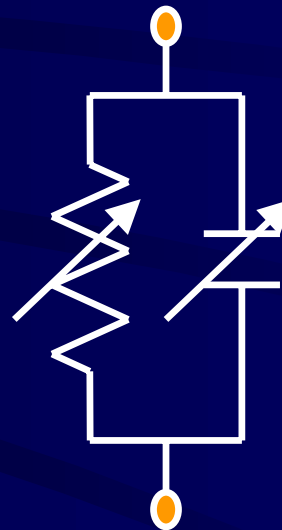Transmission Lines / Devices in a Net
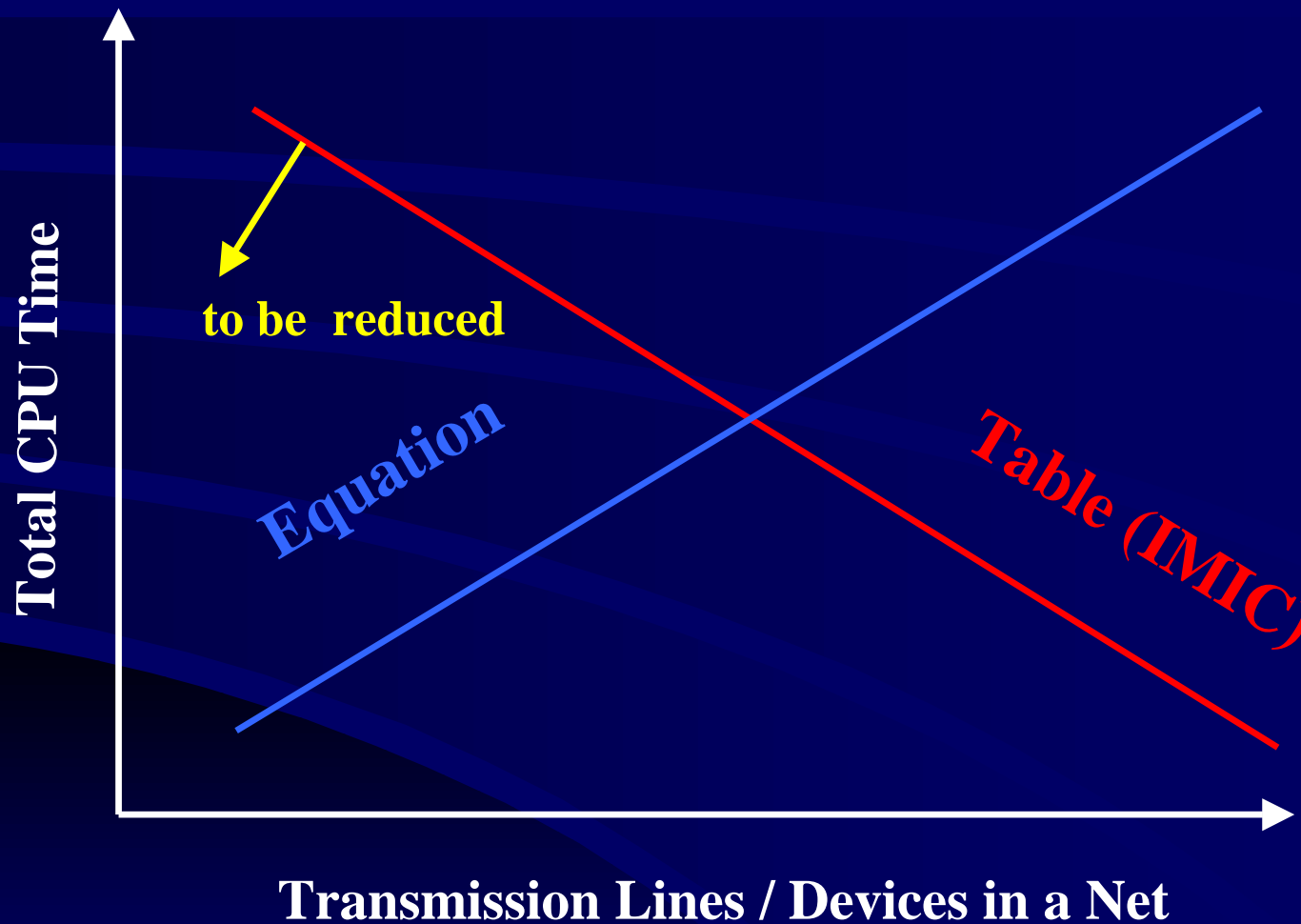
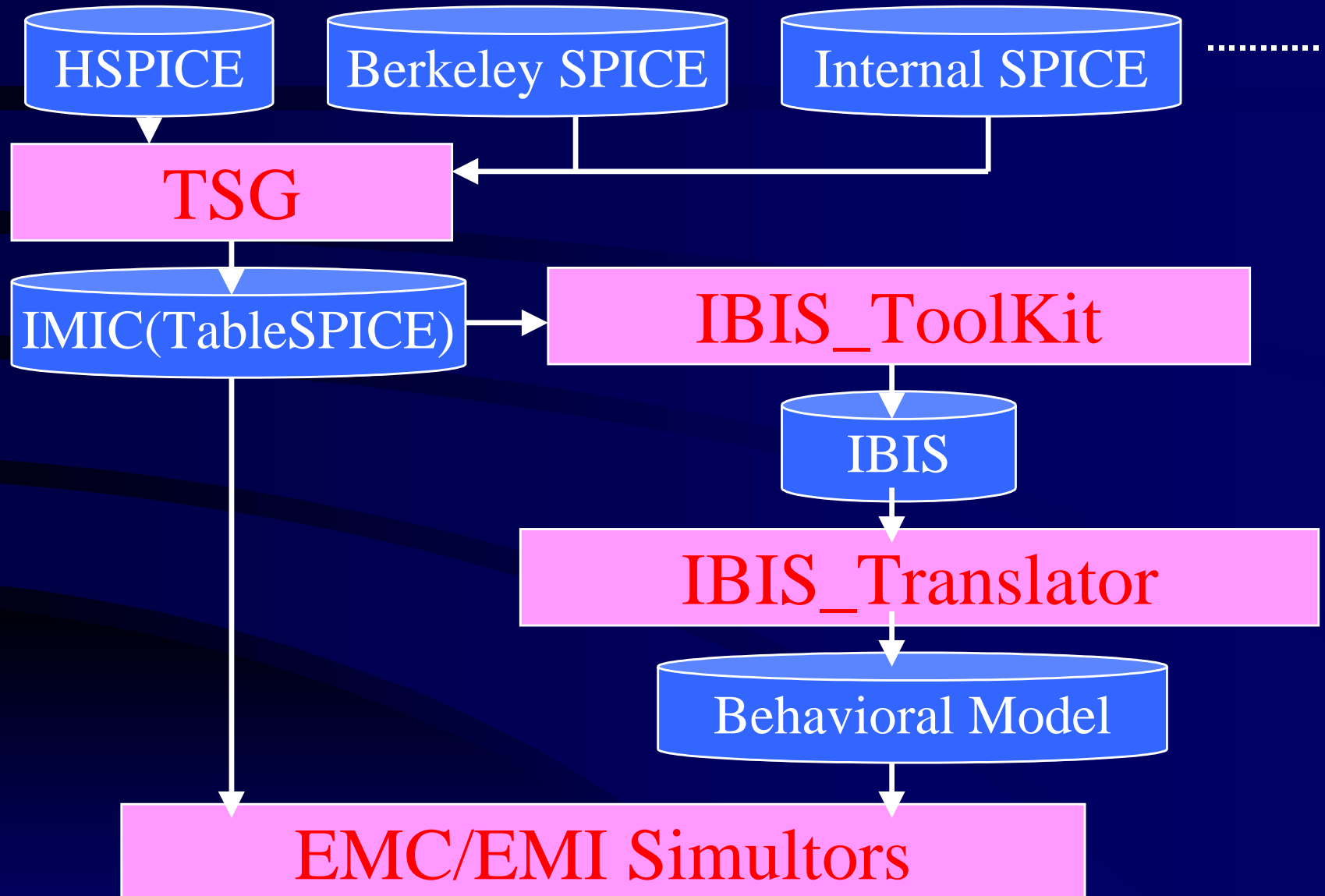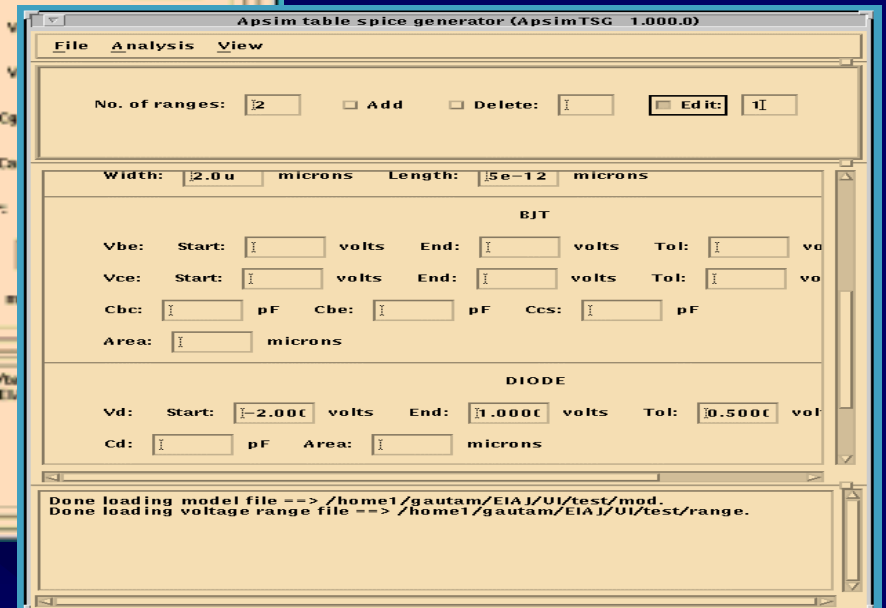# 1.3 Enhancement of Specifications
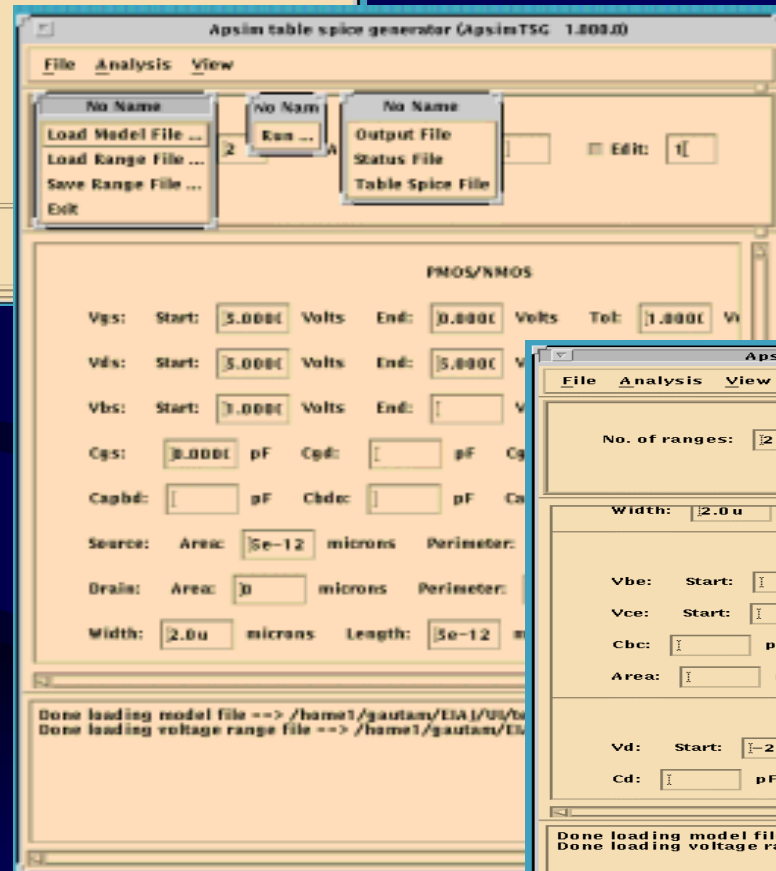
Major Changes

V-V-V-I-C-C-C
Multi-dimensional Tables

1.4 IMIC Tools

SPICE Conversion

Table_SPICE Generator
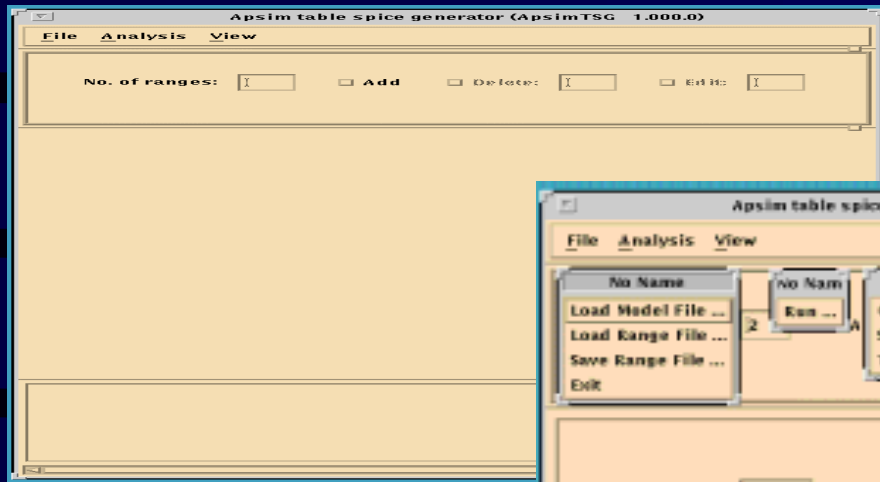
Table_SPICE to IBIS
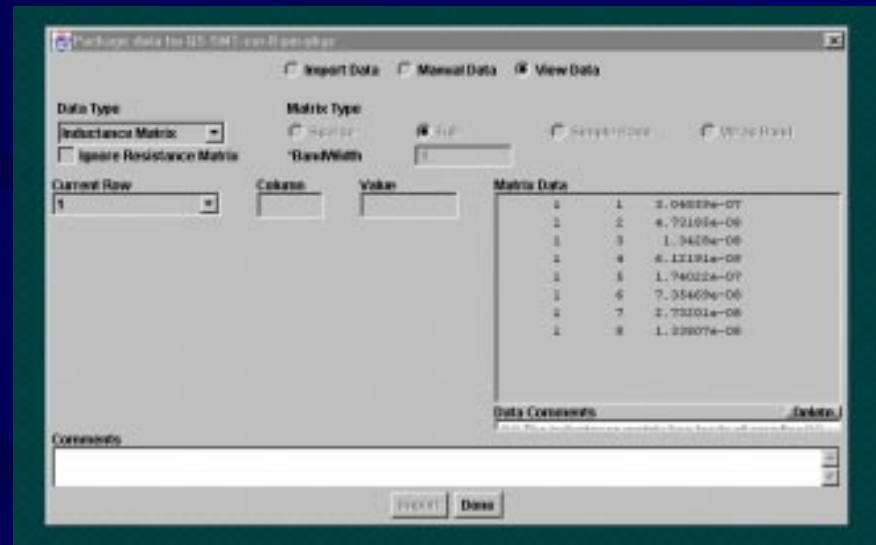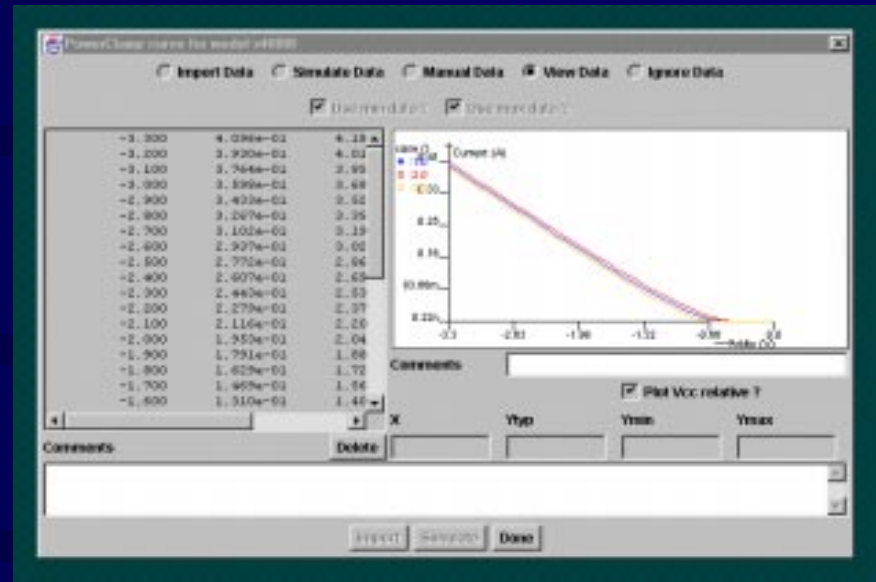
Package Modeler for Signals and BGA Ground for beyond 2,000 Pins
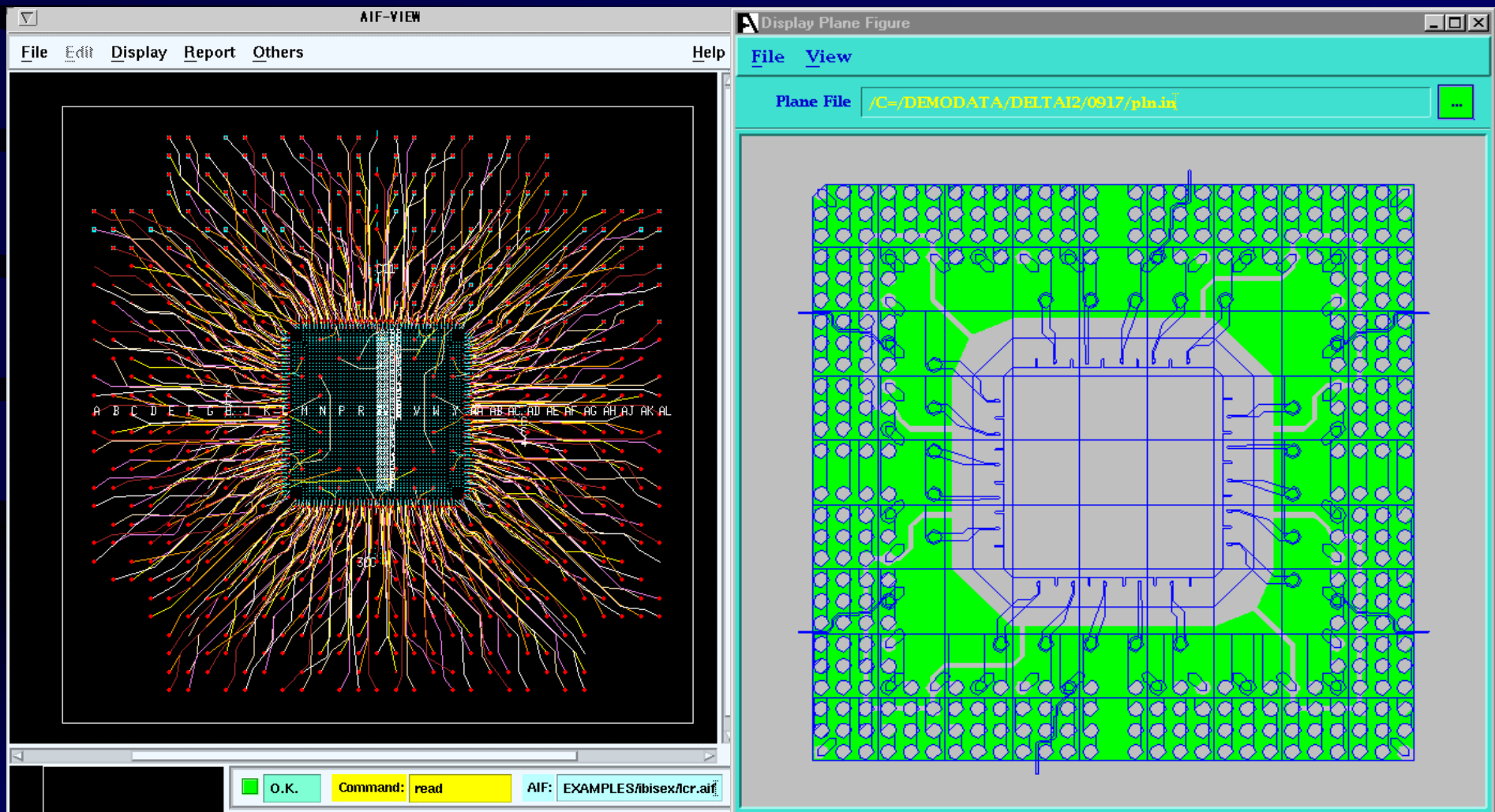
2. Advanced Package Modeling

Adding New Examples for IMIC

More QFP

New IC Package Model Examples

BGA

CSP
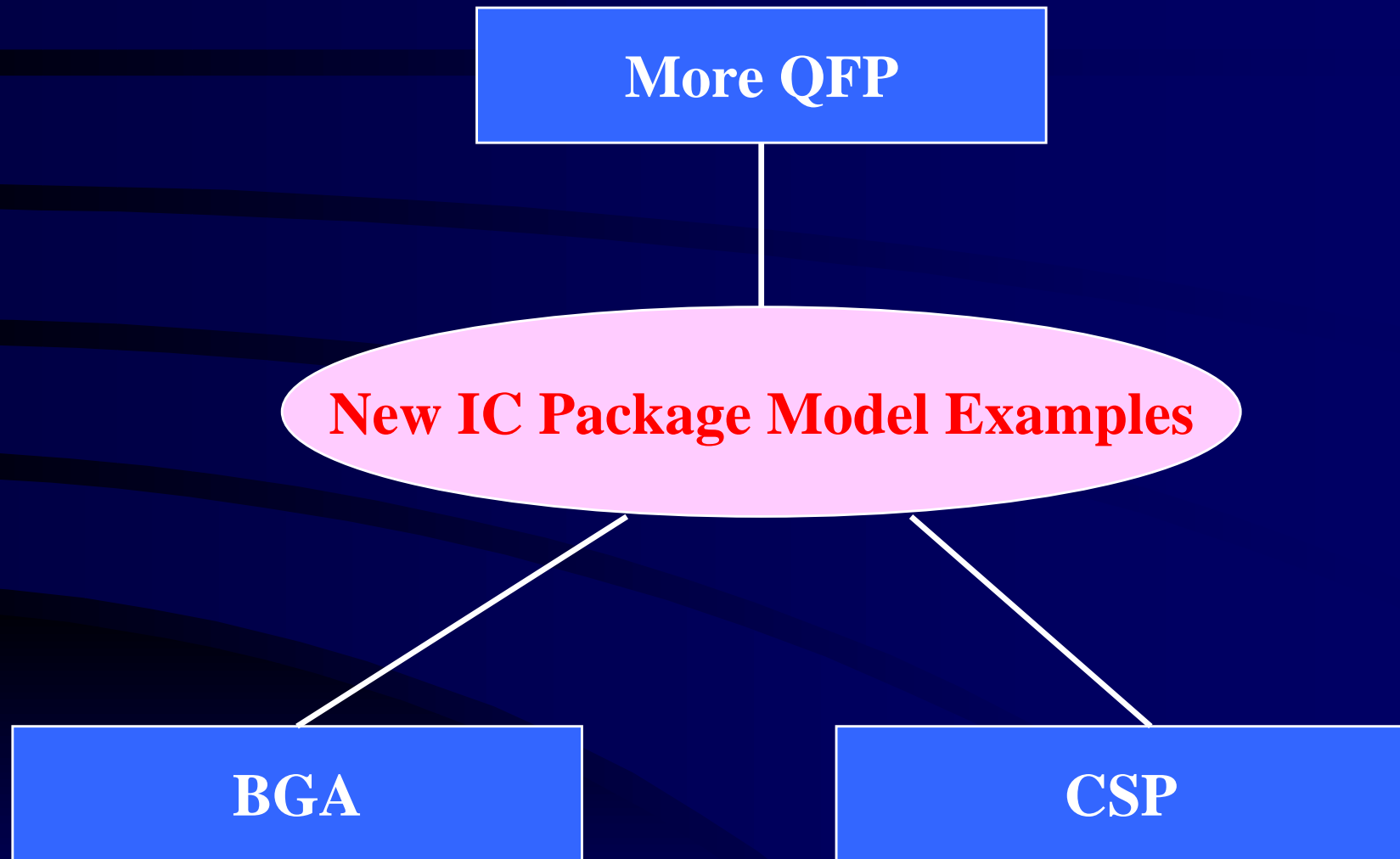
Package / Module needs Free Network Descriptions

Coupling Effect

IC Package / Module Model needs

Fork & Loop

Frequency Dependency
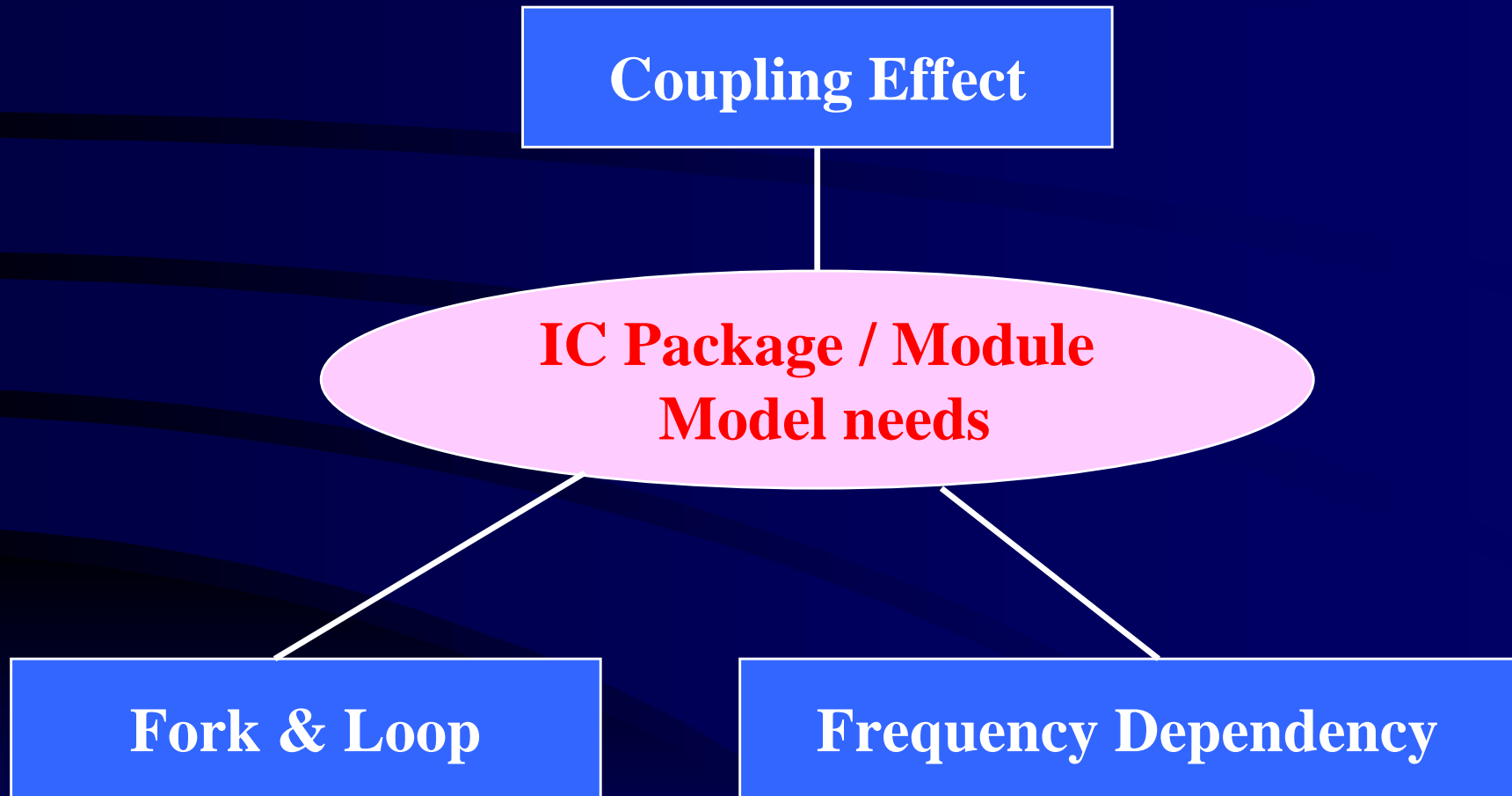
3. EMI Model Standard

Return Current Path (Common Mode EMI)

No capacitor
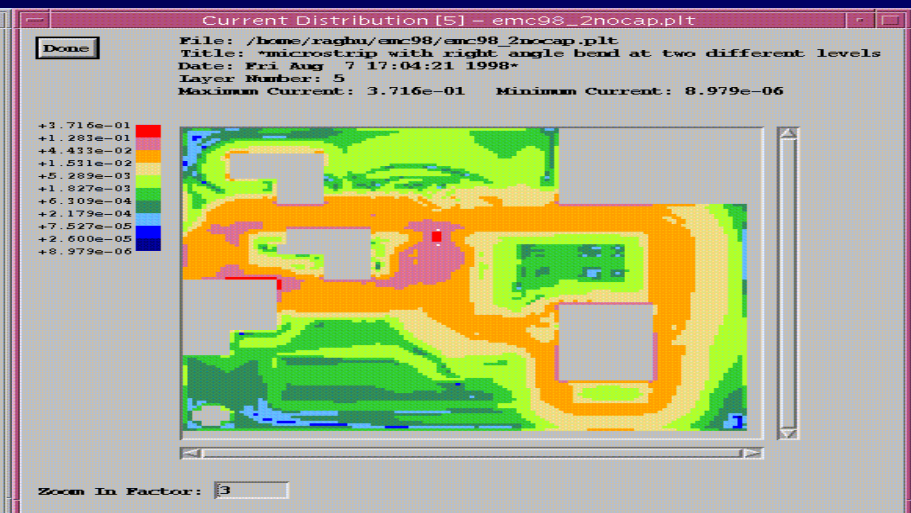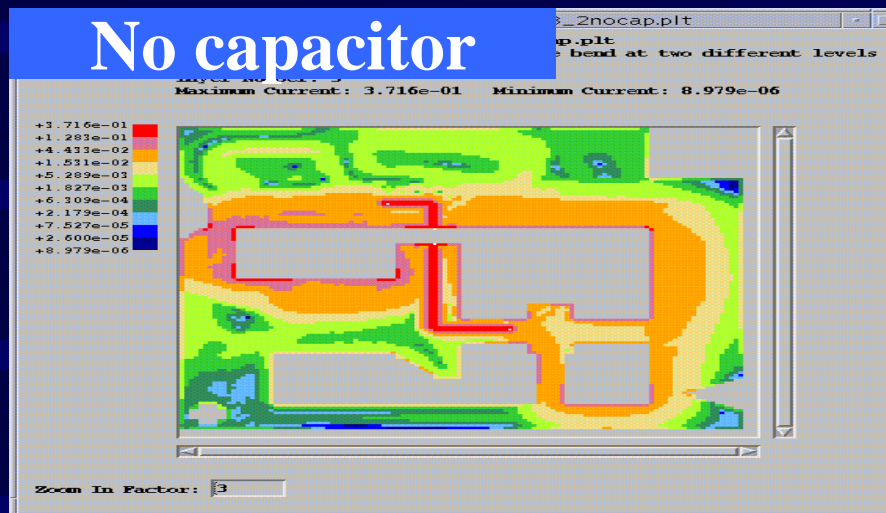
With capacitors
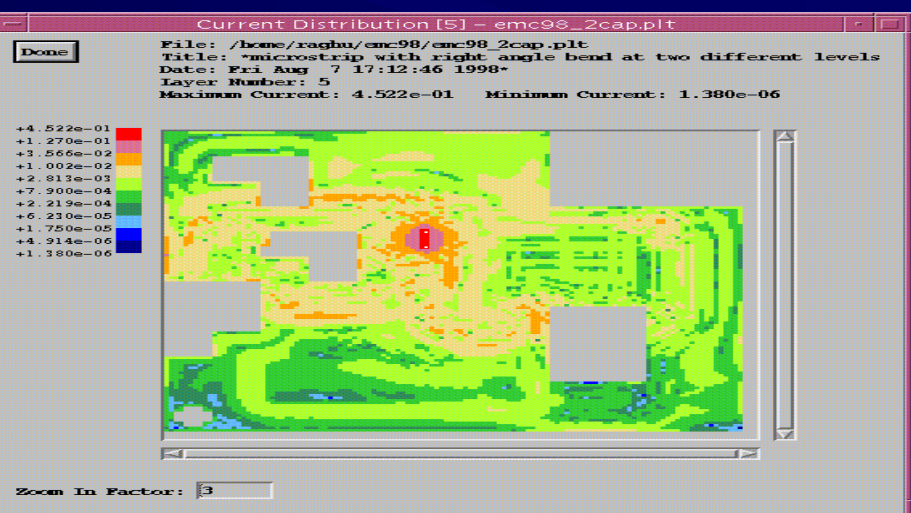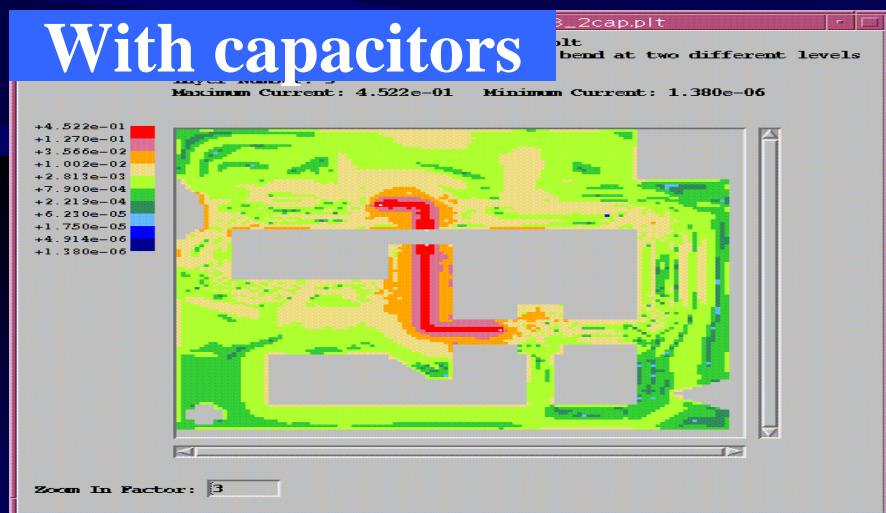
Local Ground Reduces IC EMI

Required IC & IC Package Physical Dimensions /Interconnects

Local Ground

PCB

Required Information

Package Structure

EMI

Power/Ground for
I/O & internal gates

PI

I/O Buffer

Package

SI
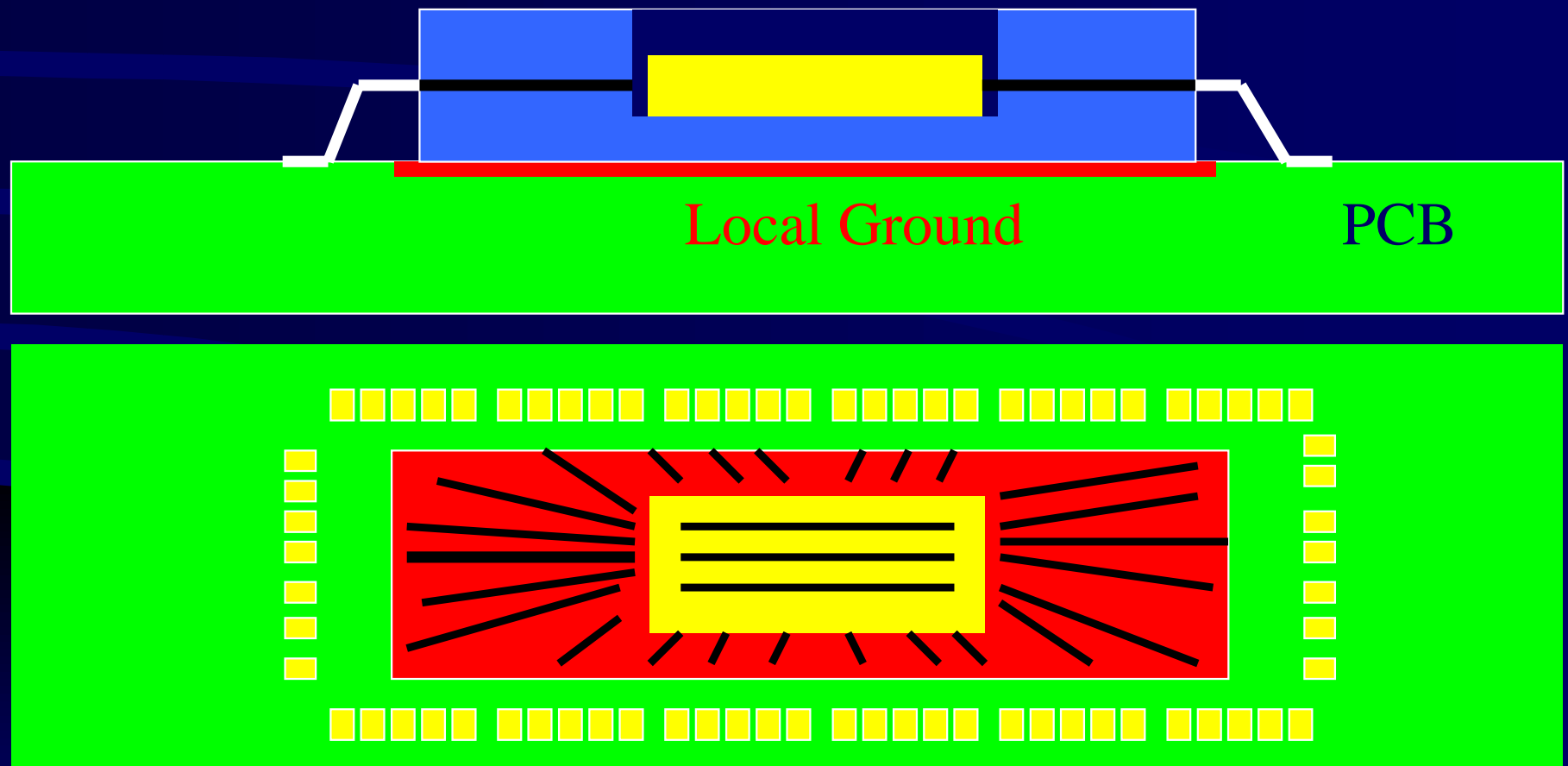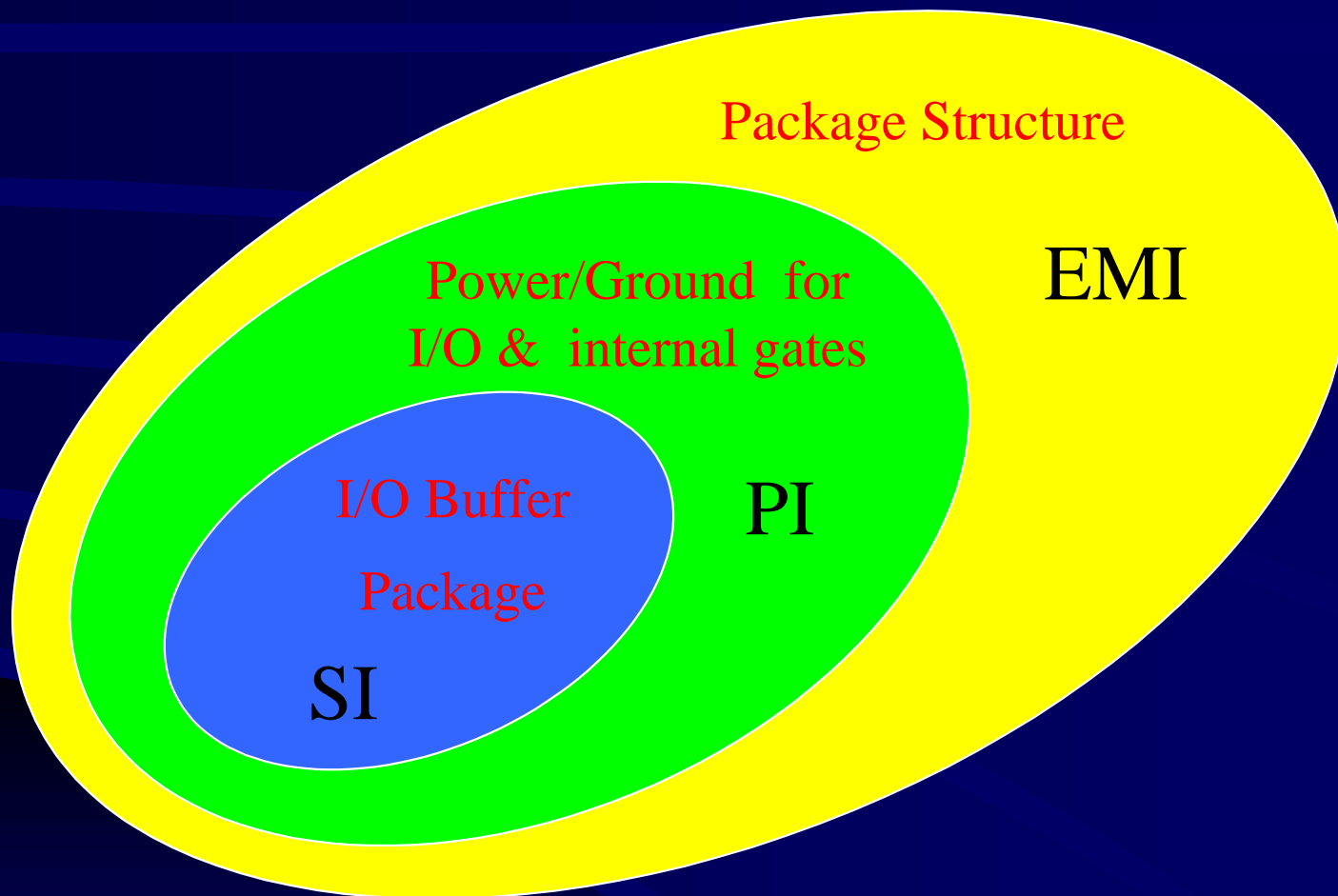
EMI Simulation needs Power/Internal Info

Regulator

Various Clock Frequency & Events
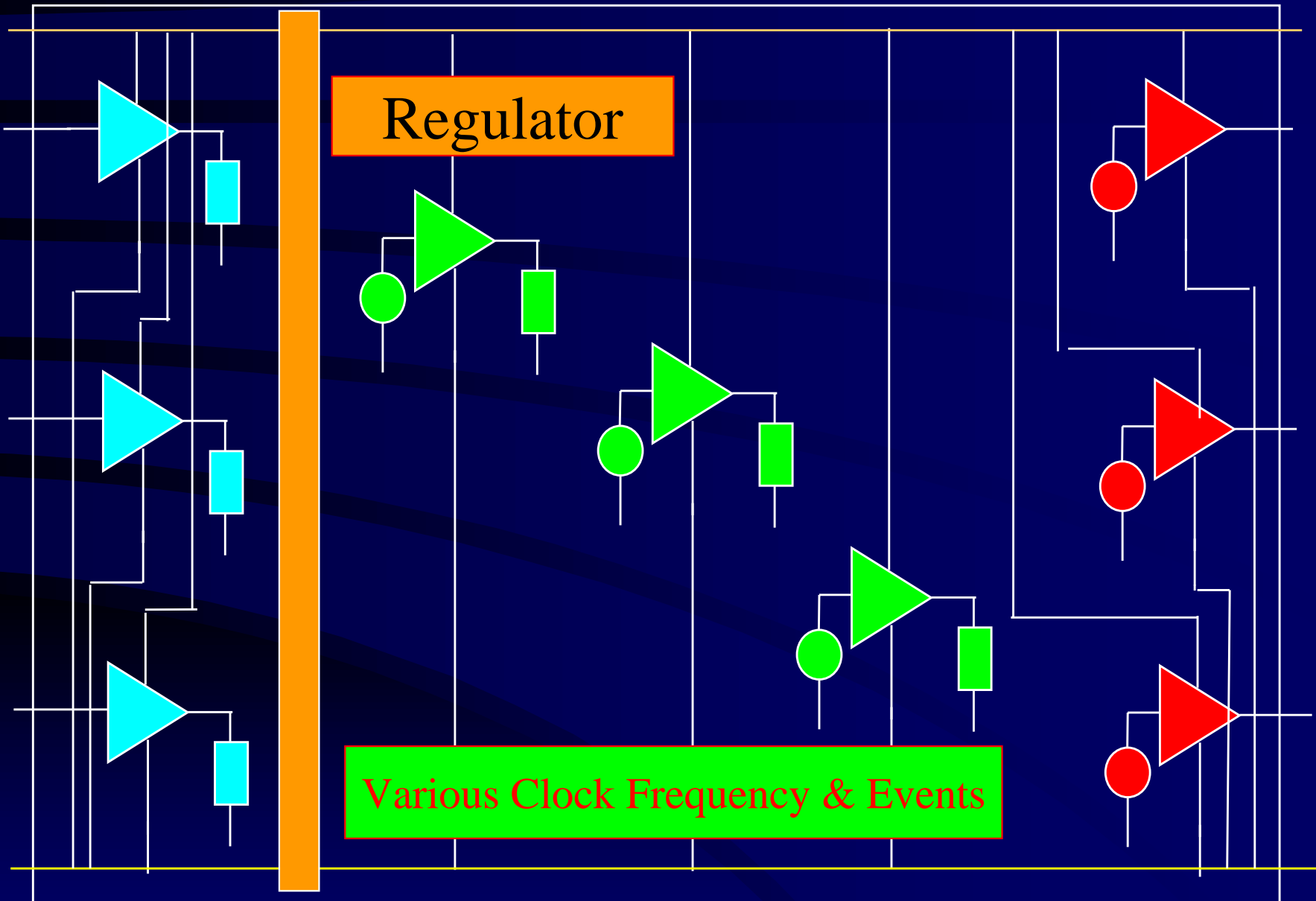
IC Internal Gate vs I/O Buffer For EMI

Internal Gates sometimes

    Much Faster

    More Power Consumption

      than Output Buffers.

Mixed Mode IC contains

    Op-Apm inside

    Output Power FETs for direct drive

      than Output Buffers.

IC Internal Gate Macro EMI Model with Various Clocks and Events
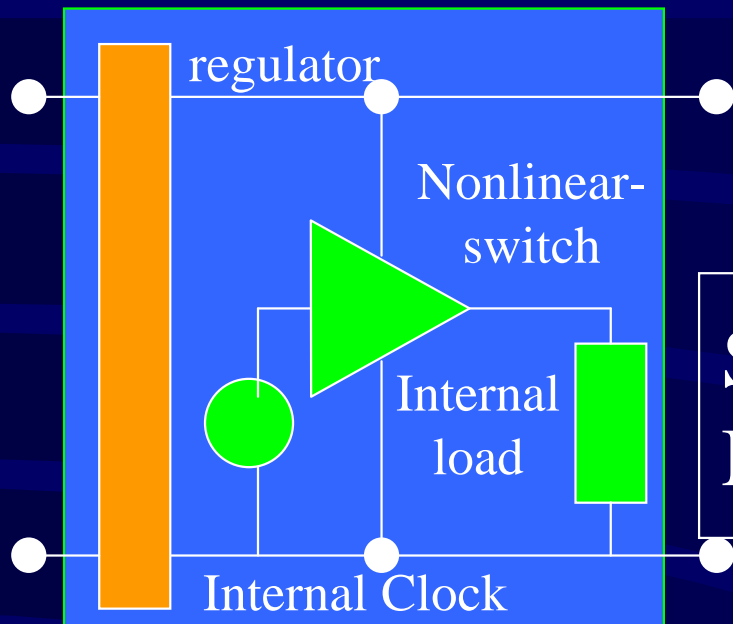
Described in IMIC

Regulator Model

Simplest :Ideal DC Power Sources
More Accurate : Loading Effect

Internal Gate Macro Model

Current or Voltage Waveforms plus Output Impedance

Macro EMI Model = Power/GND Model

IC

PCB

I/O Buffer

Package

Internal gate group
with various
Clock Frequencies

Regulator

=

Driver
/Receiver

Connectors

Various Clock
Frequency group,
Mixed Mde

Regulator
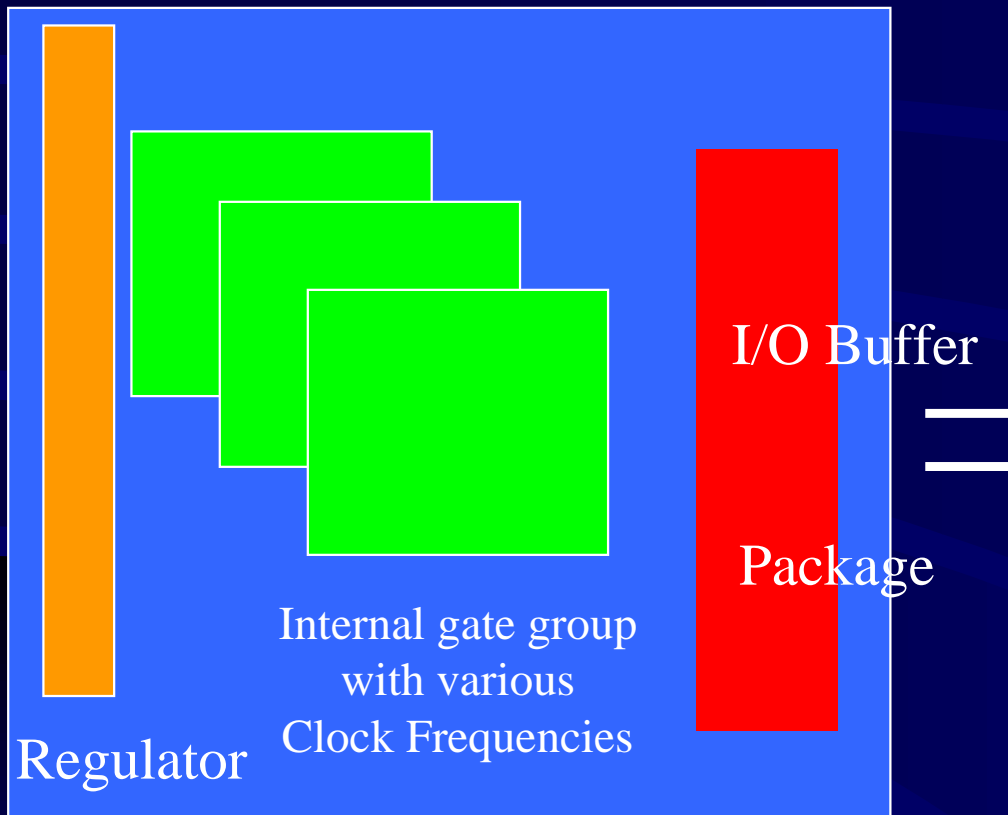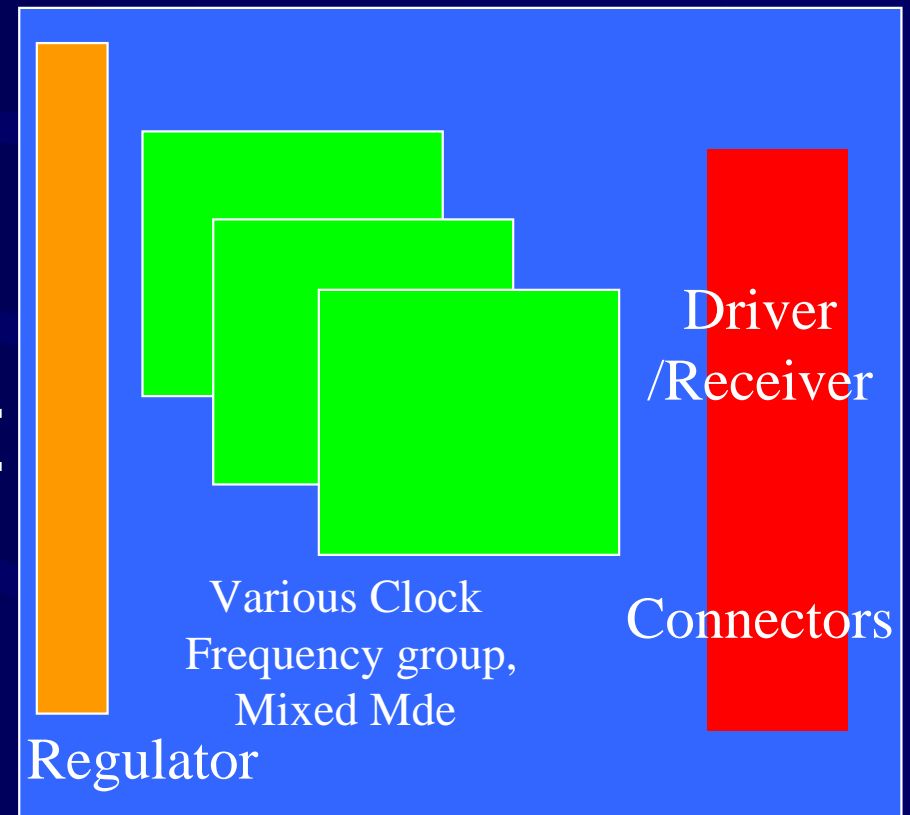
EMI Filter & Decoupling Capacitor Modeling

Current

Frequency Dependent Impedance on Data Sheet

S-Parameters on CD

Very few SPICE RLCK Models

Future

RLCK Network or Polynomial Dependent Sources

4. New Activities

Target of EIAJ/IMIC

EMI

Power Integrity

Signal Integrity
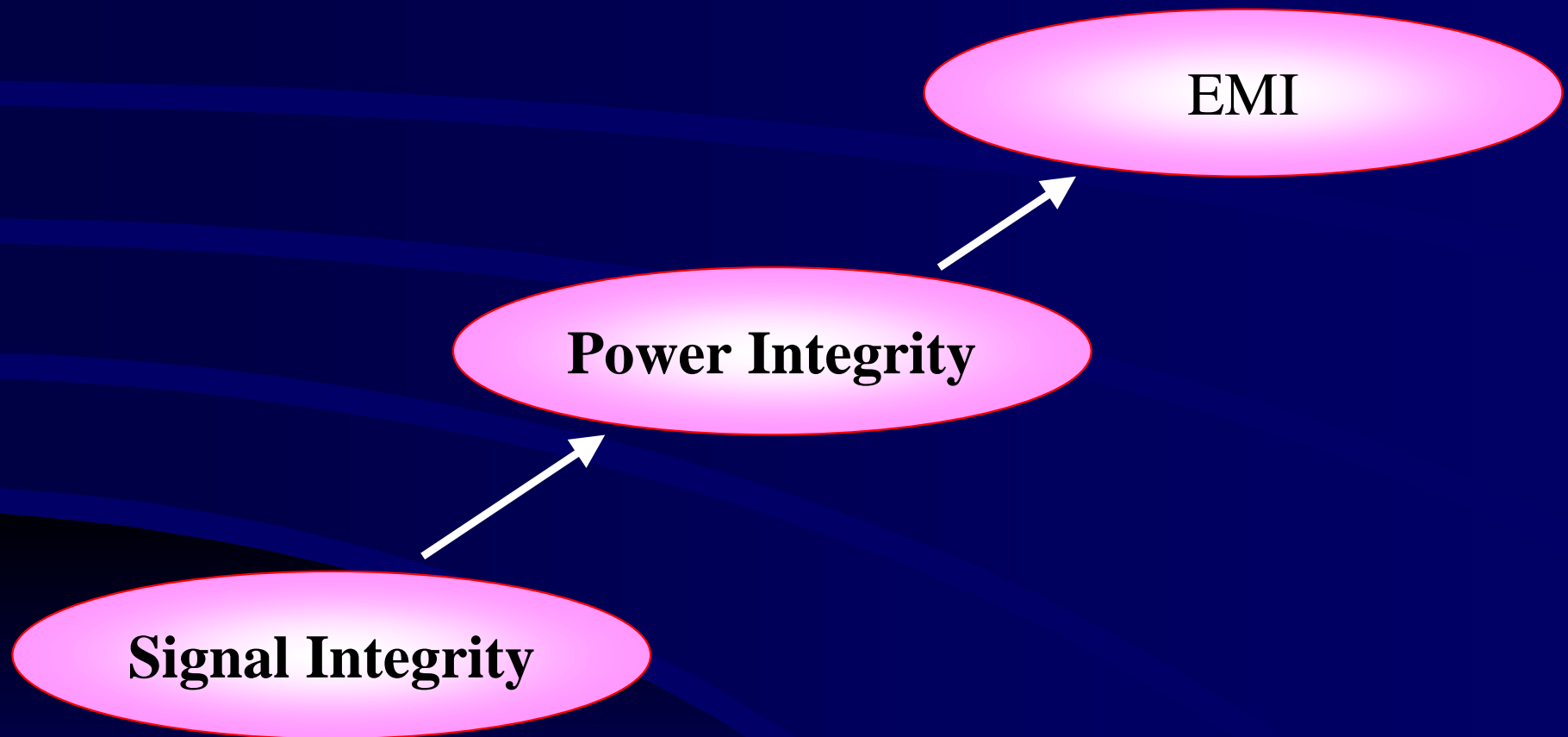
Strategy of EIAJ/IMIC

IMIC uses Table Format SPICE Syntax.

IMIC expects users to extract partial data from the "IMIC Data" depending on required accuracy and speed.

IMIC does not force EDA tool vendors to use SPICE algorithm.

One simulator vendor has released IMIC-based tools.
At least one more simulator vendor will release.

IBIS & IMIC

IBIS (EIA) → IEC ⟵ IMIC (EIAJ)

IBIS (EIA)
- IC I/O
- IC Package
- Ramping Resistor/Filter
- Accuracy WG
- Connector WG
- IBIS&IMIC Linkage/Merger SG

IMIC (EIAJ)
- IC I/O
- IC Package

Non-IC & System Level
- IBIS&IMIC Merger SG
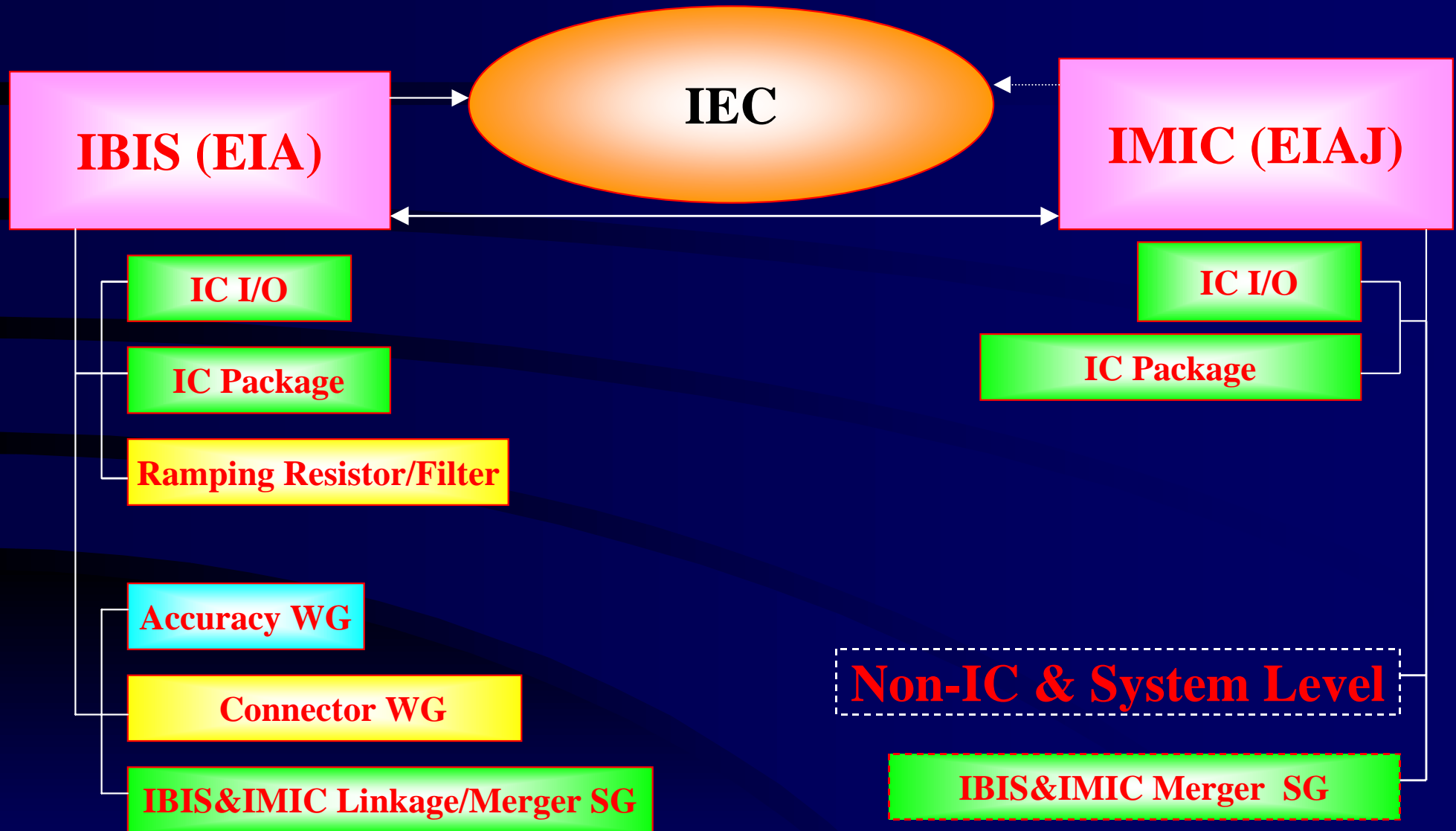
To be considered by IBIS & IMIC

	IBIS	IMIC
IC I/O	Fixed Model	Arbitrary SPICE
Accuracy	Low	High
Speed	Fast	Slow
Proprietary	OK	OK
Target	SI, System	SI,PI,EMI
Timing Info.	Yes	No
System Design	Yes	No
Follow Tech Change	Slow	Fast
Package	Weak	Strong
Non-ICs	Passive/Connect	No

Another Activity Coming Soon

Another committee on EMI/EMC modeling for Non-ICs (Discrete Components) and System Level will be formed very soon.

Component makers and end-system makers will jointly work to look at IBIS and IMIC for EMI simulation.

Components: Connectors, EMI Filters, Cables, Power Semiconductors, Crystal Oscillators.

System: Digital Consumer & Auto Mobile Electronics.

EIAJ I/O's Decision

1. No one likes two standards.

2. We prefer the "Sub-set":
   IMIC into IBIS or IBIS into IMIC

3. EIAJ I/O made a sub-working group on the IBIS and IMIC Merger.