SI-Analysis
with HSPICE based on IBIS Models

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Contents

- HSPICE behavioral model based on IBIS
  - Model features
  - Model structure
  - Load dependence of one- and two-waveform model types
- Correlation between simulation and measurements illustrated by signals on a PC motherboard system
  (Measurements: Mr. Schindlbeck, Siemens AG, Memory Product Division)
  - Block diagram/simulation model
  - Simulation and measurement results
- Conclusions

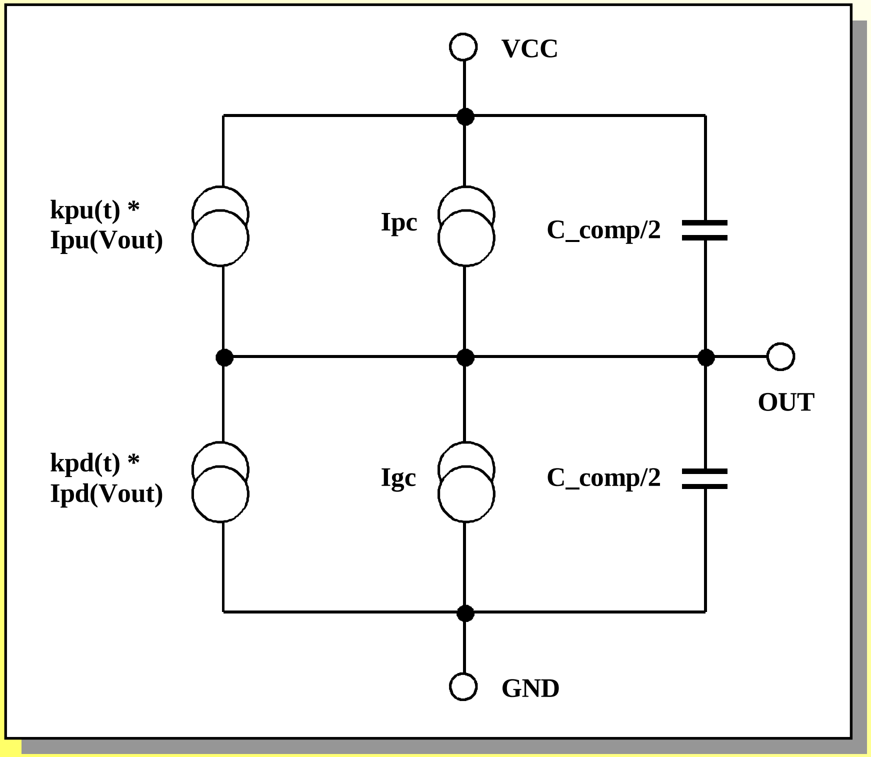
Model features

- Models are based on IBIS version 2.1/1.1
- Model types: “One- and two-waveform” models
- Parametrisized model:
  - Pulse width
  - Period
  - Delay
  - Initial state and output enable
- Scaling of driver strength
- Validity: TTL, CMOS and open sink and source drivers
- Model generation and quality checking is tool supported (UNIX shell scripts)
- Possible enhancements: ECL I/Os; input threshold/bit pattern driven models

Model Structure

- IBIS-conform model structure
  (see for instance: O.Rethmeier, “Modeling of integrated circuits to support SI-analysis”, 12th International Zurich Symposium and Technical Exhibition on Electromagnetic Compatibility, Zurich, February 1997)
  or: Bob Ross, email concerning ”IBIS TO SPICE DISCUSSION”, IBIS Open Forum, October 27, 1997)
- Voltage controlled current sources of polynominal type for pullup and pulldown current source control
- Voltage controlled voltage sources of polynominal type for timing control
- Parameter driven setting of initial conditions to overcome convergence problems
- Generation of multipliers kpu(t), kpd(t) by HSPICE runs

IBIS-conform output model



Model types:

- **One-waveform model**

  Vt-tables for only 1 load condition per edge available. Arbitrarily assumption of the multiplier relationships

  kpur/f(t) = 1- kpdr/f(t); function range: 0 to 1

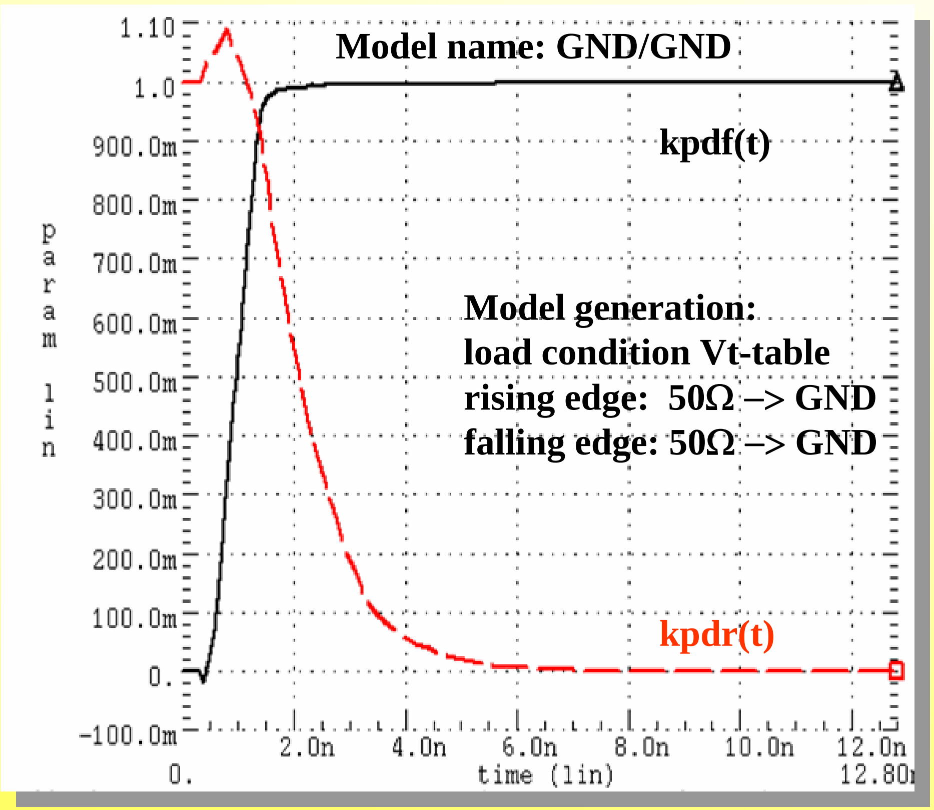
- **Two-waveform model**

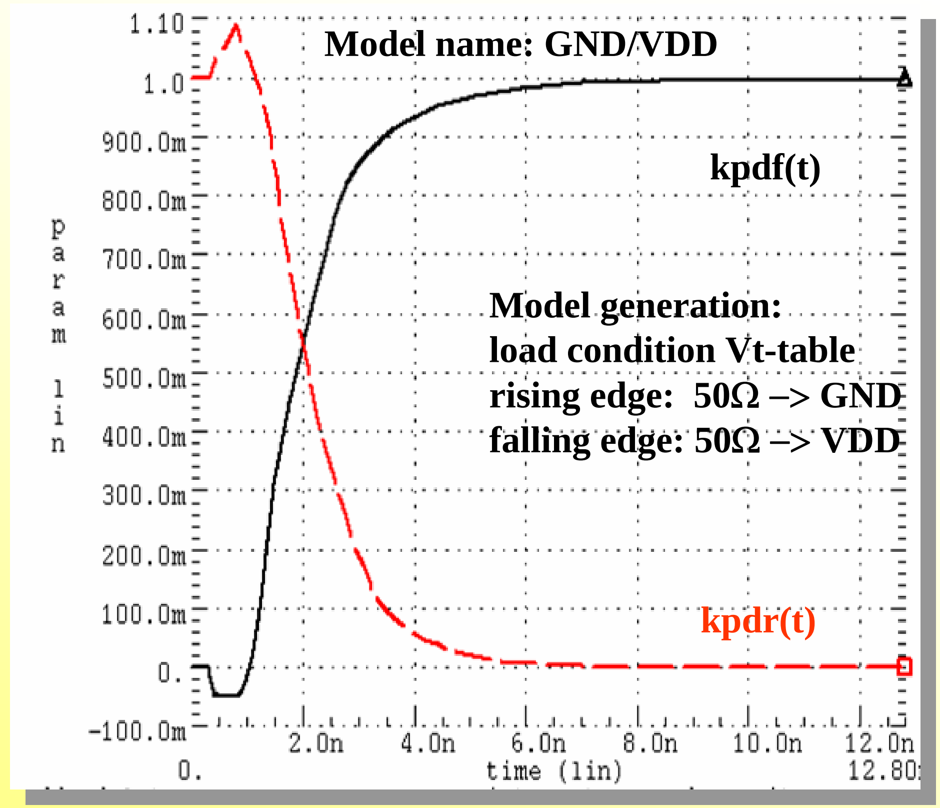
  Vt-tables for at least 2 load conditions available

  None assumption of the multiplier relationships

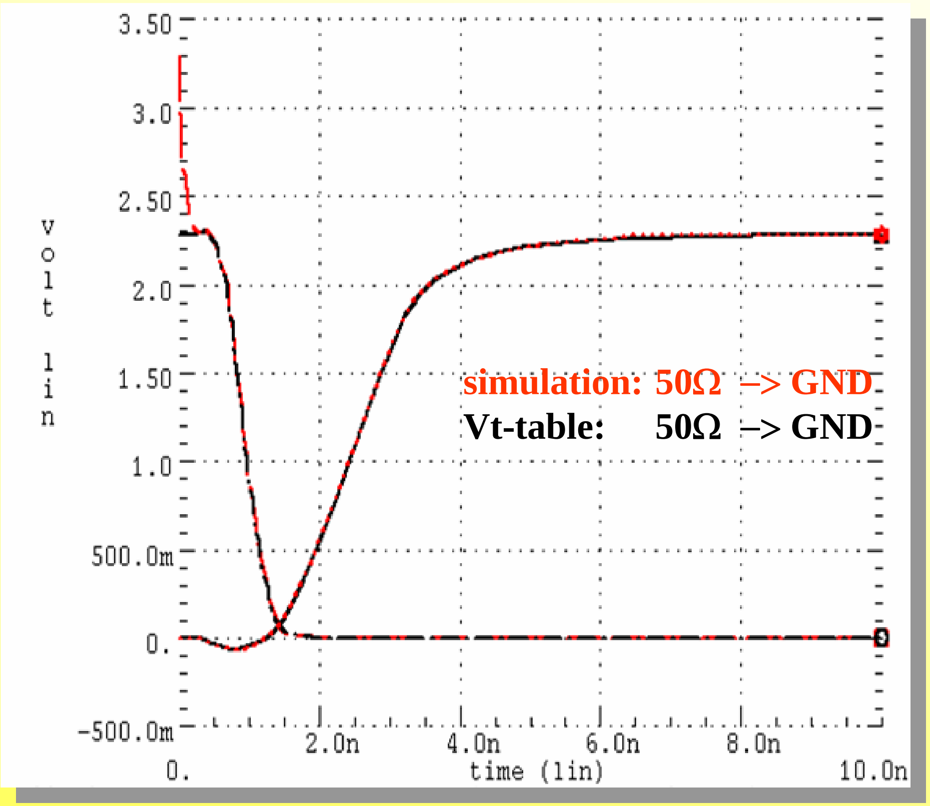
  kpur/f(t); kpdr/f(t); function range: 0;1 to 1;0

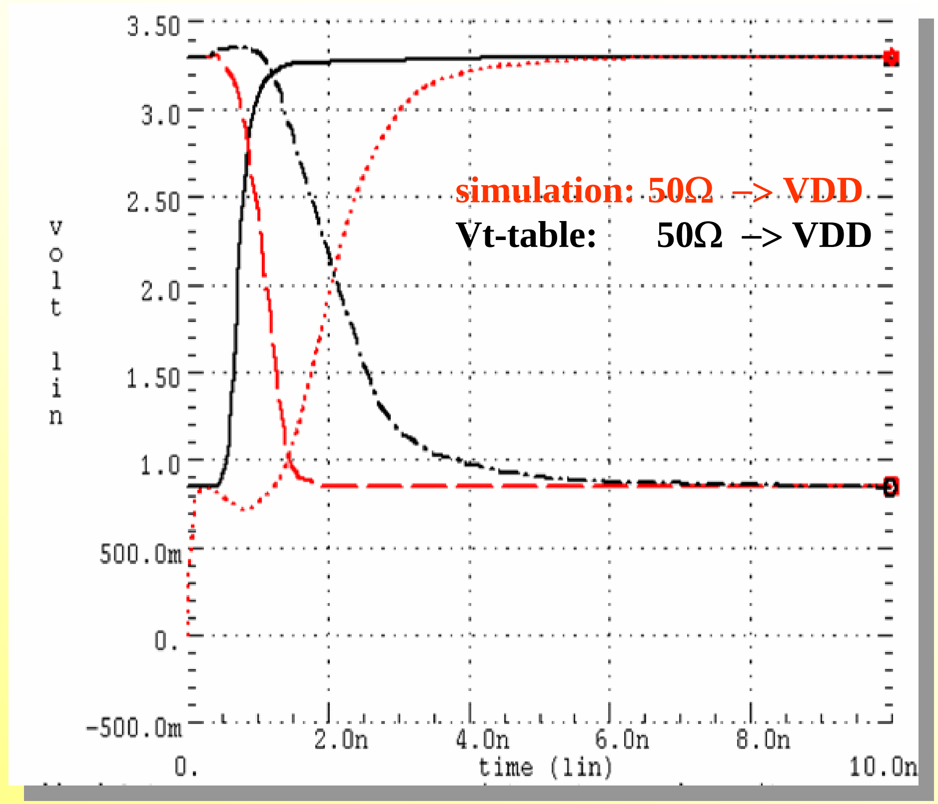
One-waveform model
Multiplier extraction with different loading conditions



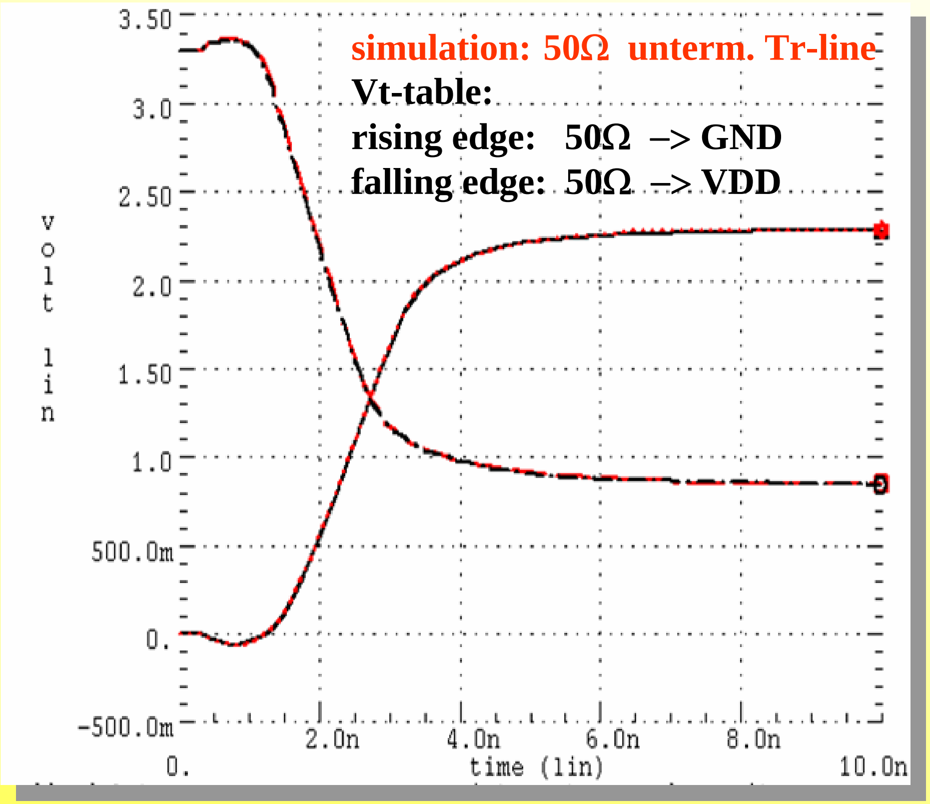


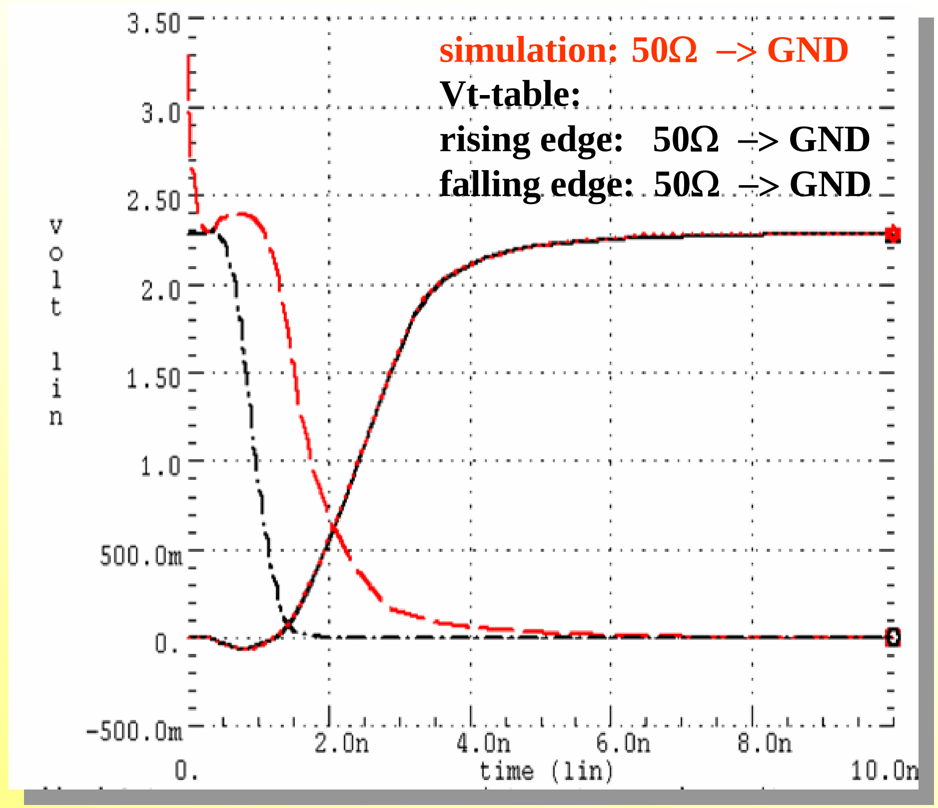
One-waveform model GND/GND
Comparison of Vt-tables and simulated rising/falling waveforms





One-waveform model GND/VDD
Comparison of Vt-tables and simulated rising/falling waveforms





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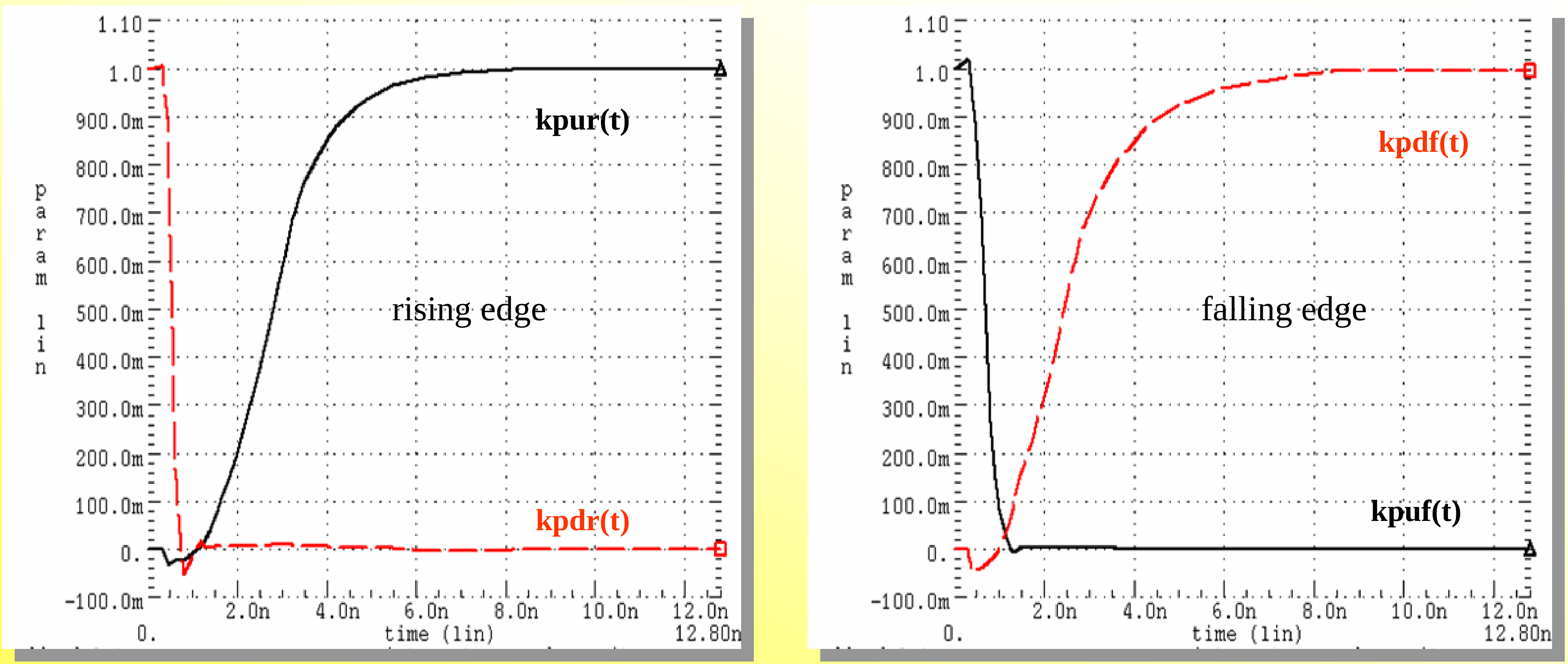
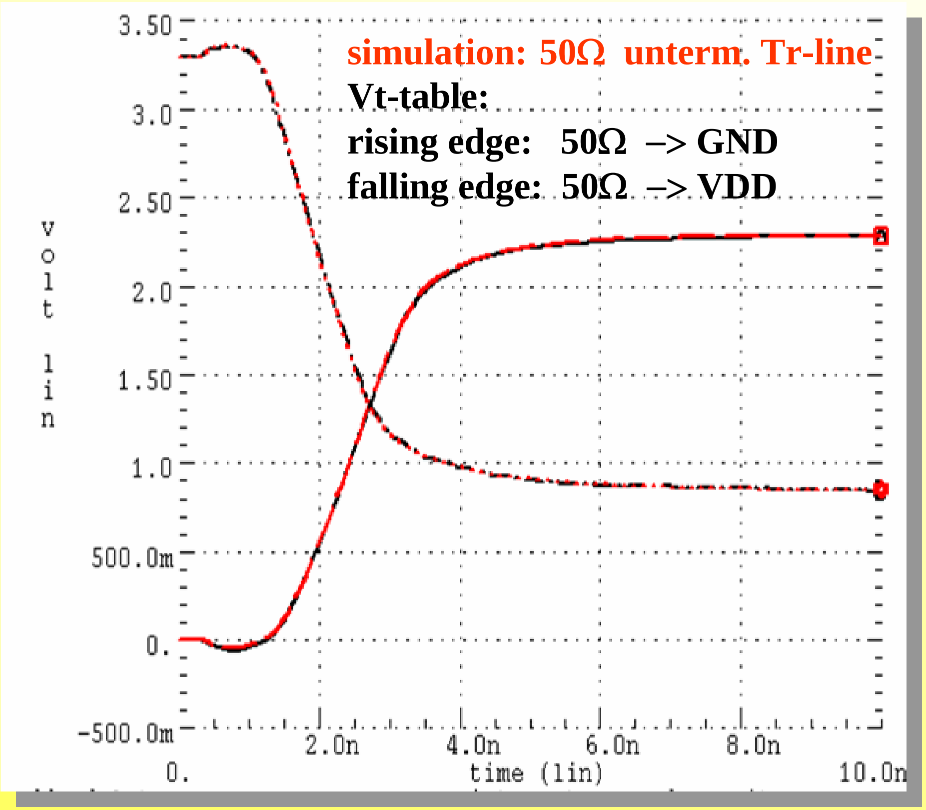
Two-waveform model

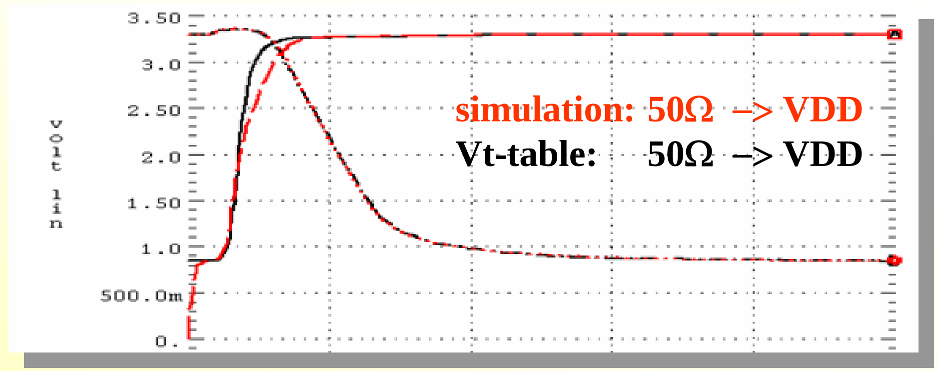
Multiplier extraction with each two loading conditions for rising and falling edges

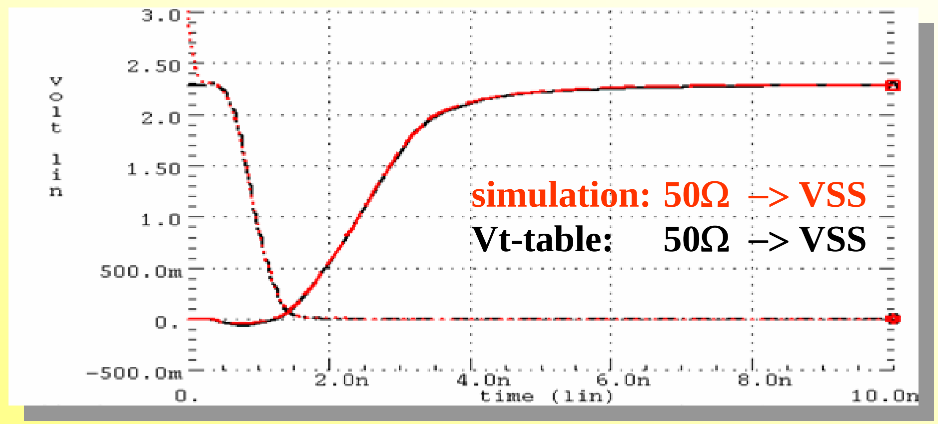


Two-waveform model

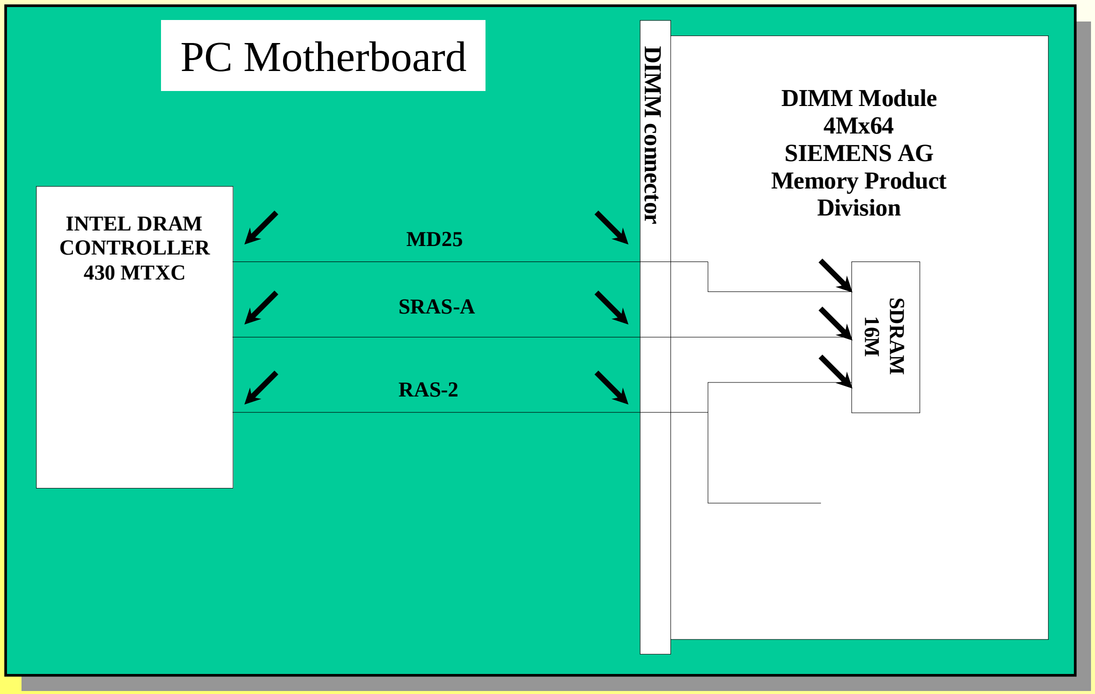
Comparison of Vt-tables and simulated rising/falling waveforms





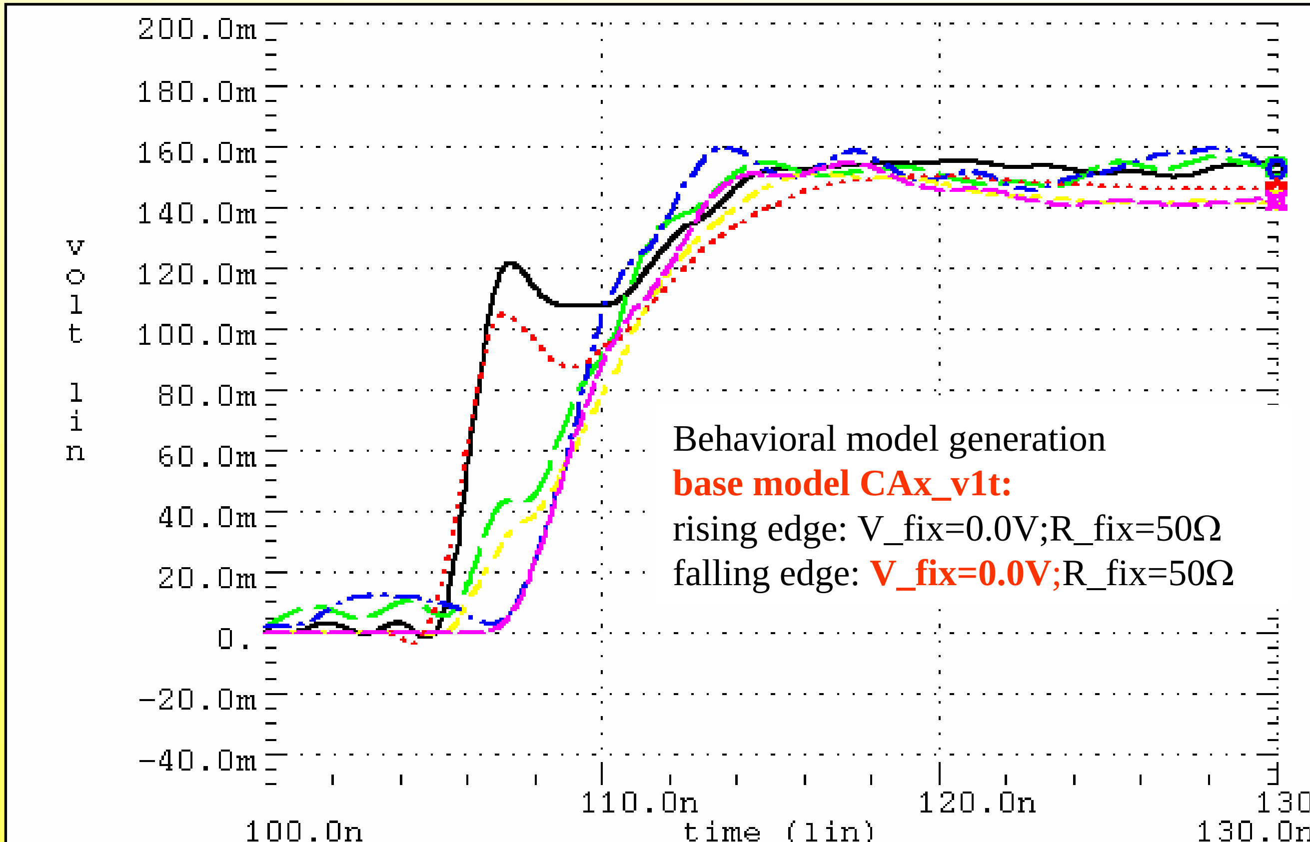


PC board Signal Integrity analysis block diagram



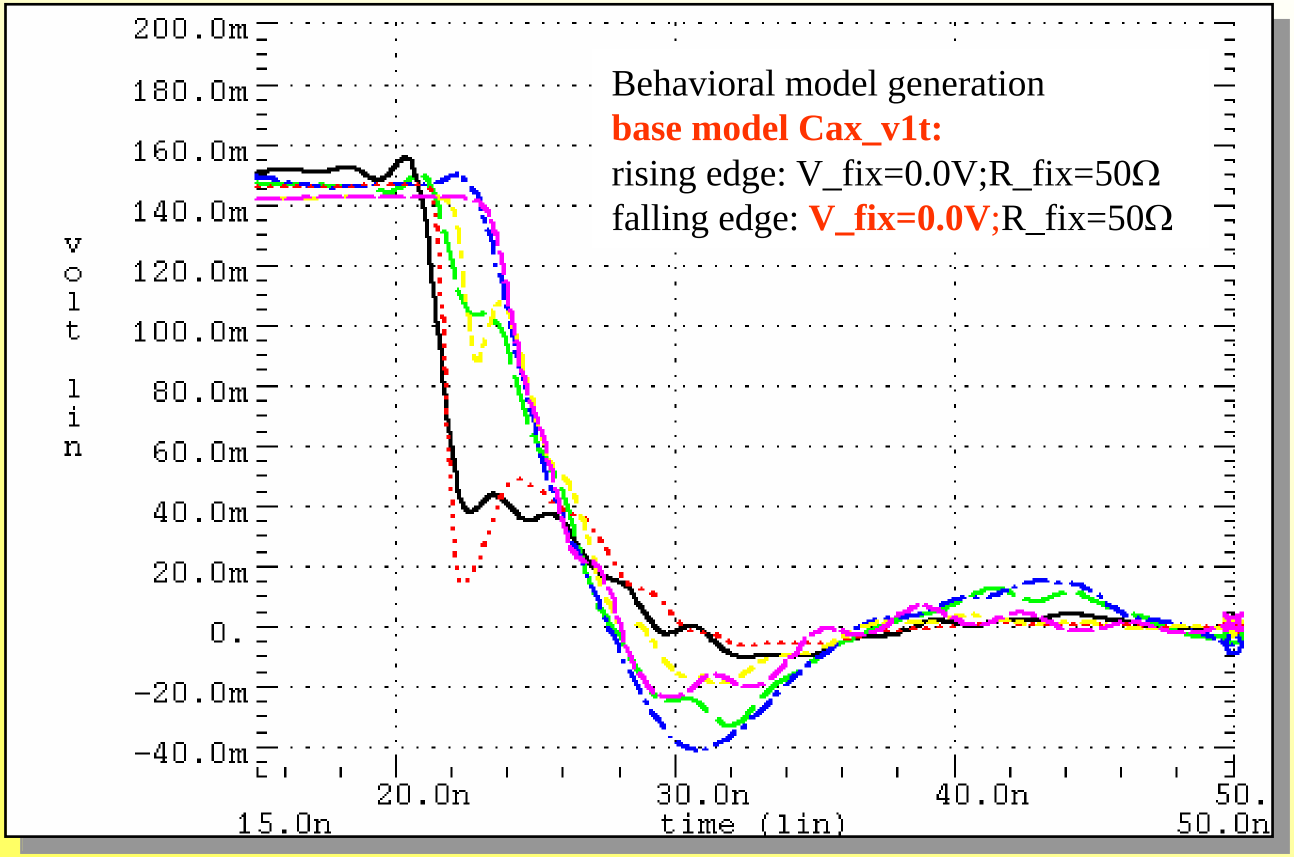
- Investigated Signals:
  Control signal SRAS-A; RAS-2
  Data signal (read) MD25
- Device modelling:
  IBIS based HSPICE One-waveform behavioral models including package
- Transmission line modelling:
  HSPICE U-model
  Parameters extracted from lay-up using 2d-field solver
- Connector modelling:
  Vendor model

Signal SRAS-A: MTXC model v1t (50Ω–>GND; 50Ω–>GND) rising edge



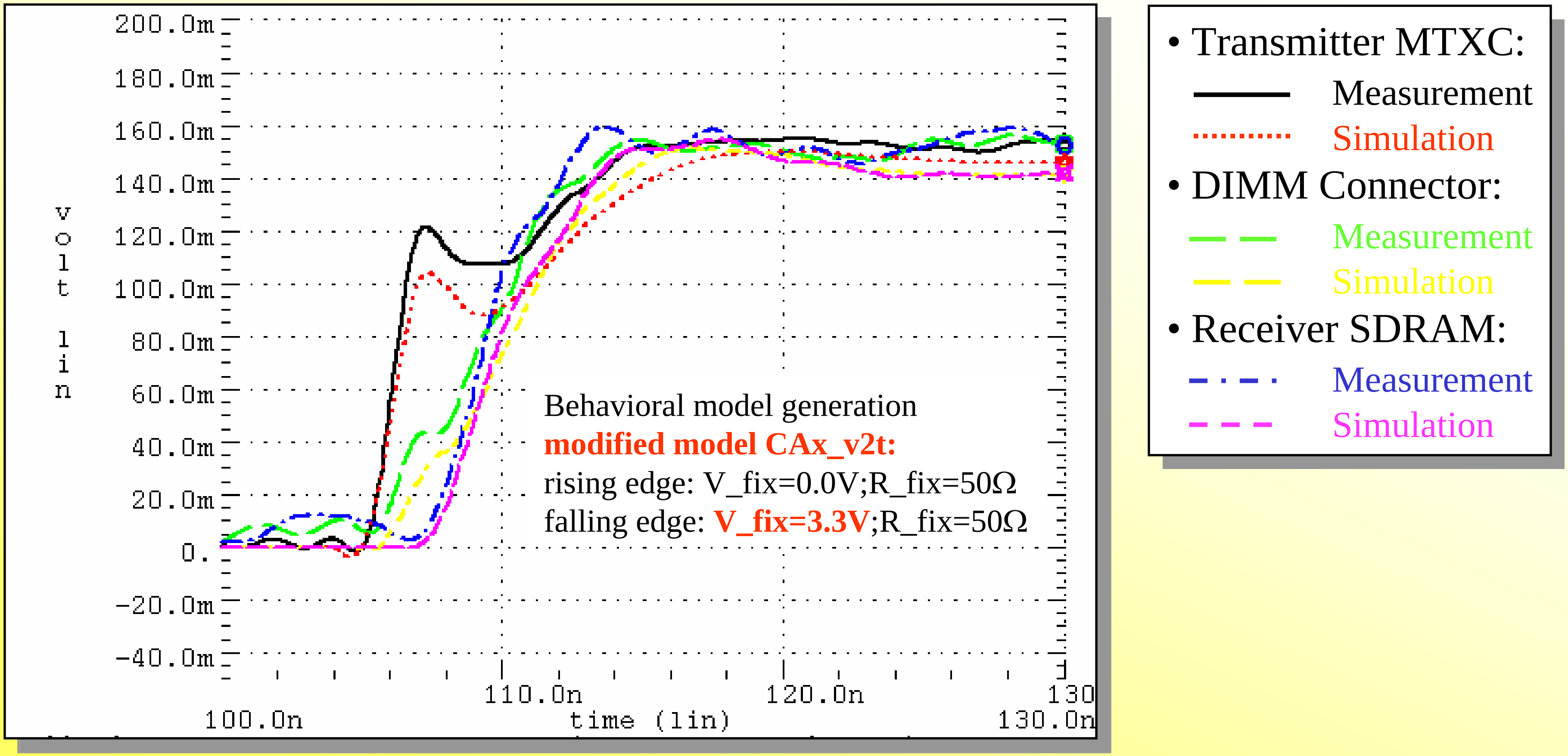
- Transmitter MTXC:
  - Measurement
  - Simulation
- DIMM Connector:
  - Measurement
  - Simulation
- Receiver SDRAM:
  - Measurement
  - Simulation

Signal SRAS-A: MTXC model v1t (50Ω–>GND; 50Ω–>GND) falling edge

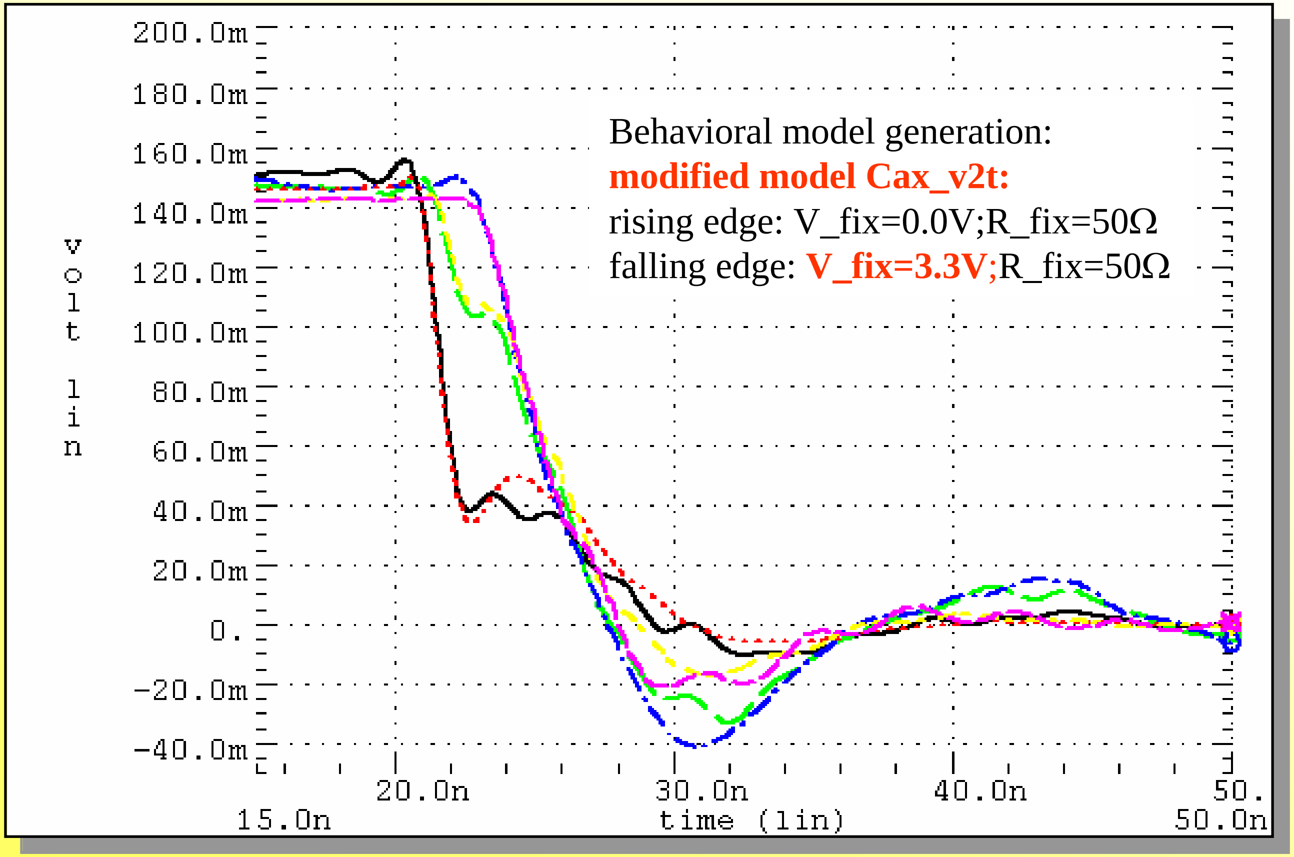


- Transmitter MTXC:
  - Measurement
  - Simulation
- DIMM Connector:
  - Measurement
  - Simulation
- Receiver SDRAM:
  - Measurement
  - Simulation

Signal SRAS-A: MTXC model v2t (50Ω–>GND; 50Ω–>VDD) rising edge

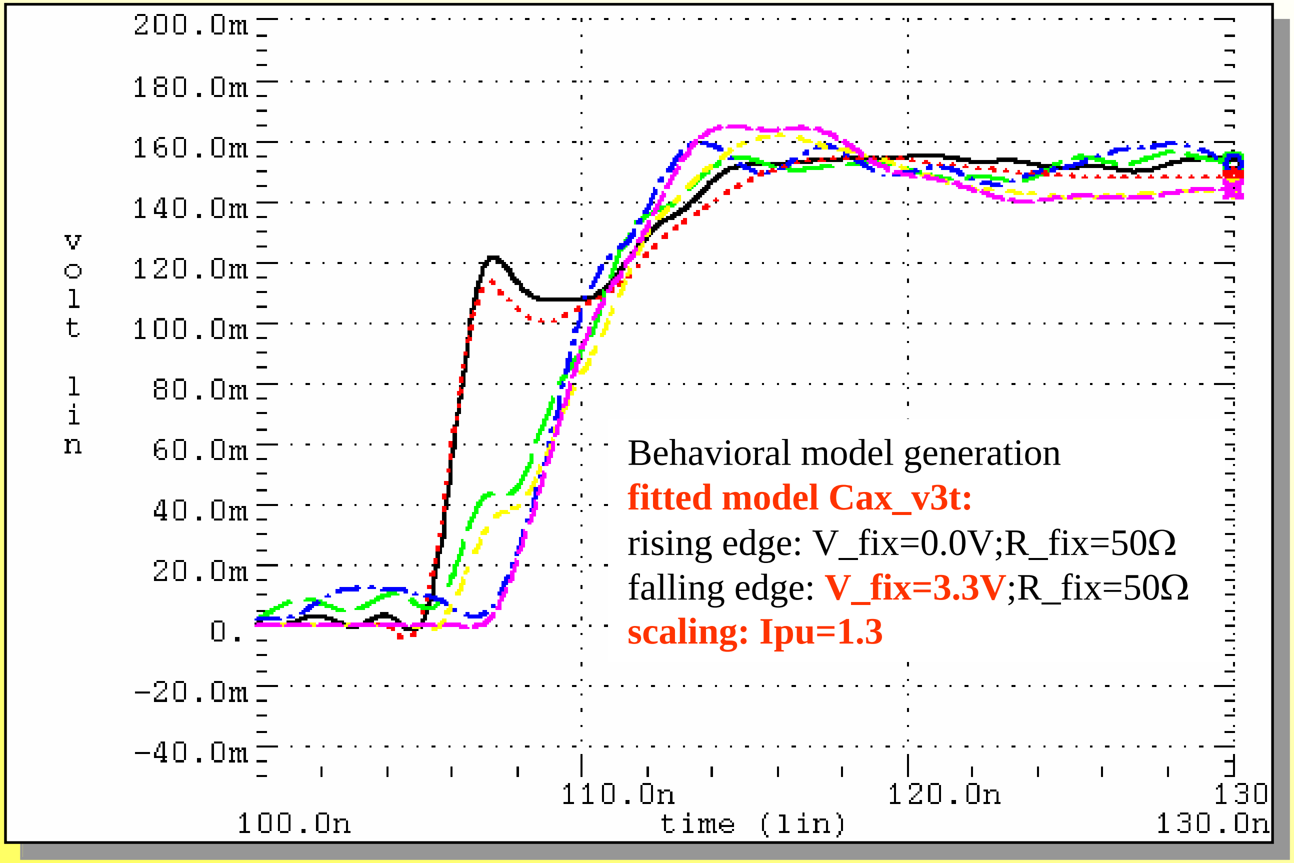


Signal SRAS-A: MTXC model v2t (50Ω–>GND; 50Ω–>VDD) falling edge



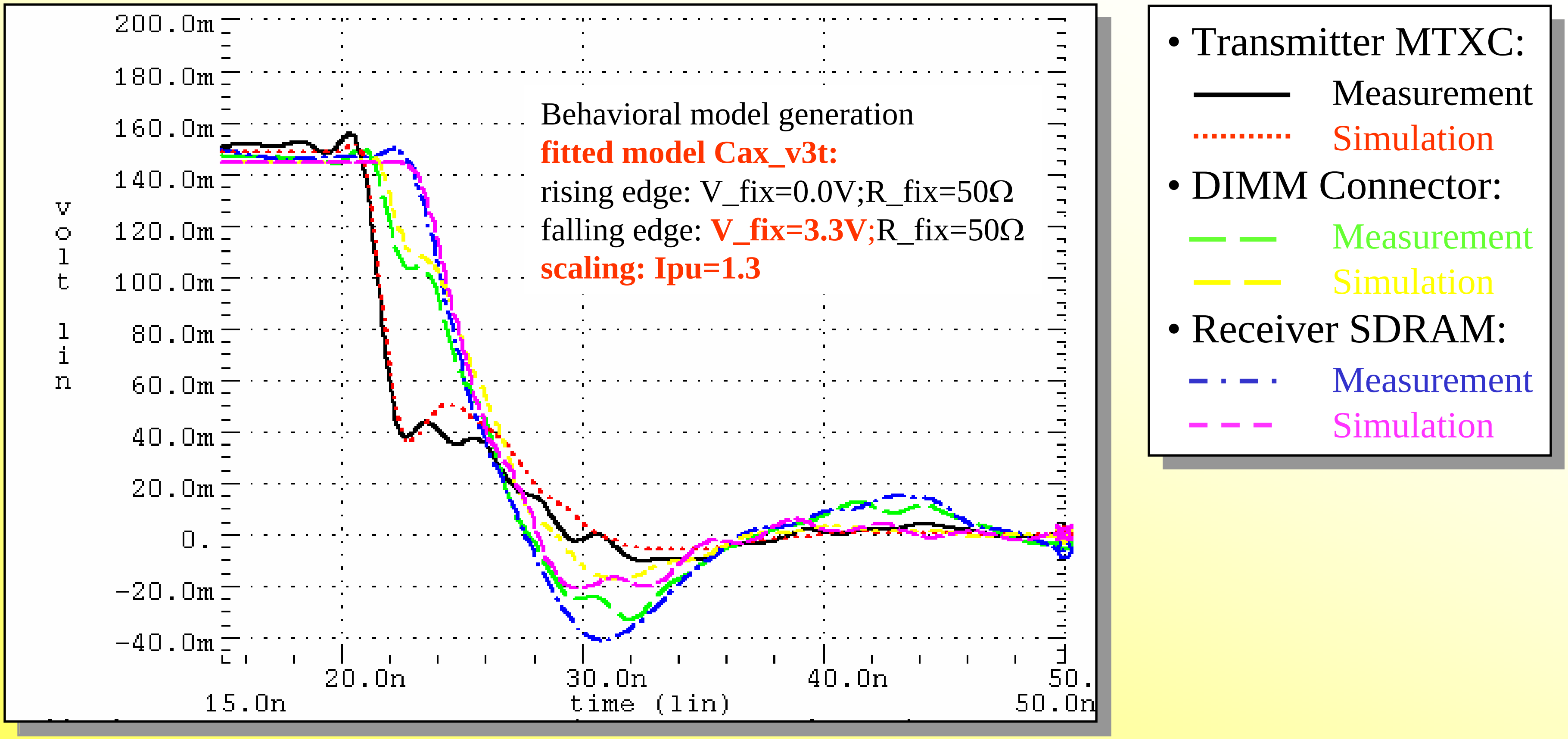
- Transmitter MTXC:
  - Measurement
  - Simulation
- DIMM Connector:
  - Measurement
  - Simulation
- Receiver SDRAM:
  - Measurement
  - Simulation

Signal SRAS-A: fitted MTXC model. Ipu scaling rising edge

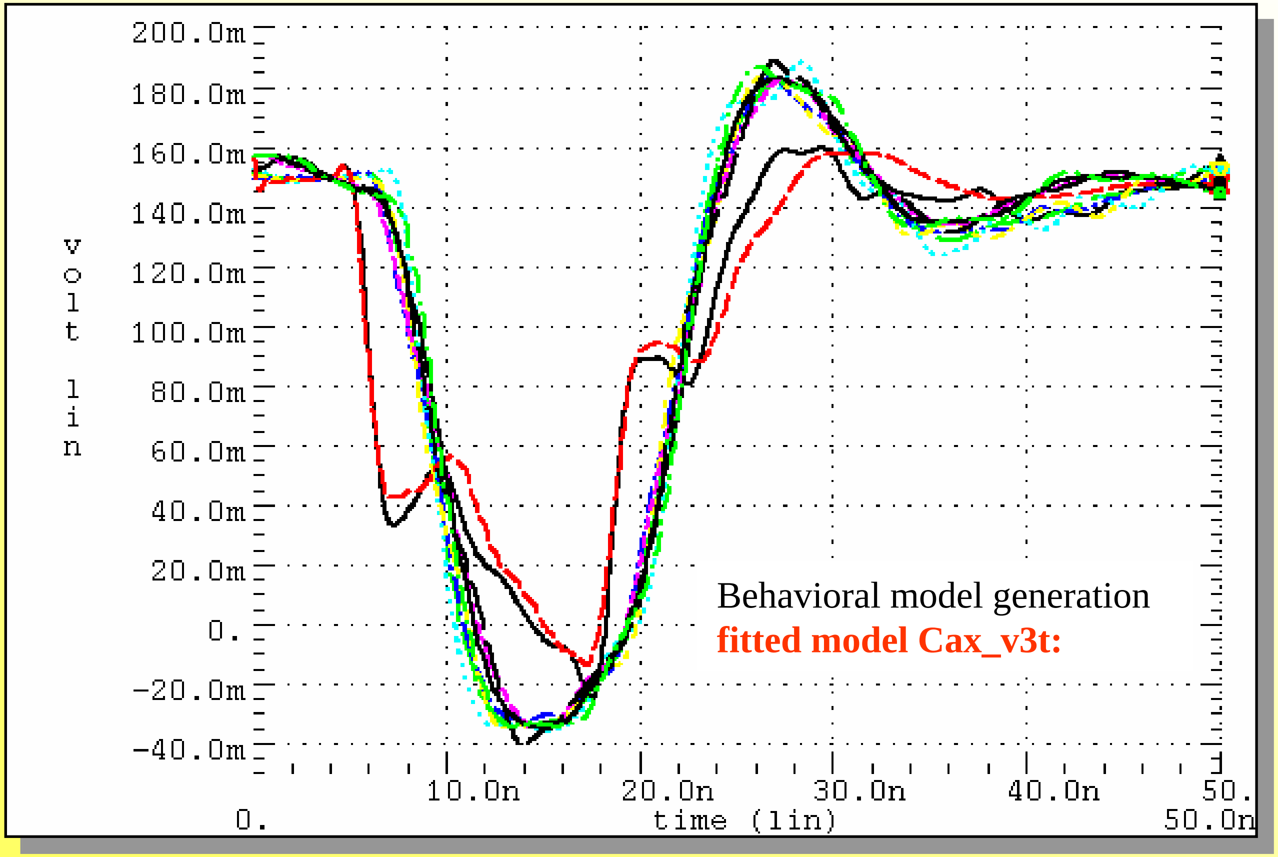


- Transmitter MTXC:
  - Measurement
  - Simulation
- DIMM Connector:
  - Measurement
  - Simulation
- Receiver SDRAM:
  - Measurement
  - Simulation

Signal SRAS-A: fitted MTXC model. Ipu scaling falling edge

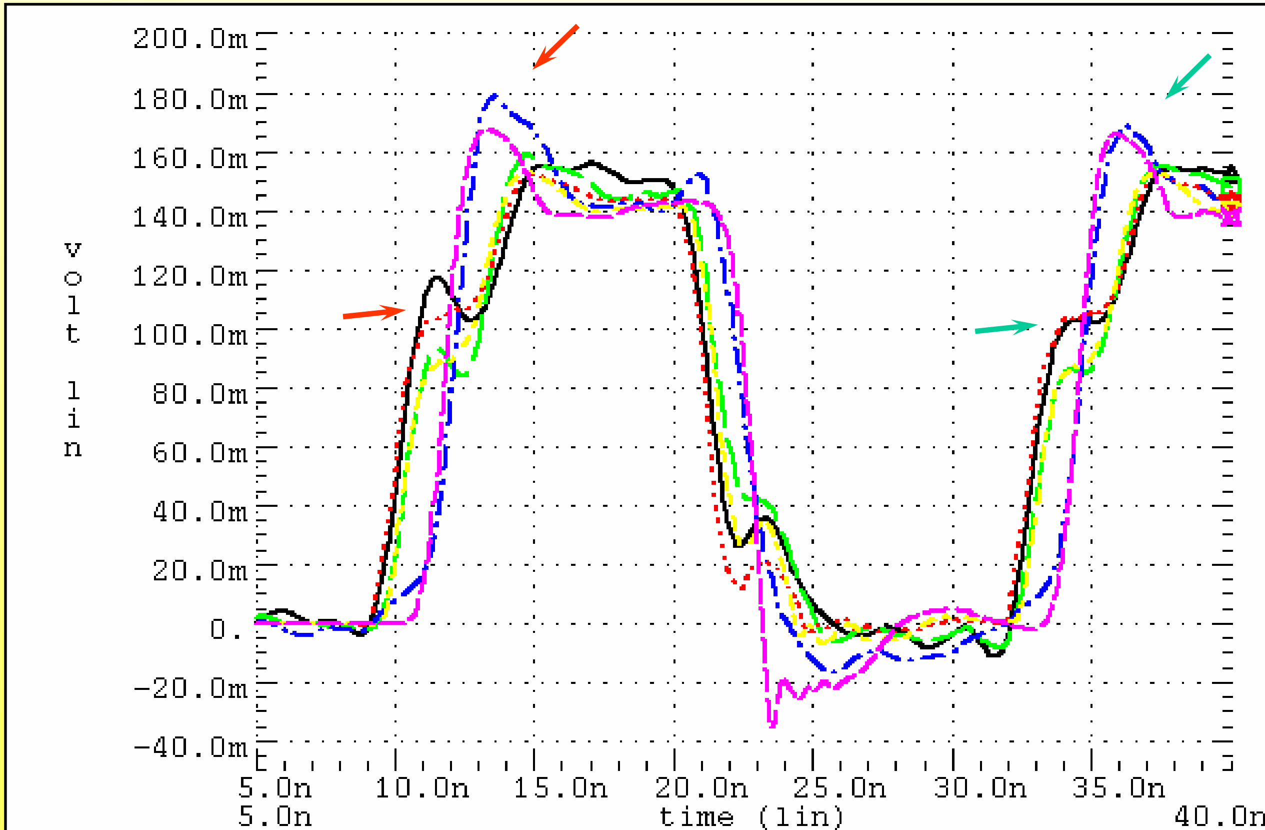


Signal RAS-2: fitted MTXC model



- Transmitter MTXC:
  - Measurement
  - Simulation
- DIMM Connector:
  - Measurement
  - Simulation
- Receiver SDRAM:
  - Measurement
  - Simulation

Signal MD25 read: SDRAM model (50Ω–>GND/10pF; 50Ω–>VDD/10pF)



- Transmitter SDRAM:
  - Measurement
  - Simulation
- DIMM Connector:
  - Measurement
  - Simulation
- Receiver MTXC:
  - Measurement
  - Simulation

Conclusions

- Exact driver modelling is one of the most important key-points to get realistic simulation results
- Validity of one-waveform models is limited on the loading condition of waveform table generation
- Validity of two-waveform models covers a wide range of loading conditions
- IBIS models should have at least waveform tables for two different loading conditions to enable two-waveform model generation
- IBIS version 1.1 models are not sufficient
- Simulations are realistic and in good coincidence with measurements if loading conditions of IBIS model generation correspond with the application