IBIS: 30 Years and Counting

The Early History

Don Telian
SI Guys, USA
Arpad Muranyi
Siemens EDA, USA
Will Hobbs
Formerly Intel Corp., Retired

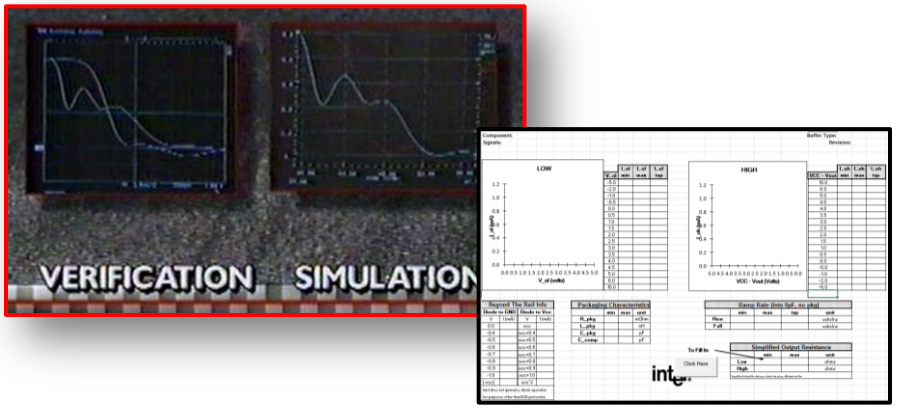
DesignCon Hybrid IBIS Summit
February 3, 2023
Santa Clara, California

A WORLD WITHOUT IBIS

How could that be?!

The Perfect Storm

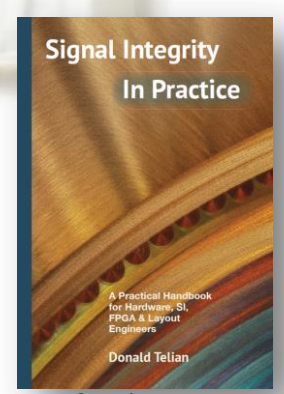
- PCI Spec -> Behavioral Modeling -> 5,000 hours
  - Arpad Muranyi
- Pentium Chipset
  - Analysis
  - Models to customers



- The “intel Buffer Information Sheet” -> iBIS
- Road trip
  - Some tools already had it

“a match on dynamite”

The 1.0 “Spec”



Section 7.1

- Vision: The IBIS Open Forum
  - Begins 4/23/93, iBIS -> IBIS
- 7 to 9 EDA Vendors
  - “Intend to support IBIS”
  - Golden Waveforms -> “IBIS Capable”
  - BIRDs
- 1.0 spec resolved in 4 meetings
  - https://ibis.org/minutes/min1993/
  - Released to larger audience at DAC on 6/17/93

Technical Challenge and Solution

- Challenge simulating EISA bus at 50 MHz– SPICE models not accurate
- Verified inaccuracy on curve tracer
- Devised I/V method under HSPICE and tweaked until accurate enough
- Moved on to PCI development
- Refined model methodology (moved from Ramp to V/t)

Execution, Expansion

- My (Will Hobbs') charter in Intel as Modeling Manager:
  - Assemble, develop and distribute logic and I/O models of Intel processors and chipsets to help customers with early designs
- Environment for I/O Buffer models within Intel in 1992
  - Spice Netlist level models
    - Not available for customers:
      - Too much proprietary info, too slow to simulate
  - Simplified Electrical Models (SEM/First Order Models)
    - Behavioral, created by x86 CPU division
    - Simple RLCD models tweaked to emulate I/O characteristics
    - Generated largely by hand, then automated
    - Fast, supported by all analog simulators
    - Limited in accuracy at process corners, complex load topologies
    - Time-consuming to generate and validate
  - "Second Order Models"
    - Behavioral, created by chipset division
    - Tabulated list of I/O characteristics over corners
    - Generated by simulation or measurement
    - Fast, but only supported by two analog simulators
- Some inter-divisional friction apparent (1st order versus 2nd order models)

First Intel I/O Modeling Summit and Workgroup

- November 1992 road trip to visit European customers– message clear: accurate and consistent models needed 6 months to 1 year before silicon
- Convened I/O Buffer Modeling Summit within Intel on 12/7/92
  - Participants included divisions producing and consuming models, and technologists
  - Presentations described both SEM and 2nd order models in detail
  - Light bulb moment: SEM is a subset of 2nd order model, not in conflict
- Formed internal working group to hammer out convergence
  - Met weekly, addressed:
    - Model generation and validation methods (automation, “golden topologies”)
    - Accuracy
    - What corners to support (fast, slow, average)
    - Distribution to customers
    - Support by EDA Vendors
  - Coined name, iBIS (Intel Buffer Information Sheet), quickly changed it to IBIS (I/O Buffer Information Sheet) to encourage other IC Vendors to join
  - Final nut to crack: getting more than 2 EDA vendors to support IBIS

Engaging the Industry

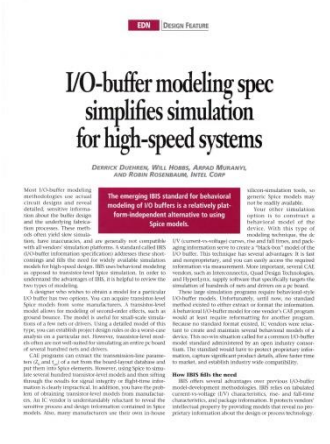
- First IBIS Open Forum for the Wider Industry: 4/23/93
  - Don Telian convened meeting to address lack of broader EDA Support
    - 7 Simulator Vendors and Intel took part: Hyperlynx , Integrity, Intusoft, Meta-Software, MicroSim , Quad-Design, Quantic Labs
  - Open Forum met biweekly
    - Other EDA vendors joined: Cadence Design, Contec
    - Agreement reached on content of IBIS V1.0 by third meeting, 5/21/93
- IBIS opened to the industry at DAC, 6/17/93
  - Broader participation:
    - AnSoft, Cadence Design, Contec, High Design Technology, Integrity Engineering, Intel Corporation, Logic Modeling Corp., Mentor Graphics, MicroSim, North Carolina State University, Performance Signal Integrity, Quad-Design, Quantic Labs, Thomson-CSF/SCTF
  - IBIS changed to I/O Buffer Information Specification (instead of Sheet)
  - Version 1.0 ratified
  - Agreed to tri-weekly or monthly meetings and additional Face-to-Face Summits

Subsequent Growth, the Next 3 Years

- Formalized IBIS Open Forum
  - Chose officers
    - Will Hobbs, Chair through 1/97; various treasurers and librarians
  - Addressed improving and enhancing IBIS
    - Introduced the Buffer Issue Resolution Document, or “BIRD”
  - Set up database, email reflector
  - Formalized charter and other administrivia
  - Did Trademark Search
  - Set up bank account
  - Encouraged press, wrote articles and press releases
    - Featured in December, 1993 EDN in their “Hot 100 Products” of the year
- Expanded membership
  - Critically, more silicon vendors
  - Additional EDA Vendors


100 HOT PRODUCTS

HOT 1993


EDN Design Feature

I/O-buffer modeling spec simplifies simulation for high-speed systems

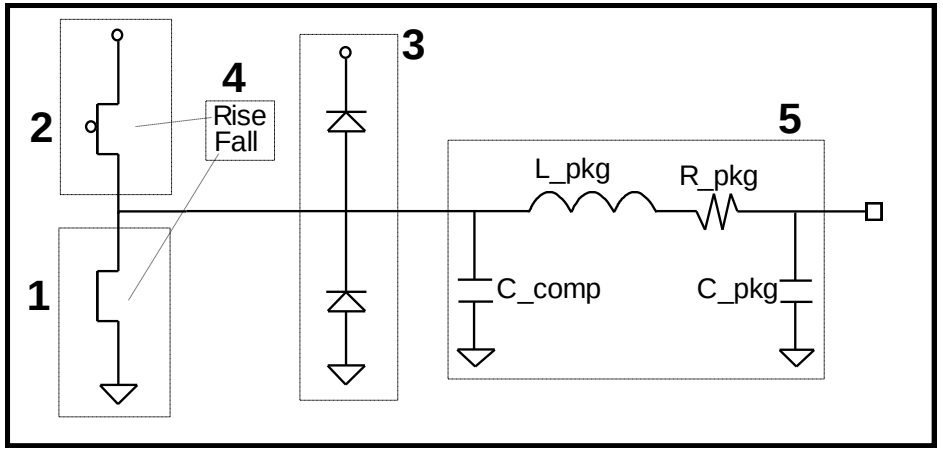
More Progress

- Created additional support collateral
  - Golden Parser, funded by member companies
    - Suggested by Jon Powell, developed by Paul Munsey and Ron Neville
    - Freed us from having to hand-check users' models
  - Cookbook– aided model users and developers
- Continued improving the spec
  - E.g., Added Support for more devices (ECL, Open Drain, improved package models, …)
- Affiliated with standards organizations
  - Nationally (US), IBIS V2.1 became ANSI/EIA-656
  - Internationally, affiliated with IEC, resulting in IEC-62014
- In January, 1997, I (Will Hobbs) turned over the gavel:
  - Chair: Bob Ross
  - Vice Chair: Syed Huq
  - Librarian: Jon Powell
- And the rest, as they say, is history
- Here's to 30 more years!!

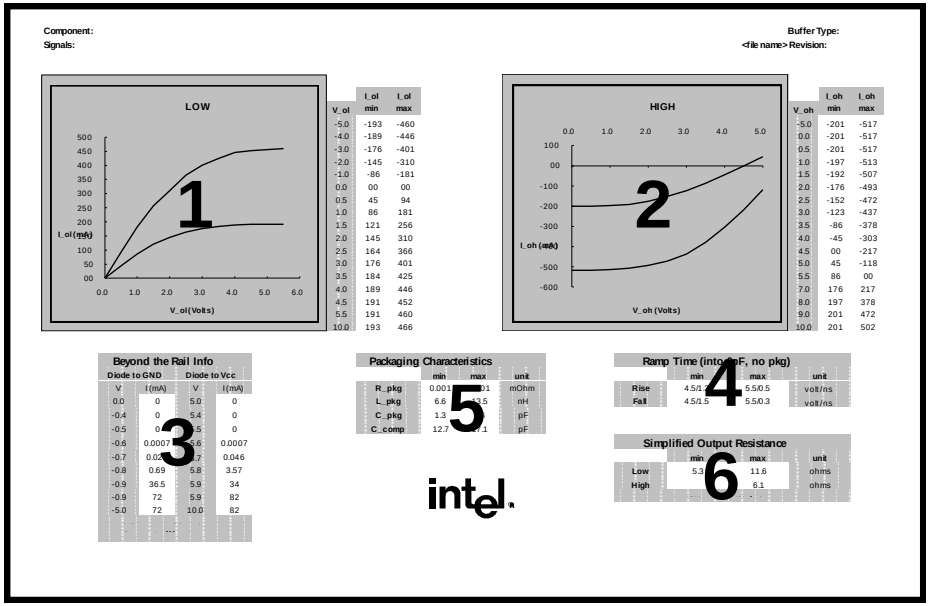
Appendix

What the early IBIS Sheets Embodied

Elements of an I/O Structure

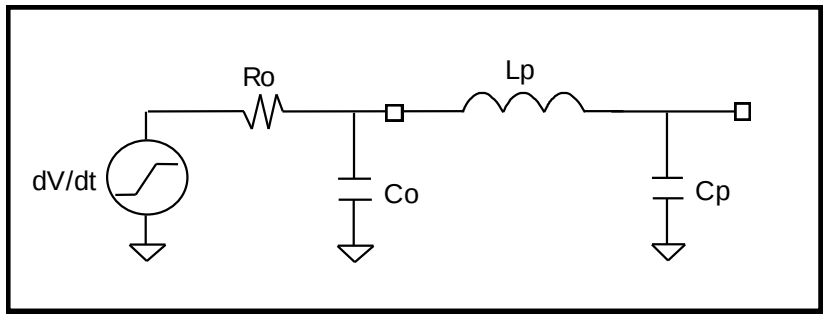


Example IBIS Sheet



IBIS and Simplified Electrical Model Correlation

Simplified Electrical Model (SEM)

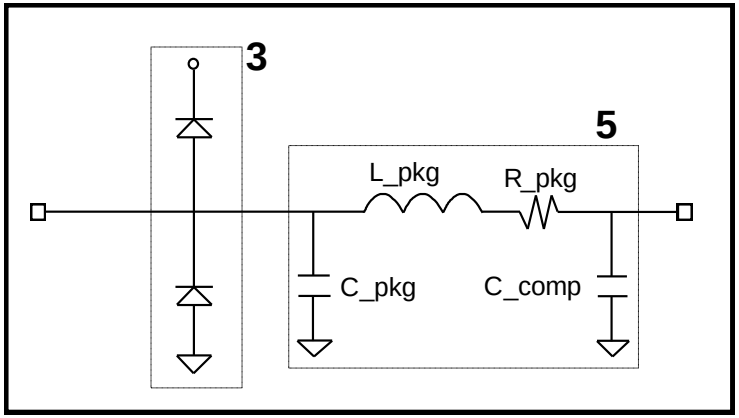


Correlation Between SEM and IBIS Parameters

SEM Parameter	Corresponding IBIS parameter	IBIS Diagram Number
dV/dt	Ramp Time	4
Ro	Simplified Output Resistance	6
Co, Cin	C_comp	5
Lp, Cp	L_pkg, C_pkg	5

IBIS Input Structure

IBIS Input Structure



Early IBIS Sheet Example

[IBIS Ver] 1.0

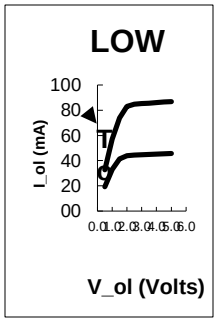
[File name] example.ibs

[File Rev] 1.0

[Componenet] p24c

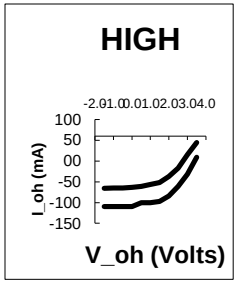
[pulldown]

V_bl	I(typ)	I(min)	(max)
-2.0	-340	-400	NA
-1.5	-190	-210	NA
-1.0	-60	-75	NA
-0.5	-23	-37	NA
0.0	00	00	NA
0.5	19	33	NA
1.0	33	57	NA
1.5	41	74	NA
2.0	44	83	NA
2.5	44	85	NA
3.0	45	85	NA
3.5	45	86	NA
4.0	45	86	NA
4.5	45	87	NA
5.0	46	87	NA
7.0	47	88	NA



[pullup]

V_bh	I(typ)	I(min)	(max)
-2.0	-67	-110	NA
-1.5	-66	-110	NA
-1.0	-65	-110	NA
-0.5	-65	-110	NA
0.0	-63	-110	NA
0.5	-61	-100	NA
1.0	-57	-100	NA
1.5	-52	-97	NA
2.0	-38	-84	NA
2.5	-18	-61	NA
3.0	15	-32	NA
3.5	45	09	NA
4.0	75	52	NA
4.5	105	93	NA
5.0	136	130	NA
7.0	240	290	NA



[Beyond the Rail Info]							
[GND_clamp]				[POWER_clamp]			
IV	I (typ)	I(min)	I(max)	IV	I (typ)	I(min)	I(max)
0.0	0	NA	NA	5.0	0	NA	NA
-0.4	######	NA	NA	5.4	1.00E-04	NA	NA
-0.5	######	NA	NA	5.5	4.10E-03	NA	NA
-0.6	0.22	NA	NA	5.6	0.22	NA	NA
-0.7	NA	NA	NA	5.7	NA	NA	NA
-0.8	NA	NA	NA	5.8	NA	NA	NA
-0.9	NA	NA	NA	5.9	NA	NA	NA
-1.0	NA	NA	NA	6.0	NA	NA	NA
-5.0	NA	NA	NA	10.0	NA	NA	NA

[Comment char] |_char

[Date] 06/15/93

[Source] From cse simulation data

[Notes] This is it

[Disclaimer] Intel does not Guaranty diode operation

[Manufacturer] Intel

[Model] model_name

Model_type input

Polarity Inverting

Enable Active-High

Vinl = 0.8V

vinh = 2.0

|variable typ min max

C_comp 12.0pF 10.0pF 15.0pF

[Variable typ min max

[Voltage range] 5.0V 4.5V 5.5V

[Pin] signal_name model_name R_pin L_pin C_pin

|

1 RAS0# Buffer1 200.0m 5.0nH 2.0pF

2 RAS#1 Buffer2 209.0m NA 2.5pF

..

...

....

20 Vcc5 Power1 200.0m NA 1.0pF

False

[Package]			
variable	typ	min	max
R_pkg	NA	140m	325m
L_pkg	NA	8.52nH	14.49nH
C_pkg	NA	6pF	6.6pF
C_comp	NA	6.1pF	6.1pF

[Ramp] (Time (into 0pF, no pkg)			
variable	typ	min	max
dv/dt_r	NA	3.4/1.914n	2.8/1.813n
dv/dt_f	NA	3.4/2.1314n	2.8/1.330n

Simplified Output Resistance			
	min	max	unit
Low	20.0	62.5	ohms
High	44.5	133.4	ohms

Assumed High Level: Low= 5 volts, High= 5 volts

Intel does not guarantee diode operation for purposes other than ESD protection

IBIS EDN Article
March 16, 1995

EDN | DESIGN FEATURE

I/O-buffer modeling spec simplifies simulation for high-speed systems

DERRICK DUEHREN, WILL HOBBS, ARPAD MURANYI, AND ROBIN ROSENBAUM, INTEL CORP

The emerging IBIS standard for behavioral modeling of I/O buffers is a relatively platform-independent alternative to using Spice models.

Most I/O-buffer modeling methodologies use actual circuit designs and reveal detailed, sensitive information about the buffer design and the underlying fabrication processes. These methods often yield slow simulation, have inaccuracies, and are generally not compatible with all vendors' simulation platforms. A standard called IBIS (I/O-buffer information specification) addresses these shortcomings and fills the need for widely available simulation models for high-speed design. IBIS uses behavioral modeling as opposed to transistor-level Spice simulation. In order to understand the advantages of IBIS, it is helpful to review the two types of modeling.

A designer who wishes to obtain a model for a particular I/O buffer has two options. You can acquire transistor-level Spice models from some manufacturers. A transistor-level model allows for modeling of second-order effects, such as ground bounce. The model is useful for small-scale simulations of a few nets or drivers. Using a detailed model of this type, you can establish project design rules or do a worst-case analysis on a particular net. However, transistor-level models often are not well-suited for simulating an entire pc board of several hundred nets and drivers.

CAE programs can extract the transmission-line parameters (Z_0 and t_{pd}) of a net from the board-layout database and put them into Spice elements. However, using Spice to simulate several hundred transistor-level models and then sifting through the results for signal integrity or flight-time information is clearly impractical. In addition, you have the problem of obtaining transistor-level models from manufacturers. An IC vendor is understandably reluctant to reveal the sensitive process and design information contained in Spice models. Also, many manufacturers use their own in-house silicon-simulation tools, so generic Spice models may not be readily available.

Your other simulation option is to construct a behavioral model of the device. With this type of modeling technique, the dc I/V (current-vs-voltage) curves, rise and fall times, and packaging information serve to create a "black-box" model of the I/O buffer. This technique has several advantages: It is fast and nonproprietary, and you can easily access the required information via measurement. More important, several CAE vendors, such as Interconnectix, Quad Design Technologies, and HyperLynx, supply software that specifically targets the simulation of hundreds of nets and drivers on a pc board.

These large simulation programs require behavioral-style I/O-buffer models. Unfortunately, until now, no standard method existed to either extract or format the information. A behavioral I/O-buffer model for one vendor's CAE program would at least require reformatting for another program. Because no standard format existed, IC vendors were reluctant to create and maintain several behavioral models of a device. This no-win situation called for a common I/O-buffer model standard administered by an open industry consortium. The standard would have to protect proprietary information, capture significant product details, allow faster time to market, and establish industry wide compatibility.

How IBIS fills the need

IBIS offers several advantages over previous I/O-buffer model-development methodologies. IBIS relies on tabulated current-vs-voltage (I/V) characteristics, rise- and fall-time characteristics, and package information. It protects vendors' intellectual property by providing models that reveal no proprietary information about the design or process technology.

EDN Hot 100 Products of 1993

100 HOT PRODUCTS

Active-filter design tool. Fildes 3.1 helps you design, optimize, and analyze active filters on a PC using DOS. The software gives you a choice of 10 active-filter topologies and includes a gain-sensitivity-product minimization algorithm that accounts for both passive and active sensitivities. $79.95. **Consulting and Training Services,** Sharpes, FL. (407) 633-9868. **Circle No. 513**

Learn VHDL for free. A self-paced audio-visual tutorial from Racal-Redac lets you use your workstation to learn how to apply VHDL. The tutorial runs under Unix and makes use of the company's Dramatix/Instrux multimedia program. Once you load the program, you sit through a realistic 15-minute overview that steps you through a simple design, runs a simulation, sets breakpoints in the VHDL code, makes corrections, and so on, as you follow each step.You also get VHDL-LE, a self-paced education package that lets you work through exercises in a manual and workbook. The program usually takes 40 hours to complete. The software requires a SPARC-based workstation and about 20 Mbytes of disk space. The company aims the material at its customers, but it's free to qualified designers. **Racal-Redac,** Mahwah. NJ. (201) 848-8000. **Circle No. 514**

Simulating switch-mode power supplies. A free newsletter from Intusoft describes models for switching converters including buck, boost, buck-boost, and Cuk topologies. Contact the company for a copy of its March newsletter. **Intusoft,** San Pedro, CA. (310) 833-0710. **Circle No. 515**

Low-cost DSP analysis software. Siglab is an interpretive DSP language for signals and systems analysis. You use it to generate test signals and system responses and display them using 2-D and 3-D custom graphics in multiple-graph windows that allow data location, zoom, and overlay. The software includes 140 built-in mathematical and systems operations used in DSP including FFTs, phase and group delay, fixed-point support, matrix algebra, polynomial generation and evaluation, window generation, complex arithmetic, and signal operators (convolution, correlation). DOS version, $99. **The Athena Group Inc,** Gainesville, FL. (904) 371-2567. **Circle No. 516**

Accurate digital models available for free. Intel's IBIS program promises to let digital-IC companies give away accurate circuit-level models of their devices. But IC makers have a tricky problem to solve before they can pass out models without giving away the farm. An accurate model can reveal proprietary design information to the IC makers' competitors. Under IBIS, simulation-software vendors will be able to generate models directly from the device maker's data. At least seven simulation-software vendors have agreed to support IBIS. An example of IBIS models is in Intel's "Pentium Processor Open Design Guide," chapter 17, order number 297267-001 free. **Intel Corp,** Santa Clara, CA. (800) 548-4724. **Circle No. 517**

Solid-state relay. The HSSR-7110 spst relay is housed in an 8-pin hermetic DIP. Contacts are rated for 0.8A ac/dc at 24V ac or 28V dc. The relay operates from a logic-level control signal (5 mA nom). Input/output isolation equals 1500V dc. The unit operates over the –55 to +125°C military temperature range. $75. **Hewlett-Packard Co,** Santa Clara, CA. (800) 752-0900. **Circle No. 518**

MS Excel-based worksheets and macros. Nineteen electronic-design tools based on MS Excel spreadsheet software are available individually at prices from $15 to $50 (or bundled in groups at a discount). Applications include linear systems analysis, spectral analysis, RF design, general engineering tools, and hardware component selection. Linear system applications include analyzing both real-time response and frequency response of systems. A spectral analysis tool produces FFTs of data. **Engineering Solutions,** Tarzana, CA. (818) 772-7231 **Circle No. 519**

Input module. The 7B35 4- to 20-mA-current input module includes an isolated loop power supply, which eliminates the need for an external supply when using a 2-wire transmitter. It operates from a single unregulated 24V supply and features a ±0.1% max span error, ±0.02% span nonlinearity, and ±1-µV/°C temperature stability. A galvanic transformer provides 1500V-rms isolation. The module meets IEEE-STD-472 and IEC-255-4 standards for transient protection. From $75 (1000). **Analog Devices Inc,** Wilmington, MA. (617) 937-1428. **Circle No. 52**

MOSFETs. The Si9420DY and Si9410DY are rated f 200 and 30V, respectively. The units are housed in 8-pin surface-mount packages and are mounted on low thermal-impedance copper lead frames, whic allow the units to di sipate 2.5W. The

Si9410DY, $0.77; Si9420DY, $0.46 (OEM qty). **Siliconix Inc,** 220 Laurelwood Rd, Santa Clara, CA 95054. (408) 9 8000. **Circle No.**

P-channel MOSFETs. single p-channel Si9430 has a 50-mΩ max on-re tance, and the dual p-ch nel Si9947DY has a 100 max on-resistance. The channel FET's source c nects directly to the hi side voltage when used a series load switch in tery applications. The nection eliminates the need for high gate volt associated with n-chan series switches. Both

Another EDN article, 9/2/93

EDN-DESIGN FEATURE

Treat pc-board traces as transmission lines to specify drive buffers

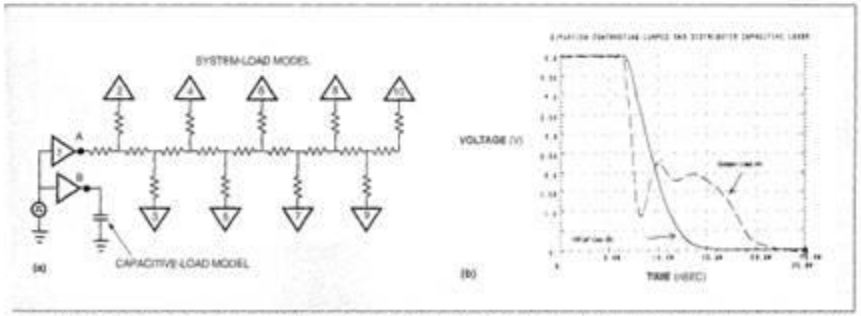
Donald Telian, Intel Corp

The Peripheral Component Interconnect (PCI) specification simplifies the design of buffer circuitry in high-speed interface systems. By using transmission-line concepts and employing ac specifications in place of dc values, PCI lets designers more accurately define a buffer's drive capability.

By employing transmission-line models and terms, the PCI specification developed by Intel Corp can thoroughly characterize the dynamic effects that result when you switch large distributed loads with a underspecified drive buffer. Because many designers oversimplify this problem, designing buffers with appropriate drive strength turns into a difficult task. Historically, designers have assumed that buffers work into simple capacitive loads. This assumption created few problems when system clock rates loafed along in the 1-MHz range. In today's world of 30-MHz-plus clock rates, however, real system loads are far from purely capacitive. In fact, even pc-board trace lengths can dramatically change the makeup of a buffer's load.

Viewing the buffer load as a simple capacitor can lead to many erroneous conclusions. The most common mistake designers make is to assume that an interconnect with many loads is like a large capacitor, which must therefore require a buffer with a large drive capability. It turns out that this is not the case, and designers must understand the transmission-line mechanisms involved here. To better understand the difference in driver response between a capacitive load and a true system load, consider **Fig 1a**.

Here, a system load is actually made up of numerous devices interconnected through traces that you can model as transmission lines. Aside from their clamping characteristics, the receiving devices are predominately capacitive. However, the system model represents a distributed capacitance and yields waveforms



g 1—A system load is made up of multiple devices interconnected through pc-board traces, which you can treat as transmission lines (a). is distributed capacitance yields waveforms very different from those of the lumped-capacitance model (b).