

# Study on potential feature additions for bit-by-bit simulation technique to address the DDR5 requirements.

DesignCon IBIS Summit, Santa Clara, California February 1, 2019 Ted Mido Synopsys Inc.

# **Background: Increasing Challenges in DDR4 and beyond**

Achieving Low BER with ISI, Crosstalk, SSO and Clock/Random Jitter

- Lossy coupled transmission lines
  - -Inter-Symbol Interference (ISI) and Crosstalk co-exist
- Highly nonlinear transistor buffer
  - Tens of thousands of transistors
  - Simultaneous Switching Operation (SSO) strongly affects driver timing (Power Supply Induced Jitter : PSIJ)
- Low Bit Error Rate (BER) requirement for (LP)DDR4
  - -DDR3 and earlier try to achieve 100% pass with a guard-banded (derating table) setup
  - -(LP)DDR4 admits random (unbounded) jitter, achieve BER ~=  $10^{-16}$  (\*1)
- Equalizer (FFE and/or DFE) requirement for DDR5

Conventionally: 100~1000 bit transient

Quick yet thorough design prediction becomes essential for complex/high-speed DDR systems

Now and future: convolution/superposition techniques and pure SPICE transient simulation should both be used



# **Analysis Flow for DDR**

To capture nonlinear, multi-lane and single ended system performance



# **Introduction to IBIS-AMI**

- IBIS-AMI: Algorithmic Modeling Interface
  - Complex waveform filters by programing languages (e.g. C/C++)
    - waveform in, waveform out
  - Interface with EDA tools (simulators)
  - A model consists of two files
    - Compiled runtime library (binary) file : \*.dll (windows), \*.so (unix)
    - Parameter control (text) file : \*.ami
  - IBIS-AMI flow requires channel analysis specific information
    - Unit Interval, Bit segment size, impulse response etc.







# Simulation technique comparisons (1: convolution)





# Simulation technique comparisons (2: superposition)



Methodology," DesignCon 2004



# Simulation technique comparisons (3: transient)



**SYNOPSYS**<sup>®</sup>

# **DDR Design Requires Configurable Testbench**

- Traditionally DDR designers:
  - -Used to use IBIS and/or transistor models for both Tx and Rx
  - -Used to use transient with relatively short bit length
- Current and upcoming DDR specs additionally requires:
  - -Complex equalization esp, Rx DFE
  - Requires statistically defined jitter (Rj) and BER down to 10<sup>-16</sup>



Transistors...

Switchable Simulation Engines:

Switchable Rx models: Resistor, IBIS, IBIS-AMI, Transistors..



# **Potential Analysis Flow for** DDR5



Superposition flow for long bit sequence

Edge pattern (e.g. pulse)

© 2018 Synopsys, Inc. 9

# **Capturing SSO in Eye Diagram Generation**

Create a Power Supply Induced Jitter (PSIJ) Distribution and Apply to Signal (DQ) Eye Diagram



# **Two Step Approach**

DQ/DQS Characterizations plus SSO Characterization



#### **SYNOPSYS**<sup>®</sup>

# Target System (\*1)

- DDR4 with 2667Mbps
- Simulate a single byte lane during a write operation
- Identical PRBS patterns to excite SSO effects. Then flip one bit to excite odd mode coupling on one of the bits.
- Minimal decoupling capacitor included
- 85mm of  $51\Omega$  stripline
- $60\Omega$  ODT to VDDQ



SYNOPSYS<sup>®</sup>

(\*1) John Ellis, "Capturing (LP)DDR4 Interface PSIJ and RJ Performance Accurately, Reliably and Quickly," track 4, DesignCon 2017



# **Challenges in SSO Noise Characterization**

SSO Translates to Timing Uncertainty

- SSO is input pattern dependent
- Stronger timing variation than voltage variation
- Power Delivery Network (PDN) has long time constant (deeper ISI)





# **SSO Noise Probability Density Function (PDF)**

PDN: Deep ISI, Relatively Linear Network  $\rightarrow$  Edge response superposition for SSO-PDF



SYNOPSYS

# **Translate Voltage Noise to Timing Jitter**





- Measure  $\delta \tau$  (with v.s. without noise) on Vout at Vref
- Compute  $\delta \tau / \delta V$ noise



**SYNOPSYS**<sup>®</sup>

# **Applying SSO Timing Jitter**



## **Correlation Study with Transient**





Good agreement between two methods

## **External Clock Extension for IBIS-AMI**

For DDR5





# **Proposal in JEDEC for DFE with DQS**

### 8.10 Rx Stressed Eye - Q3'18 Ballot #1848.18A Proposal

The stressed eye tests provide the methodology for creating the appropriate stress for the DRAM's receiver with the combination of ISI (both loss and reflective), jitter (Rj, Dj, DCD), and crosstalk noise. The receiver must pass the appropriate BER rate when the equivalent stressed eye is applied through the combination of ISI, jitter and crosstalk.



Figure 154 — Example of Rx Stressed Test Setup in the Presence of ISI, Jitter and Crosstalk

- (Rx) IBIS-AMI flow needs extensions
  - Take external clock for bit slicer
  - Take external clock in eye diagram generation

# **Potential Interface addition in IBIS-AMI**

- Use "double **\*clock\_times**" array
  - -Conventionally used to let the EDA tools know the CDR clock ticks (output)
  - -For DDR5, this array for the EDA tools to let IBIS-AMI model know the external clock ticks (input)

```
long AMI_GetWave (double *wave,
long wave_size,
double *clock_times,
char **AMI_parameters_out,
void *AMI_memory)
```

- Additional reserved parameter "External\_Clock"
  - -Has to be included in IBIS-AMI string when specified : (My\_DFE (External\_Clock True) (...))
  - -Let EDA tool prepare clock ticks stored in \*clock\_times array

# **Result 1: Correlated Jitter Case**

- Apply identical sinusoidal jitter (Sj) sequence to both DQ and DQS
- DQ has an Rx side DFE with (tap, weight) = (1, 0.02), (2, 0.01)





# **Result 2: Uncorrelated Jitter Case**

- Apply sinusoidal jitter (Sj) sequence with different frequency to DQ and DQS.
- DQ has an Rx side DFE with (tap, weight) = (1, 0.02), (2, 0.01)



 $\mathcal{X}_k$ 

-*d* 

 $\mathcal{V}k$ 

£

**Bit Slicer** 

# Conclusions

- Discussed about challenges and requirements for DDR4/5 designs
  - Combinational use of multiple methods would be essential
  - Comparison among multiple analysis engines and models
  - Potential flow for DDR5 to capture ISI/nonlinearity/crosstalk/SSO/Equalizer
- Demonstrated two step approach to take SSO effect in DDR analyses
  - -Generated SSO noise probability density
  - Determined Voltage noise to timing jitter translation factor
  - -Achieved good correlation between transient and edge response superposition methods
- Discussed IBIS-AMI enhancement to take external clock ticks
  - -External clock has to be taken into account both in DFE and in eye diagram generation





# Thank You

