DRAM Equalization for Next-Generation DDR Technologies

Randy Wolff

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Agenda

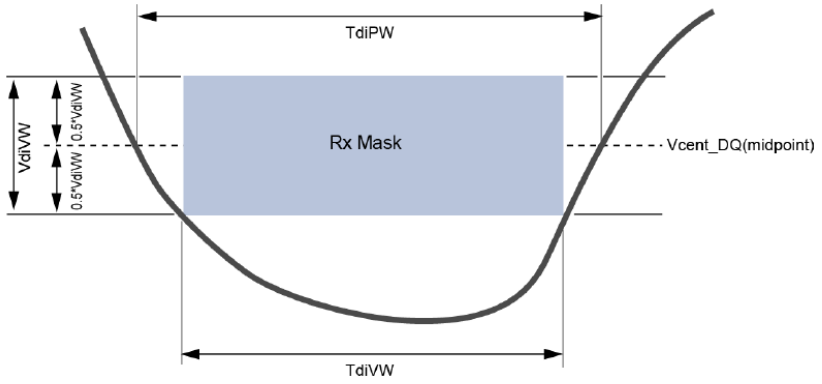
- Equalization in next-generation DRAM
- JEDEC BER requirements
- Non-linearities in IBIS-AMI simulations
- Channel characterizations
- Example IBIS-AMI simulation
- IBIS-AMI model support
- Wrap-up

Equalization in Next-Generation DRAM

- DDR systems are implementing equalization techniques in DRAM and controllers to improve SI at higher data rates
  - DDR4 @ 3200 Mbps
  - DDR5 @ 4000+ Mbps
  - GDDR6
- Many controllers have implemented TX FFE and RX CTLE in DDR4
- DRAM may have vendor-specific implementations of CTLE and/or DFE in DDR4 and JEDEC-specified DFE in DDR5
- IBIS-AMI or AMI-like simulation techniques may be needed to include equalization in simulation results

Are SerDes Analysis Techniques Required by JEDEC?

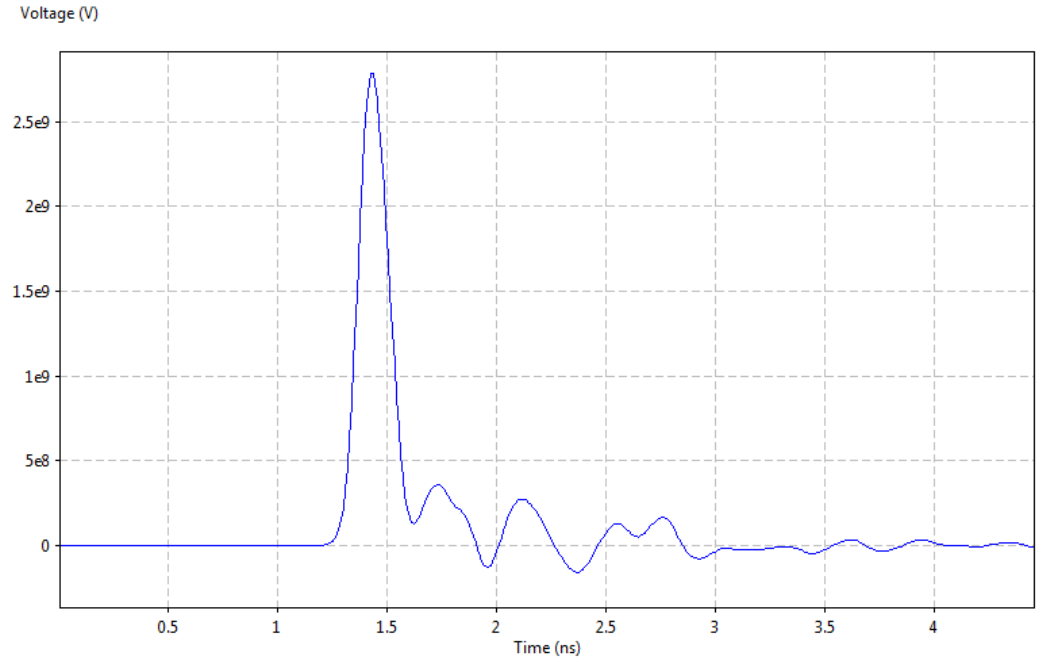
- Some confusion exists about BER definitions in the DDR4 JEDEC spec
  - JEDEC: “The input buffer design specification is to achieve at least a BER = E-16 when the RxMask is not violated. The BER will be characterized and extrapolated if necessary using a dual-Dirac method from a higher BER (tbd).”
  - The BER is from the DRAM, not System perspective.
  - This does not mean the system needs to be simulated to 1E-16 BER
- What BER do you need to simulate to? Depends on your system requirement.
- Low BER modeling not enabled in DDR4, since RJ not defined for DRAM
  - May change with RJ spec’d for DDR5



Capturing Non-linearities in IBIS-AMI Simulations

- AMI simulation will characterize a channel (typically with a rising step response) to create an impulse response (IR)
- What non-linearities can be captured in the IR?
  - Non-linear I-V of on-die termination and output driver
    - Only ringing characteristics of 0-to-1 transition, not 1-to-0 transition
  - Non-linear characteristics of pulldown to pullup transition captured in IBIS [Model] V-t waveform

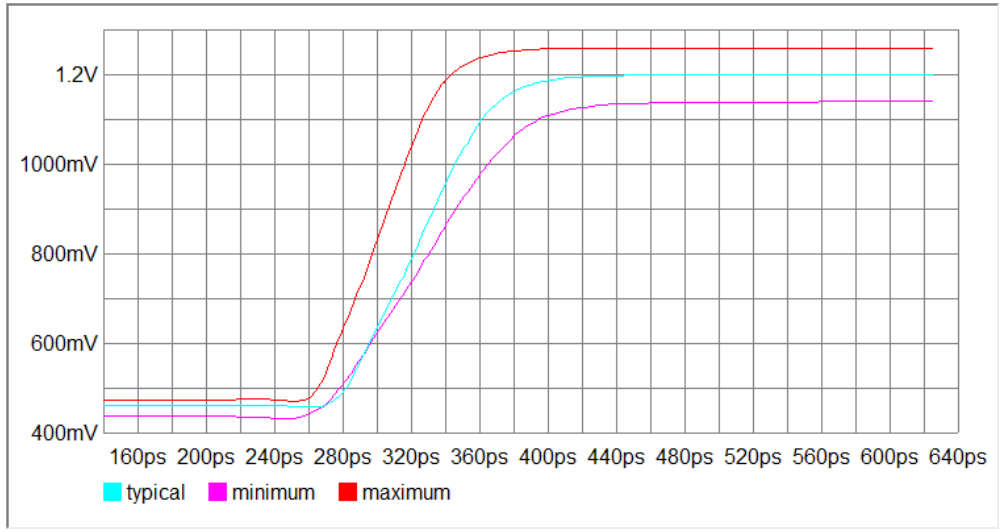
2-DIMM 1-rank DDR4 channel Impulse Response

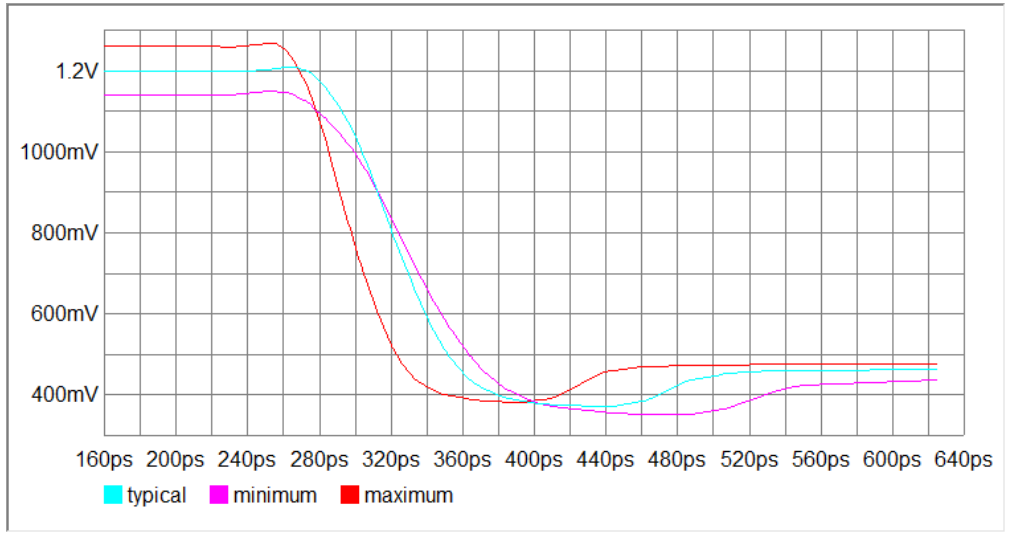


Capturing Non-linearities

- Which non-linearities are not captured with rising step response?
  - Imbalanced pulldown/pullup behavior
  - Overshoot characteristics of pulldown (not actual pre-emphasis), so can't be modeled as FFE
  - SSO noise effects that may add significant jitter and voltage margin degradation

Imbalanced Pullup/Pulldown Transition Behavior



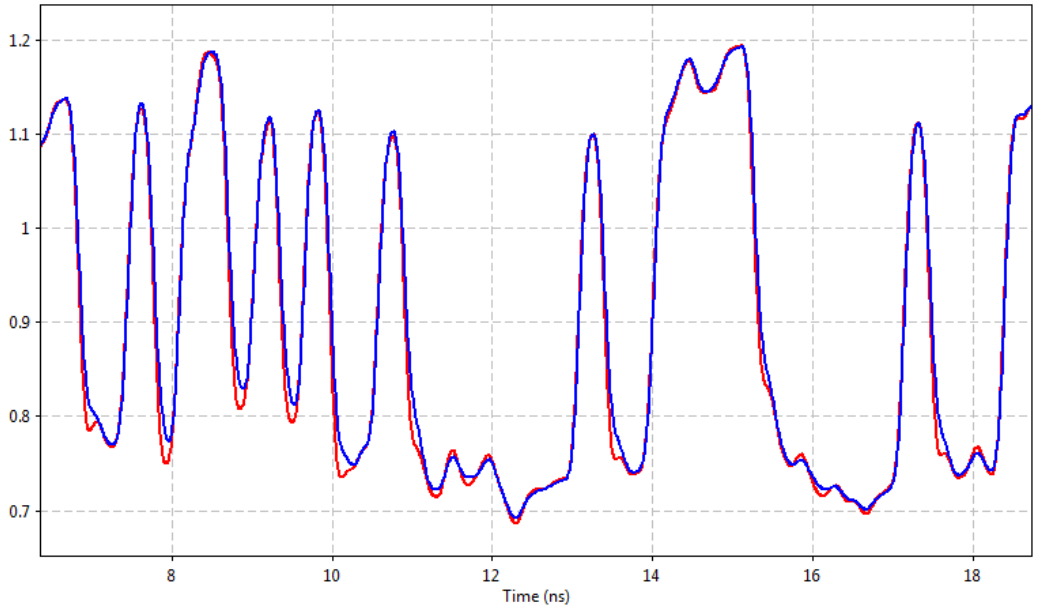


Channel Characterization Options

- Time Domain waveform from rising step channel characterization shown on right
- Mismatch seen in 0's
- Other options may be available in simulators
  - Rise/fall
  - PRBS
  - ?

Blue –Channel simulation

Red – IBIS time domain simulation

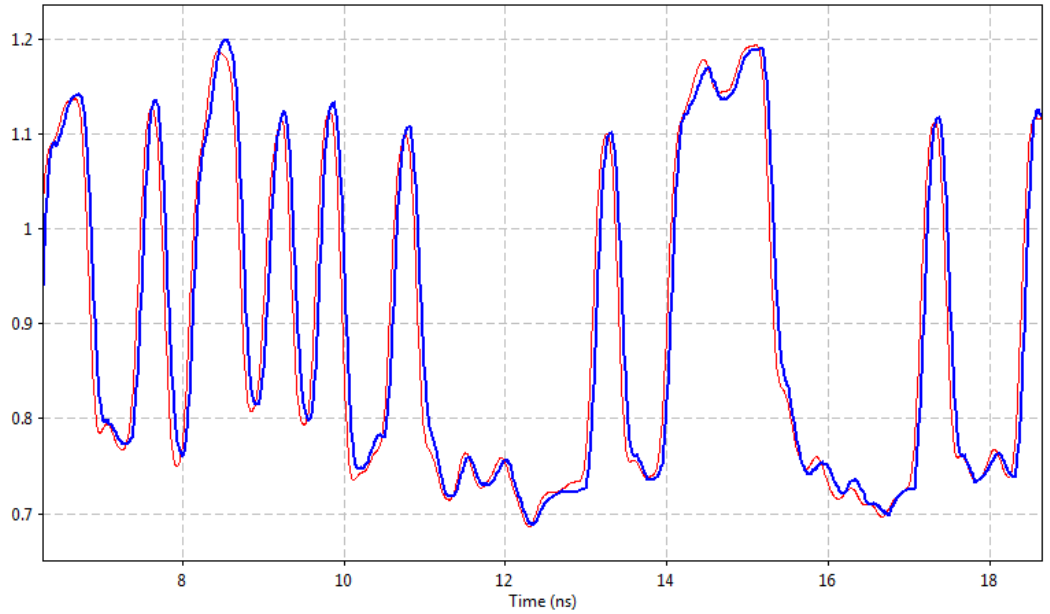


Channel Characterization Options

- PRBS-based channel characterization with same stimuli as time domain
- Shows some improvement in 0's
- What correlation is acceptable?
  - TBD

Blue –Channel sim

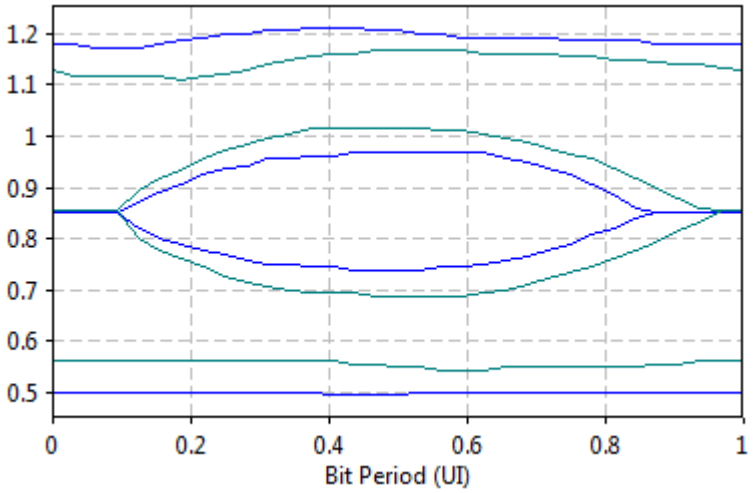
Red – IBIS time domain sim



Example IBIS-AMI Simulation with DFE

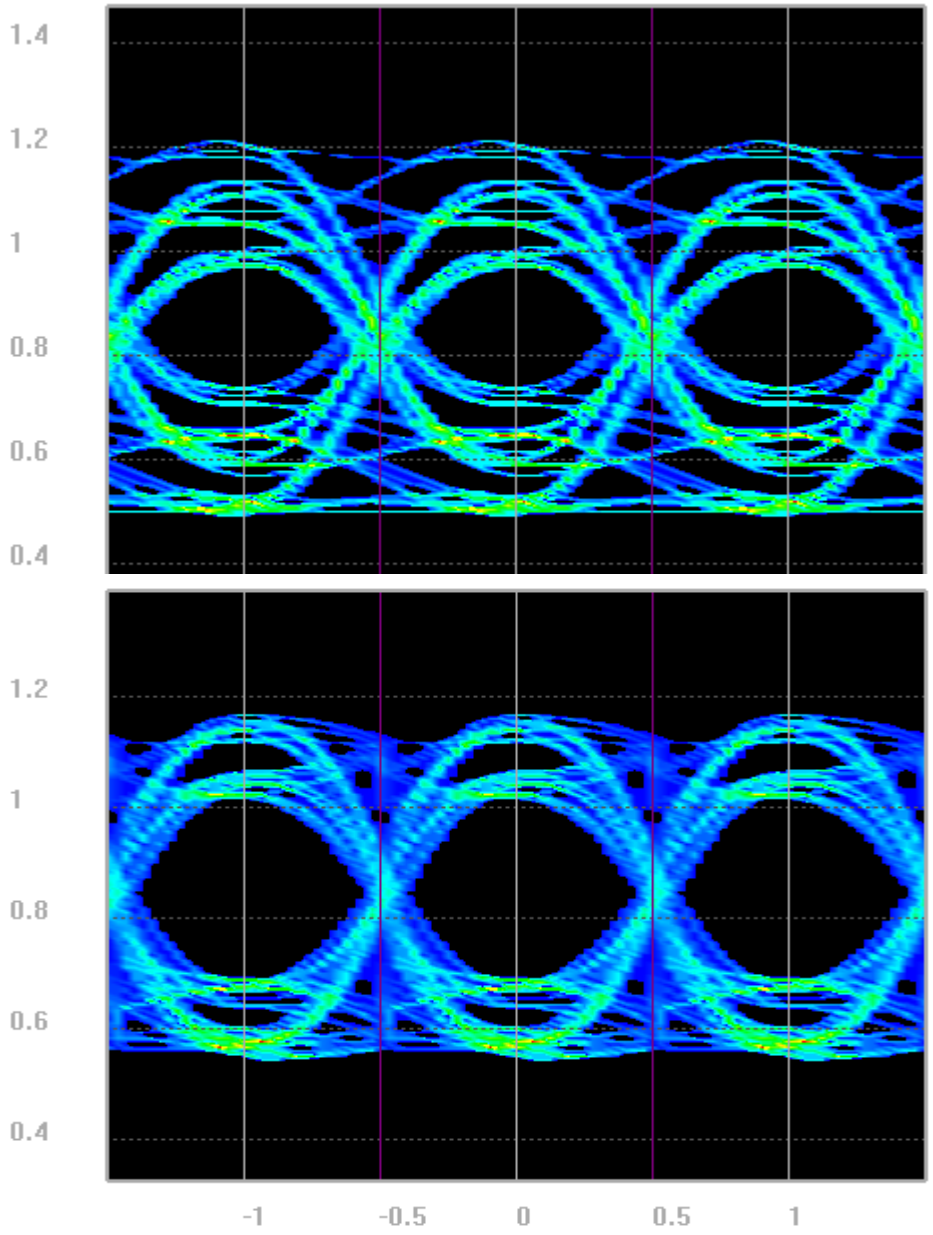
- 2-DIMM, 1-rank @3200 Mbps
- Non-optimized termination to increase reflections
- IBIS-AMI model of 3-tap DFE improves eye height from 0.218mV to 0.317mV (+99mV)

Eye Contour plots



No DFE

3-tap DFE



IBIS-AMI Modeling Support

- IBIS-AMI models for DRAM equalization have limited support
  - Two EDA vendors supporting IBIS-AMI for DDR simulation
  - Some EDA vendors supporting AMI-like channel simulation flows with non-AMI custom solutions
  - Some EDA vendors supporting traditional IBIS simulation flows for DDR simulation with equalization post-processing techniques

Wrap-up

- Equalization techniques used in SerDes interfaces have come to single-ended signaling interfaces
- Multiple simulation techniques may be needed to characterize non-linear effects seen in single-ended signals (SSO)
  - Traditional time domain and IBIS-AMI type
- What do DRAM and controller vendors do now to support DDR system simulations?
  - May need to support IBIS-AMI, IBIS, and custom models for each customer based on the EDA software they use
  - Deja-vu of IBIS-AMI for SerDes circa 2007
  - Continuing dialog needed between model creators, EDA vendors, and system designers to enable a better solution


Micron