



IBIS Open Forum Minutes

Meeting Date: **February 2, 2018**

Meeting Location: **DesignCon 2018 IBIS Summit, Santa Clara, CA, USA**

VOTING MEMBERS AND 2018 PARTICIPANTS

ANSYS	Curtis Clark
Applied Simulation Technology	(Fred Balistreri)
Broadcom	(Yunong Gan)
Cadence Design Systems	Brad Brim, Ken Willis*, Ambrish Varma*
Cisco Systems	Stephen Searce*, Cassie Yan*, Baosh Xu*
CST	Stefan Paret*
Ericsson	Anders Ekholm*, Zilwan Mahmod*, Guohua Wang*
GLOBALFOUNDRIES	Steve Parker*
Huawei Technologies	(Hang (Paul) Yan)
IBM	Greg Edlund*
Infineon Technologies AG	(Christian Sporrer)
Intel Corporation	Hsinho Wu*, Michael Mirmak*, Nilesh Dattani*
	Fernando Mendoza Hernandez*, Varun Gupta*
	Subas Bastola*, Hansel Dsilva*
IO Methodology	Lance Wang*
Keysight Technologies	Radek Biernacki*, Ming Yan*, Heidi Barnes*
	Pegah Alavi*
Maxim Integrated	Joe Engert*, Yan Liang*
Mentor, A Siemens Business	Arpad Muranyi*, Weston Beal*, Raj Raghuram*
	Carlo Bleu*, Mikael Stahlberg*, Yasushi Kondou*
	Vladimir Dmitriev-Zdorov*
Micron Technology	Randy Wolff*, Justin Butterfield
NXP	(John Burnett)
Qualcomm	Kevin Roselle*, Tim Michalka*
Raytheon	Joseph Aday*
SiSoft	Mike LaBonte*, Walter Katz*, Todd Westerhoff*
Synopsys	Ted Mido*, Adrien Auge, Scott Wedge*
Teraspeed Labs	Bob Ross*
Xilinx	Ravindra Gali*
ZTE Corporation	(Shunlin Zhu)
Zuken	Michael Schaeder*, Takayuki Shiratori*

OTHER PARTICIPANTS IN 2018

Google	Zhiping Yang*
Haskware	David Banas*

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KEI Systems
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Kazuki Murata*
Kenichi Higashiura*, Hiroyuki Motoki*
(Jose Godoy)
Ron Olisar*
Megumi Ono*
Wei-hsing Huang*
Tom Lee*
Yasuki Torigoshi*, Yoshinori Fukuba*

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
February 16, 2018	624 227 121	IBISfriday11

For teleconference dial-in information, use the password at the following website:

<http://tinyurl.com/y7yt7buz>

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting.

NOTE: "AR" = Action Required.

OFFICIAL OPENING

The IBIS Open Forum Summit was held in Santa Clara, California at the Santa Clara Convention Center, during the week of the 2018 DesignCon conference. About 61 people representing 32 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

<http://www.ibis.org/summits/feb18/>

Mike LaBonte welcomed everyone to the Summit, opening the meeting at 8:30 a.m. He noted there were 18 presentations mentioning IBIS during the DesignCon conference. He thanked the

sponsors Cadence Design Systems, Keysight Technologies, Mentor, a Siemens Business, and Synopsys for offsetting the cost of food and audio-visual equipment.

IBIS UPDATE

Mike LaBonte (SiSoft)

Mike LaBonte noted there are 26 members of the IBIS Open Forum currently. There have been 499 Open Forum meetings so far. Task groups meet weekly. The IBIS 7.0 specification is in development, and he proposed a timeline for 7.0 ratification. Two BIRDs need to be finished and voted on before the specification can be finalized.

IBIS-ATM TASK GROUP REPORT

Arpad Muranyi (Mentor, a Siemens Business)

Arpad Muranyi noted that the ATM task group has been using some of its time to facilitate Interconnect task group discussions on BIRD189. Arpad showed a list of BIRDs that were accepted and rejected in the last year and some BIRDs that are expected to be rejected. Other pending BIRDs are in discussion.

IBIS INTERCONNECT TASK GROUP REPORT

Michael Mirmak (Intel Corporation)

Michael Mirmak introduced the Interconnect proposal started by the task group in 2014. BIRD189.5 is in the final stages of preparation. The BIRD adds support for IBIS-ISS and Touchstone models of passive interconnect in packages and on-die. Michael reviewed the new keywords. Grouping provides a lot of flexibility for organizing interconnect models. One key change in the latest draft addresses victim/aggressor crosstalk concepts. Some models may include pins that do not include all their crosstalk aggressors from the physical device. A terminal declaration as A_gnd was introduced to allow a terminal to connect to simulator node 0.

Ken Willis asked if you can have redundant single line and coupled line models in the same model. Michael replied that you can.

Arpad Muranyi noted there is a 1:1 pin to buffer assumption for signal pins. For power pins, you can have multiple forks and joins.

Heidi Barnes asked if A_gnd is a reserved name, what happens if you import a netlist using that name. Michael responded that it is used in the terminal declaration section, so A_gnd is only in the IBIS file and declares the terminal is connected to node 0. Walter Katz added there was a lot of discussion about node 0. If not doing power aware simulations, it does not matter. If doing power aware simulations, it also does not matter if you are doing ground referenced simulations. If you want VSS to float, then A_gnd in any subcircuits can cause problems.

Tim Michalka asked if you can branch a signal such as in a dual-die DRAM. Walter clarified that this is currently done in EBD, and an EMD language will be developed next to take care of this. Arpad added that the signal cannot split in the current proposal.

Greg Edlund stated that once the BIRD is passed, he would like to help work on test cases.

Walter commented that a key point is you don't have to rewrite models. Models generated today are just wrapped for IBIS. He noted you may use one tool to generate on-die interconnect models and another tool for generating package models. You can put these into separate sets. One important use of groups is to handle corner cases. Typ/min/max is not relevant in package modeling, so groups can be labeled with specific corner case definitions.

EFFECTIVE SIMULATION SET UP WITH LATEST IBIS MODELS – COOPERATION WITH IEC 63055/IEEE 2401

Yoshinori Fukuba*, Kazuki Murata** (*Toshiba, **Ricoh)

Yoshinori Fukuba noted that collaboration with IBIS will shorten development time for LSI Package Board (LPB) modeling. LPB is a format for interoperable design. The standard describes each part of the information exchange enabling models to be connected facilitating a system level simulation. LPB is developed within JEITA. Cooperation between IBIS and LPB started in 2013.

Kazuki Murata discussed technical aspects of LPB. Simulation time has been shortened by improved software and computer calculations. Setups and parameter collection can still take a long time. Connecting pins between models can take a long time when automated methods fail. LPB contains information about physical positions of pins to aid in pin matching. The data is in XML format. Modifications made during the design and development phase can lead to wasting time when setting up new simulations. Once you setup simulations by using LPB, you can reuse setup data.

LPB files should be released by component vendors. Kazuki demonstrated a tool used to create a LPB file for a DRAM package. When die pad information is available in IBIS 7.0, LPB die modules may be available. LPB needs to be updated to support new IBIS syntax.

Yoshinori proposed for the future to establish joint efforts for harmonization between the latest IBIS and IEEE 2401. IEEE-SA members may join the P2401 work on the IEEE 2401-2020 standard.

Walter Katz clarified that in BIRD189, it is made clear how not to double count package models with new and legacy package models. It is up to the EDA tool to determine which package model to use. IBIS needs to add a new section giving the x-y location of each pin to help provide information for LPB. For a flip chip package, a section could be added to describe x-y locations for ball pad locations. Mapping of signal names becomes difficult when die and package and board designers use different tools.

GO BIG OR GO HOME: THE FIRST TRANSATLANTIC TELEGRAPH CABLE AND THE BIRTH OF ELECTRICAL ENGINEERING

Tom Lee (Stanford University)

Mike LaBonte introduced Tom Lee by displaying his biography. Tom joined Stanford in 1994. He has extensive academic accomplishments, several awards, and significant industrial experience. Tom holds over 60 patents and has authored textbooks. He owns many oscilloscopes and electronic components.

Tom's biography and abstract are uploaded. Per Tom's request, the presentation itself is not publicly distributed because it is used in many other settings and for student orientation. Tom's abstract plus some additional details are presented here.

"Abstract: Electrical engineers are the children of a failure so traumatic that we don't even talk about it. American paper magnate Cyrus West Field wanted to span the Atlantic in the 1850s with a telegraph cable; it was the Victorian era's equivalent of shooting for the moon. Amplifiers would not exist for another half-century, so success would require mastery of a number of complex technical disciplines. Regrettably, the project's technical head was a medical doctor. A British board of inquiry convened to assess the resulting failures noted that the electrical arts lacked even a basic vocabulary to describe the failure. William Thomson was eventually named the new head of the project, and final success followed in 1866. The volt, ohm and ampere were formally defined shortly thereafter and the profession of electrical engineering was born. Thomson -- arguably the first professional electrical engineer -- became Lord Kelvin, and EEs have been busy making mischief ever since."

Tom added many interesting details. Based on Moore's law, many transistors now support five million cell phones sold daily. This contributes to producing 100 TPA every year (100 transistors per ant on earth annually). The story of the transatlantic cable reveals that the secret to Greatness is a function of Money, Ignorance, Luck, and Craziness, as expressed in the formula $G = f\{M,I,L,C\}$. In the path to greatness, Murphy's law also seems to prevail. Luck may also prevail as new technologies emerge at convenient times.

One technology was the discovery of Gutta-Percha, a natural substance from trees mainly in Singapore/Malaysia. It is a thermoplastic, chemically stable, and has tolerance of water. This was useful to protect the cable from corrosion. Another key technology was the highly sensitive mirror galvanometer by Lord Kelvin to detect small voltages. Magnets canceled out the earth's magnetic field.

The transmission data rate target for the transatlantic cable was 1-2 words per minute, but the first cable in 1857/1858 achieved only 0.1 words per minute. Many problems arose, and the cable went silent after 23 days. It took 16 hours to transmit a 98-word message perhaps with the operator using context to fill in the somewhat garbled transmission. Perhaps this was a first application of what would be done today by artificial intelligence. After much debate, a new, heavier cable was proposed. However, it required a five times bigger ship than had currently existed to lay it. As luck would have it, a new class of ships were being constructed to hold enough fuel to travel non-stop from England to Australia.

The overall cable properties were length of 3000 nautical miles, series resistance of 8 kohms, shunt capacitance of 740 uF, and shunt resistance of 200 kohms. This provided an RC time constant of 6 seconds. Five words per minute could be transmitted, exceeding the original target. The cable snapped several times before finally being placed in service in 1866. By 1891, more cables formed a global communications network.

Many legacies emerged from Cyrus West Field's initial money, ignorance, luck and craziness. They include the unit of resistance, the electrical engineering profession emerging as the Institution of Electrical Engineers, and several EE degree programs at universities in the 1880s. The cable descendants include networks that contribute to 250,000 texts per second.

The full story of successes and failures illustrates all aspects of the bottom line: "May you always have as much MILC as you need."

SUBCIRCUITS, S-PARAMETERS AND T-LINE MODELS: WHY AND HOW WE SET REFERENCES

Vladimir Dmitriev-Zdorov (Mentor, a Siemens Business)

Vladimir Dmitriev-Zdorov presented some not well known facts about S-parameters. There are two important moments with S-parameters. The first is how the ports are defined when measured. The second is how the terminals are used when simulated. With S-parameter models, ports are electrically isolated. Inter-port relations are established by controlled sources. S-parameters can properly represent subcircuits if they are properly created and used. Grounding S-parameter ports is ok but should not be overdone. In many cases, S-parameters require connection to global references in places where it didn't exist in the prototyped objects. Some S-parameters have no grounded terminals. Exposing ports for a DC-blocking capacitor in a channel model requires specific grounding of one terminal of the capacitor.

Bob Ross asked about slide 10, if both sides need a ground connection. Vladimir confirmed the two grounds are needed and are sufficient for the circuit.

USING IBIS-AMI IN COM ANALYSIS

Wei-hsing Huang (SPISim)

Wei-hsing Huang described the motivation to create an open source link-analysis platform to shorten the IBIS-AMI modeling design cycle. Channel Operating Margin (COM) is a simplified version of BER analysis for figure-of-merit based channel optimization and analysis. COM analysis uses exhaustive search for FFE and CTLE optimization. DFE is optimized separately.

The COM flow can be modified to use IBIS-AMI models. It is easier if AMI_Init is available for the TX and RX. GetWave can be used by first convolving the single bit response with a bit stream. He showed an example of replacing a COM FFE with a self-optimization FFE.

An AMI parser is not necessarily needed. The flow can also be used for back-channel analysis development.

Michael Mirmak commented that COM is for checking of meeting the specification and IBIS-AMI is used to get designs better than the specification. He asked what is the best purpose for this tool. Wei-Hsing noted the tool is useful for understanding the AMI flow. If someone is a system designer, they can budget crosstalk or TX/RX solution space. One can use COM as figure of merit for AMI model optimization.

Walter Katz noted the intent of COM was to eliminate simulation originally. COM represents the best an AMI model can do. One can use an AMI model measured at the center of the eye and optimize to get the same result as COM analysis.

ADDRESSING DDR5 DESIGN CHALLENGES WITH IBIS-AMI MODELING TECHNIQUES

Todd Westerhoff, Doug Burns, Eric Brock (SiSoft)

Todd Westerhoff noted that DDR has evolved to require less attention to skews in the system, assuming that the controller takes care of timing alignment. AMI models were designed around SerDes channels, and DDR channels are very different. To begin looking at AMI simulation techniques for a DDR5 system, Todd started with a DDR4 2-DIMM system. One topology acts as many different nets, with four defined read and write transactions. Simulations were completed to optimize the terminations and drive strengths on the four DRAM and the controller. Data rate was swept in 400 MT/s increments from 3200 to 6400 MT/s. It turned out that the margin at 4400 MT/s was much better than at 3600 MT/s. Plotting aligned pulse responses made it easy to see that ISI was peaking at sample times for the 3600 MT/s case versus the 4400 MT/s case.

Todd created an IBIS-AMI model to look at the effects of using a multi-tap DFE in the DRAM RX to open up the eye. He used an adapting DFE to approximate the training a controller would do then locked the settings once "Ignore_Bits" was reached. The adapting DFE model approximated the optimally trained fixed-tap model well. Locking the clock in a typical AMI model approximated a forwarded clock behavior. Todd noted that the presentation only covered part of the full methodology needed for DDR5 analysis.

Ambrish Varma stated that Todd didn't talk about non-linearities in rise/fall edge asymmetry. Todd replied this is early in the analysis of what is important to model in DDR5.

A question was asked if the 4400 MT/s vs. the 3600 MT/s difference was specific to the topology shown. Todd responded yes.

DRAM EQUALIZATION FOR NEXT-GENERATION DDR TECHNOLOGIES

Randy Wolff (Micron)

Randy Wolff noted that DDR systems are implementing equalization techniques in DRAM and controllers to improve SI. Methods such as IBIS-AMI simulation are needed to include the effects of equalization in simulations. He clarified some confusion relative to the DDR4 JEDEC specification about BER definitions and noted there are no JEDEC requirements for simulating to low BER. However, low BER simulation may be more relevant in DDR5. Randy described some issues with capturing non-linearities inherent in DDR systems when doing AMI simulations. Some simulators may have options to better capture the effects of non-linearities. He showed results of simulating a DDR system including a 3-tap DFE in the DRAM RX. IBIS-AMI models are currently supported in only two simulators. Continuing dialog is needed between model creators, EDA vendors, and system designers to enable a better solution for equalization modeling in single-ended signaling systems.

Arpad Muranyi asked what is needed from models and simulators to support DDR5. Randy responded that multiple approaches may be necessary such as time-domain simulation to capture non-linearities such as SSO effects as well as AMI-like simulations to see the effects of equalization and simulate to low BER including RJ effects.

Ambrish Varma noted that IBIS-AMI currently supports both differential and single ended signals.

Walter Katz stated that AMI processing assumes use of an impulse response and an LTI system. DDR systems are not so linear due to reflections. We may decide that AMI needs to be able to process two impulse responses to better deal with rise/fall mismatches in the TX. Also, a controller will have its own unique equalization requirements beyond what is specified for the DRAM.

Ken Willis noted that DDR5 will go up to 6.4 GT/s. He asked if the systems will start to approximate SerDes channels to hit these speeds. Randy commented that this is expected to be the trend and is already seen in graphics DRAM designs operating at faster speeds but are more point-to-point topologies.

DDR5 EQUALIZATION OPTIONS WITH IBIS

Arpad Muranyi (Mentor, a Siemens Business)

Arpad Muranyi looked at a case study of using non-IBIS AMI models for DDR5 analysis. He noted that more Verilog-A models are being released by model makers, and most EDA vendors support Verilog-A. Arpad created a Verilog-A model for a data buffer that included a clock input allowing an integrated DQS signal to clock the model. He showed some code snippets implementing a DFE. The Verilog-A model was simulated with a traditional time domain simulator. These results were compared to an IBIS-AMI-like statistical simulator as a reference. The results of the DFE modeling compared well between the two simulations. The IBIS Verilog-A simulation time is comparable to normal IBIS simulations and grows proportionally with the number of bits simulated.

Arpad then added a PDN model to introduce significant non-linear effects into the simulation. The time domain simulation captured the non-linear effects much better than the IBIS-AMI-like statistical simulator. This happens because channel characterization is a snapshot of the channel's behavior at a certain time. He noted that Verilog-A models are not limited to modeling DFE. Arpad questioned the need for multi-million bit simulations due to the length of bit streams in DDR systems.

Arpad stated that IP protection might be required for equalization models. Verilog-A models can be encrypted, but the encryption is simulator specific.

Ambrish Varma commented that he has done silicon correlation with AMI models. Isn't it too early to dismiss IBIS-AMI modeling? Nitin Bhagwath said that IBIS-AMI is also not the standard, so it is important to look at other options. Arpad stated it could be possible to address more non-LTI effects in the AMI specification, but how long do we wait. Arpad added you might not have to simulate millions of bits if you use worst case bit stream analysis.

Greg Edlund asked how difficult it was to implement the code to clock the data with DQS. Arpad replied it is very easy to implement this in code.

IEEE P370 TOUCHSTONE DATA: HEADER/COMMENT INFORMATION (AD HOC PRESENTATION)

Jim Nadolny (Samtec)

[Presented by Heidi Barnes (Keysight Technologies)]

Heidi Barnes noted that many people get S-parameters that behave poorly in simulation. IEEE P370 has focused on developing a header for Touchstone files that includes information on date of measurement, fixture removal de-embedding method, port mapping, and quality metrics. Heidi asked if some of this information could be integrated into Touchstone 2.0.

Michael Mirmak asked if Touchstone is a data file format only, would the pin information be better in an external file. Heidi responded that she thinks the pin information is critical and needs to be in the file. Anders Ekholm commented that he thinks this information should be in the files, and not as comments.

Walter commented that Touchstone 2.0 has not been adopted very successfully due to the requirement to parse keyword information. Walter recommended including the information as comments so existing readers don't have problems. Walter noted this should only be for measurements of passive interconnect.

Michael asked if someone from P370 could attend the Interconnect task group meeting to present the information. Heidi responded she would invite a representative to attend an IBIS meeting.

IBIS-AMI POST-SIMULATION ANALYSIS

Mike LaBonte, Todd Westerhoff (SiSoft)

Mike LaBonte noted IBIS has supported post-processing such as modeling receiver behavior through measurement levels. IBIS 5.0 included more information for IBIS-AMI modeling such as clock times to process in the EDA tool. Many post-processing methods are not specified by IBIS such as eye metrics, random function seeds, and BER calculation. Without specifying post-processing methods, tools can produce different results for the same analysis. This can be inconsistent with user expectations.

Mike proposed support for specifying methods for eye height measurement and the seed for clock jitter modeling. He showed an example of two methods for accumulating the eye diagram that give very different results. Eye height could also be measured differently if one uses the actual clock times or ignores the clock.

There are also requests for more FEC support in IBIS-AMI. The requests relate to behaviorally modeling FEC gain. Mike proposed helping models report post-processing results. For example, an RX model could calculate FEC gain and pass simulation outputs to a new

AMI_Report function. This could output HTML code that would be displayed by the simulator.

Mike summarized that some portability issues are actually due to differences in post-process implementation.

Walter Katz commented that for post-processing, if IBIS could agree upon methods for displaying eye diagrams, not to make them AMI parameters, these could be choices for the EDA tool to give the user a choice on. For FEC gain, the reporting would be a trivial change. If a GetWave call is 0 long, it could be a key to generate reports they want to do again. We have a DLL_ID, so it could be a base file name for generating outputs in HTML format. We could give the model maker simple tools to do what they want. Mike noted adding the AMI_Report function sounds like a big change, but you could barely specify what it does.

Arpad Muranyi commented we should agree on how it should be done and put it in the specification instead of having so many options. He sees the clock ticks as how the waveform should be displayed. Arpad encouraged model makers to look at clock ticks more seriously, since he has seen many models where the clock ticks are bogus and not meaningful. Ken Willis stated it is a good idea for the tool to have the option to ignore clock ticks. Arpad added that the assumption in the EDA tool about the CDR may not be right. Mike noted it may be that the ignore_bits are too short and the CDR hasn't locked yet.

Michael Mirmak commented it might be nice to have eye height and width in the specification so the model author says how to look at the data. Mike noted that when doing statistical analysis, how do you look at the eye without a clock placement. Michael added it would be good to tell model makers if there is information they should really be providing because the real silicon does.

Arpad commented that it might be time to revisit specifying an eye mask. This has been discussed before.

Mike noted it would be faster to get information in models if there was a method in IBIS not requiring IBIS to add keywords.

Walter commented that most standards define how measurements should be made. Ken noted that some IP providers might comply with something different (better) than the standard. Michael added that you could have an evaluation selector for an IP used in multiple situations to have spec-defined or IP-specific requirements. Arpad stated that if we don't want to put the eye mask definition itself into the specification, we could define a parameter/keyword which is a pointer to a mask definition of a specific standard such as USB.

CONCLUDING ITEMS

Mike LaBonte again thanked the sponsors Cadence Design Systems, Keysight Technologies, Mentor, a Siemens Business, and Synopsys, the presenters, organizers and attendees.

The meeting concluded at approximately 3:50 PM.

NEXT MEETING

The next IBIS Open Forum teleconference meeting will be held February 16, 2018. The following IBIS Open Forum teleconference meeting is tentatively scheduled on March 9, 2018.

NOTES

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This meeting was conducted in accordance with ANSI guidance.

All inquiries may be sent to info@ibis.org. Examples of inquiries are:

- To obtain general information about IBIS.
- To ask specific questions for individual response.
- To subscribe to the official ibis@freelists.org and/or ibis-users@freelists.org email lists (formerly ibis@eda.org and ibis-users@eda.org).
- To subscribe to one of the task group email lists: ibis-macro@freelists.org, ibis-interconn@freelists.org, or ibis-quality@freelists.org.
- To inquire about joining the IBIS Open Forum as a voting Member.
- To purchase a license for the IBIS parser source code.
- To report bugs or request enhancements to the free software tools: ibischk6, tschk2, icmchk1, s2ibis, s2ibis2 and s2iplt.

The BUG Report Form for ibischk resides along with reported BUGs at:

<http://www.ibis.org/bugs/ibischk/>
<http://www.ibis.org/bugs/ibischk/bugform.txt>

The BUG Report Form for tschk2 resides along with reported BUGs at:

<http://www.ibis.org/bugs/tschk/>
<http://www.ibis.org/bugs/tschk/bugform.txt>

The BUG Report Form for icmchk resides along with reported BUGs at:

<http://www.ibis.org/bugs/icmchk/>
http://www.ibis.org/bugs/icmchk/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

<http://www.ibis.org/bugs/s2ibis/bugs2i.txt>
<http://www.ibis.org/bugs/s2ibis2/bugs2i2.txt>
<http://www.ibis.org/bugs/s2iplt/bugspl.txt>

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

<http://www.ibis.org/>

Check the IBIS file directory on [ibis.org](http://www.ibis.org) for more information on previous discussions and results:

<http://www.ibis.org/directory.html>

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SAE STANDARDS BALLOT VOTING STATUS

Organization	Interest Category	Standards Ballot Voting Status	December 15, 2017	January 5, 2018	January 26, 2018	February 2, 2018
ANSYS	User	Active	X	-	X	-
Applied Simulation Technology	User	Inactive	-	-	-	-
Broadcom Ltd.	Producer	Inactive	-	-	-	-
Cadence Design Systems	User	Active	X	-	X	X
Cisco Systems	User	Inactive	-	-	-	X
CST	User	Inactive	-	-	-	X
Ericsson	Producer	Inactive	-	-	-	X
GLOBALFOUNDRIES	Producer	Active	-	-	X	X
Huawei Technologies	Producer	Inactive	-	-	-	-
IBM	Producer	Inactive	-	-	-	X
Infineon Technologies AG	Producer	Inactive	X	-	-	-
Intel Corp.	Producer	Active	X	X	X	X
IO Methodology	User	Active	-	X	X	X
Keysight Technologies	User	Active	-	X	X	X
Maxim Integrated	Producer	Inactive	-	-	-	X
Mentor, A Siemens Business	User	Active	X	X	-	X
Micron Technology	Producer	Active	X	X	X	X
NXP	Producer	Inactive	-	-	-	-
Qualcomm	Producer	Inactive	-	-	-	X
Raytheon	User	Inactive	-	-	-	X
SiSoft	User	Active	X	X	X	X
Synopsys	User	Active	X	X	X	X
Teraspeed Labs	General Interest	Active	X	X	X	X
Xilinx	Producer	Inactive	-	-	-	X
ZTE Corp.	User	Inactive	X	-	-	-
Zuken	User	Inactive	X	-	-	X

Criteria for SAE member in good standing:

- Must attend two consecutive meetings to establish voting membership
- Membership dues current
- Must not miss two consecutive meetings

Interest categories associated with SAE standards ballot voting are:

- Users - members that utilize electronic equipment to provide services to an end user.
- Producers - members that supply electronic equipment.
- General Interest - members are neither producers nor users. This category includes, but is not limited to, government, regulatory agencies (state and federal), researchers, other organizations and associations, and/or consumers.