**IBIS Summit at DesignCon 2018**

February 2, 2018 **Agenda**

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| 08:00 | **REFRESHMENTS AND SIGN IN** |
| 08:30 | **WELCOME AND INTRODUCTIONS** Mike LaBonte (SiSoft) |
| 08:45 | **IBIS Update** Mike LaBonte (SiSoft) |
| 09:00 | **IBIS-ATM Task Group Report** Arpad Muranyi (Mentor, a Siemens Business) |
| 09:10  | **IBIS Interconnect Task Group Report** Michael Mirmak (Intel Corporation) |
| 09:30 | **Effective Simulation Set Up with Latest IBIS Models - Cooperation with IEC 63055 / IEEE 2401** \*Yoshinori Fukuba, \*\*Kazuki Murata (\*Toshiba, \*\*Ricoh)[Presented by Yoshinori Fukuba (Toshiba)] |
| 10:05 | **BREAK, REFRESHMENTS (15 Minutes)** |
| 10:20 | **Go Big or Go Home: The First Transatlantic Telegraph Cable and the Birth of Electrical Engineering** Thomas Lee, Stanford University |
| 11:05 | **Subcircuits, S-parameters and T-line models: Why and How We Set References** Vladimir Dmitriev-Zdorov (Mentor, a Siemens Business) |
| 11:30 | **Using IBIS-AMI in COM Analysis** Wei-hsing Huang (SPISim) |
| 12:00 | **FREE LUNCH (Pre-registration required, 60 minutes))** |
| 13:00 | **Addressing DDR5 Design Challenges with IBIS-AMI Modeling Techniques** Todd Westerhoff, Doug Burns, Eric Brock (SiSoft) [Presented by Todd Westerhoff (SiSoft)] |
| 13:30 | **DRAM Equalization for Next-Generation DDR Technologies** Randy Wolff (Micron Technology) |
| 13:50 | **DDR5 Equalization Options with IBIS** Arpad Muranyi (Mentor, a Siemens Business) |
| 14:20 | **BREAK, REFRESHMENTS (15 Minutes)** |
| 14:35 | **IBIS-AMI Post-Simulation Analysis** Mike LaBonte, Todd Westerhoff (SiSoft) [Presented by Mike LaBonte (SiSoft)] |
| 15:05 | **OPEN DISCUSSION AND CONCLUDING ITEMS** Next Open Forum Meeting: February 16, 2018 |
| 17:00 | **END OF MEETING ROOM AVAILABILITY** |

