

# **A System Developer's Perspective on AMI**

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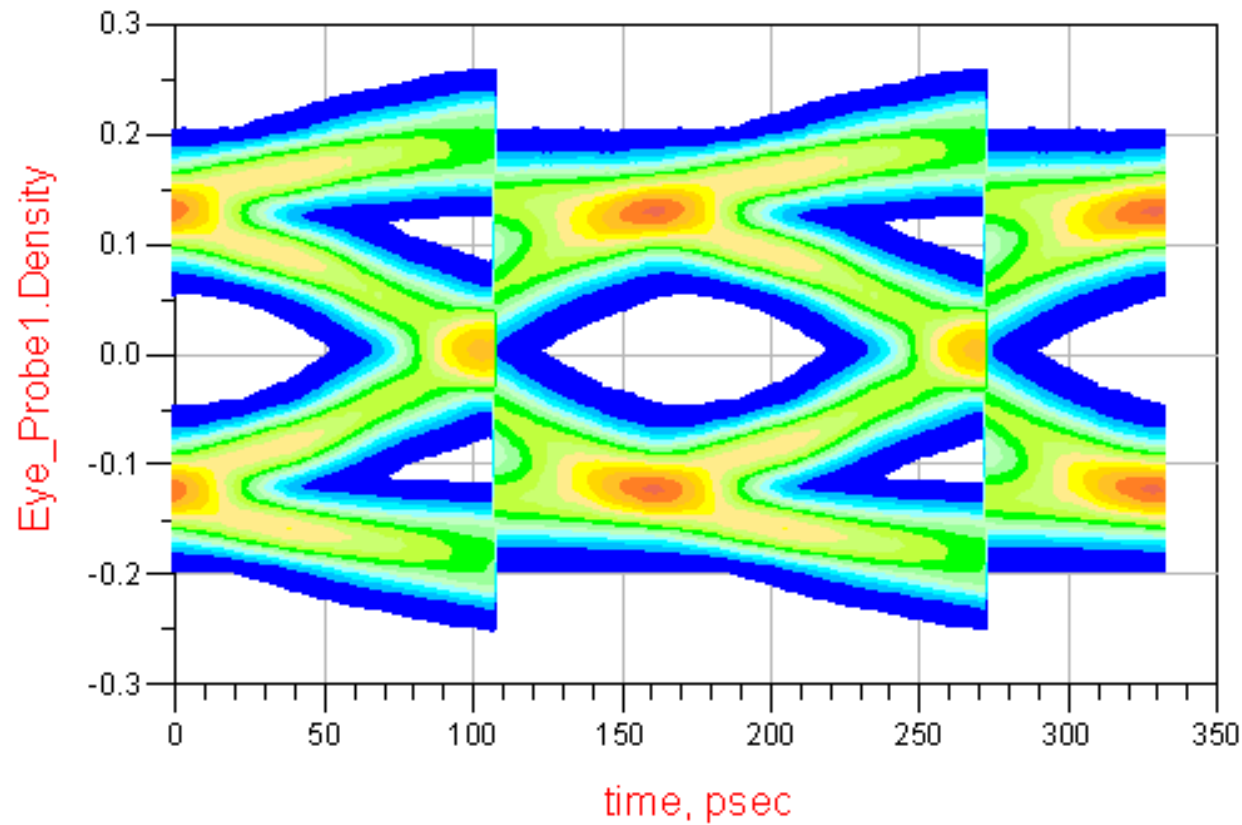
# Agenda

- AMI user's experience at IBM
- AMI Check List
- DLL verification

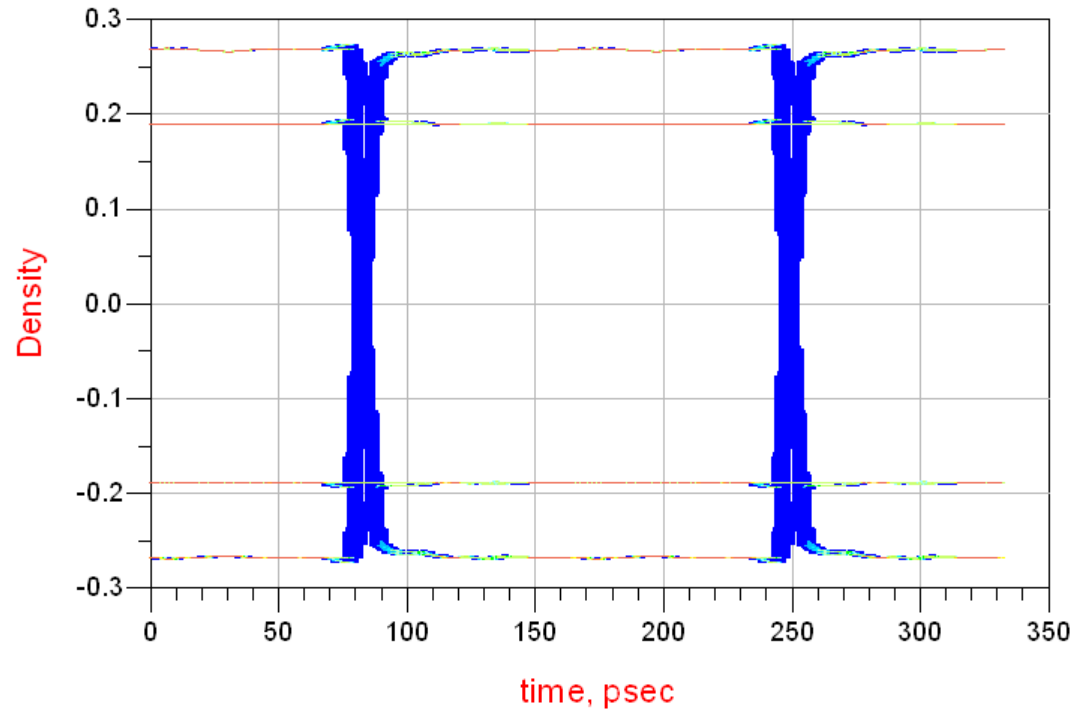
# State of AMI at IBM

- Two years into the effort
- Models from three suppliers
- Iterated with suppliers to get DLL to run
- Simulator evaluation is in round two
- Model-to-hardware correlation in progress
- IBM's internal simulator supports AMI
- No hardware yet designed with AMI models

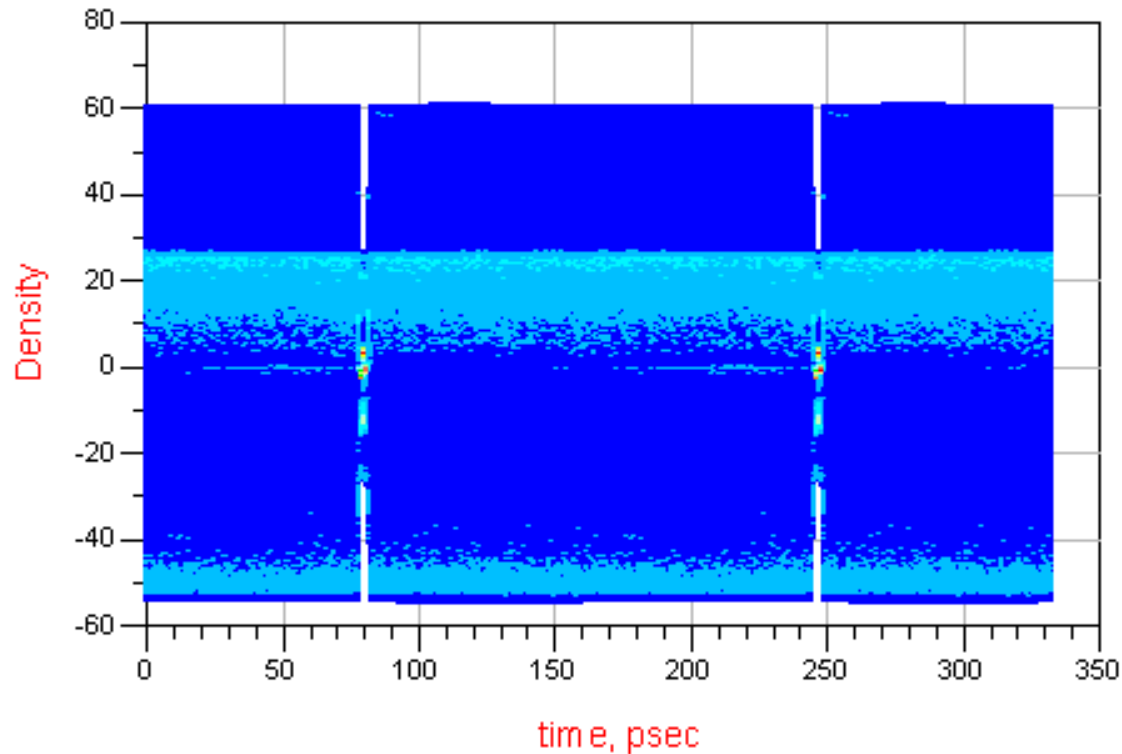
# Ideal TX & RX with 20 in. of 4-mil wire



# Swapped in AMI model...



# Example simulation from supplier



# AMI Check List

- Completeness
- Usage
- Documentation
- Accuracy

Statement of understanding between AMI supplier and customer; communication of expectations.

# Completeness

- ✓ .ibs file passes syntax checker
- ✓ TX .ami and .dll files
- ✓ RX .ami and .dll files
- ✓ Analog model included in .ibs file
- ✓ Touchstone package model(s)
- ✓ RX training algorithm included in DLL
- ✓ List other software necessary to run simulations



# Usage

- ✓ All files distributed in a single archive
- ✓ Model installation directory independent of execution directory
- ✓ Support for Windows and Linux
- ✓ Multiple instances of one model will run in one simulation/analysis
- ✓ Multiple instance of multiple models will run in one simulation/analysis
- ✓ Support for multiple simultaneous simulations/analyses (parallel processing)
- ✓ Unrecognized parameters do not cause failure

# Usage, con't

- ✓ Useful parameter description
- ✓ Model returns correct results at any samples-per-bit setting
- ✓ Ability to manually override equalizer settings
- ✓ No double counting of package, e.g. s-parameters and .ibs file
- ✓ No double counting of C\_Comp, e.g. s-parameters and .ibs file

# Documentation

- ✓ Support contact information
- ✓ User guide
- ✓ Software used to develop model
- ✓ Simulator(s) and version used to test model
- ✓ Company that developed model
- ✓ Company that designed serializer-deserializer (serdes) circuit
- ✓ Company that manufactured chip
- ✓ Type of TX equalization and number of taps
- ✓ Type of RX equalization and number of taps
- ✓ S-parameter port map

# Accuracy

- ✓ Lab report to include:
  - TX jitter decomposition measurements
  - RX stressed eye testing
  - Model-to-hardware correlation
  - Proof of industry standard compliance
- ✓ Does the PHY have an “on-chip oscilloscope” feature and software?
- ✓ Will the PHY output a test pattern with an oscilloscope connected?
- ✓ PRBS length?

# IBM's PHY Lab Report: PVT Corners

Corner	NFET $V_t$	PFET $V_t$	$L_{eff}$
Fast	Low	Low	Narrow
Nominal	Nominal	Nominal	Nominal
Slow	High	High	Wide

Corner	Minimum	Nominal	Maximum
$T_j$			
VDD			
AVTX			
AVRX			
AVDD			

# IBM's PHY Lab Report: TX Jitter

Jitter Component	Symbol	Nom	Max	Units
Total Jitter	TJ			ps, p-p
Deterministic Jitter	DJ			ps, $\Delta$ - $\Delta$
Data Dependent Jitter	DDJ			ps, p-p
Duty Cycle Distortion	DCD			ps, p-p
Periodic Jitter	PJ			ps, $\Delta$ - $\Delta$
Random Jitter	RJ			ps, rms

Eye Measurement	Min	Ave	Max	Units
Eye Opening				mV, p-p
Eye Amplitude				mV, p-p
Eye Width				ps

# IBM's PHY Lab Report: RX Stressed Eye

Component	Min	Max	Units
TX Amplitude			mV, p-p
TX Random Jitter			UI
TX Bounded Uncorrelated Jitter			UI
Link Dispersion Penalty			dB
Near End Crosstalk Frequency			ppm
Crosstalk Amplitude			mV

# DLL Test Bed

