IBIS Open Forum Minutes

Meeting Date: **February 4, 2010**
Meeting Location: **DesignCon IBIS Summit, Santa Clara, CA, USA**

VOTING MEMBERS AND 2010 PARTICIPANTS

Actel	(Prabhu Mohan)
Agilent	Radek Biernacki*, Ming Yan*, Fangyi Rao*
AMD	Nam Nguyen
Ansoft Corporation	(Steve Pytel)
Apple Computer	(Matt Herndon)
Applied Simulation Technology	(Fred Balistreri)
ARM	(Nirav Patel)
Cadence Design Systems	Terry Jernberg*, Wenliang Dai*, Ambrish Varma*
Cisco Systems	Syed Huq*, Mike LaBonte, Tony Penaloza*, Huyen Pham*, Bill Chen*, Ravindra Gali*, Zhiping Yang*
Ericsson	Anders Ekholm*, Pete Tomaszewski*
Freescale	Jon Burnett*, Om Mandhana*
Green Streak Programs	Lynne Green*
Hitachi ULSI Systems	(Kazuyoshi Shoji)
Huawei Technologies	(Jinjun Li)
IBM	Adge Hawes*
Infineon Technologies AG	(Christian Sporrer)
Intel Corporation	(Michael Mirmak), Myoung (Joon) Choi*, Vishram Pandit*, Richard Mellitz*
IO Methodology	Lance Wang*
LSI	Brian Burdick
Mentor Graphics	Arpad Muranyi*, Neil Fernandes*, Zhen Mu*
Micron Technology	Randy Wolff*
Nokia Siemens Networks GmbH	Eckhard Lenski
Samtec	(Corey Kimble)
Signal Integrity Software	Walter Katz*, Mike Steinberger*, Todd Westerhoff*, Barry Katz*
Sigrity	Brad Brim*, Kumar Keshavan*
Synopsys	Ted Mido*
Teraspeed Consulting Group	Bob Ross*, Tom Dagostino*
Toshiba	(Yasumasa Kondo)
Xilinx	Mike Jenkins*
ZTE	(Huang Min)
Zuken	Michael Schaeder*

OTHER PARTICIPANTS IN 2010

AET, Inc.	Mikio Kiyono*
Altera	John Oh*, Hui Fu*

Avago	Razi Kaw*
Broadcom	Mohammad Ali*
Curtiss-Wright	John Phillips*
ECL, Inc.	Tom Iddings*
eSilicon	Hanza Rahmai*
Exar Corp.	Helen Nguyen*
Mindspeed	Bobby Altaf*
NetLogic Microsystems	Eric Hsu*, Edward Wu*
Renesas Technology	Takuji Komeda*
Simberian	Yuriy Shlepnev*
Span Systems Corporation	Vidya (Viddy) Amirapu*
Summit Computer Systems	Bob Davis*
TechAmerica	(Chris Denham)
Texas Instruments	Bonnie Baker*
Independent	AbdulRahman (Abbey) Rafiq*, Robert Badal*

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
February 19, 2010	203 886 410	IBIS

For teleconference dial-in information, use the password at the following website:

https://cisco.webex.com/cisco/j.php?J=203886410

All teleconference meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

OFFICIAL OPENING

The IBIS Open Forum Summit was held in Santa Clara, California at the Santa Clara Convention Center during the 2010 DesignCon Conference. About 56 people representing 32 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.eda-stds.org/ibis/summits/feb10/

Bob Ross opened the meeting by welcoming the attendees. He asked people in the room to provide brief introductions for themselves. Bob asked how many people were model makers, EDA software developers, and model consumers. He thanked Cisco for sponsoring the event.

IBIS ACTIVITIES AND FUTURE PLANS

Bob Ross, Teraspeed Consulting Group

Bob Ross introduced the 2009-2010 officers. He summarized recent IBIS activities including meetings, summits, the new logo, and active task groups. Task groups include the IBIS Model Review, IBIS Quality, Interconnect Modeling and Advanced Technology Modeling. The ibischk5 parser was released in 2005 to support IBIS 5.0. He introduced the new flags in ibischk5. A Touchstone 1.0/2.0 parser, tschk2, was also released in 2009. Bob detailed the –canonical and –describe flags of tschk2. Arpad Muranyi asked if there were any issues with degradation of significant digits when using the -canonical flag to convert between Touchstone 1.0 and 2.0 versions. Bob was not aware of any. Bob finished with a list of known future projects.

TOP 10 ISSUES AS SEEN DURING IBIS MODEL REVIEWS

Lynne Green, Green Streak Programs

Lynne Green began by detailing the model review flow. Seven companies are active reviewers. Most model makers have moved to using s2ibis3. Many well known issues are still around. Four issues are related to the headers and setup. Six issues relate to the data such as extrapolation issues, non-monotonicities and V-t curve lengths. More people are using the IBIS Cookbook and running ibischk5. Model makers and their managers need training. Differential models need a lot more care. The model review committee is still needed. Syed Huq asked if there was a way to speed up the review time of the committee. Lynne replied that all of the reviewers are volunteers, so she can't set deadlines on them.

IBIS QUALITY CHECKLIST REV. 2.0

Moshiul Haque, Randy Wolff, Micron Technology

Randy Wolff gave a brief overview of the quality levels detailed in the IBIS Quality Specification, Rev. 1.0 and 2.0. He introduced the new IBIS Quality Checklist to go along with the 2.0 specification. The checklist is a spreadsheet designed to be filled out for a single IBIS file. It summarizes all of the model checks from the specification. The checklist spreadsheet has three tabs for a summary, components, and models. He showed an example of the checklist filled out for an IBIS file. He encouraged model makers to begin using the checklist.

Arpad Muranyi asked if the overall quality level within the report could be calculated based on the quality levels of the component and model sheets. Randy said he would share this question

with the IBIS Quality Committee.

PIN-PAIR ORIENTED EXTRACTION METHOD FOR DIFFERENTIAL PAIR IBIS MODELING

Lance Wang, IO Methodology

Lance Wang noted that people have struggled to develop differential pair models. Pseudo differential pair models are modeled ok with [Diff Pin]. True differential pair buffers are more difficult. The best way to model a differential pair signal is to model the subtracted currents between the positive pin and the negative pin. IBIS I-V curves are table lookups where the output current is a summation of the pullup, pulldown, power clamp, and ground clamp tables. The differential current can be put into both IBIS current curves, but it must be extracted for a real system load condition. Lance showed correlation of the model to a simple differential resistor test load as well as to an AC coupled test load. Both positive and negative buffer models must be used at the same time, and the simulation may not be accurate if the models are used under different conditions than when extracted.

Arpad Muranyi commented that he had described another method in the cookbook where the differential current was included as a serial model with the single ended currents present in the two single-ended models. Walter Katz noted that Lance's method was a simplification of Arpad's method for buffers where you don't have any skew between the active high and low buffers. Most buffers fall into the simpler category. Walter noted that there is a common model voltage needed during the extraction. Lance added that there may be problems with the ibischk utility seeing mismatch between I-V and V-t curves. V-t curves may be scaled to match the I-V curves. Arpad noted that one might get different results from various tools due to scaling of the V-t curves.

SIGNAL LOOP INDUCTANCE IN [PIN] AND [PACKAGE MODEL]

Randy Wolff, Micron Technology

Randy Wolff began with a definition of inductance, noting that a loop must be defined. Self and mutual inductance were defined. Partial inductance is a mathematical construct. Partial self inductance and partial mutual inductance have no meaning independent from other partial inductances that form a loop. Randy showed the inductance matrix from a 3D field solver solution of three traces in free space. The partial self inductances were the same for each trace, but the loop inductance was different depending on the defined return path. This concept was applied to other signal/ground arrangements. Simulations that do not model the return path properly were shown to give bad results. Randy showed that partial self inductances cannot be compared between various 3D field solvers. Only loop inductances can be compared. Complex models of self and mutual inductance can be simplified to a single loop inductance value in some simulations. Randy pointed out that [Pin] parasitics in IBIS models usually do not include loop inductance, but instead include self inductance. He showed an example of an internal tool used at Micron to calculate loop inductance from the full inductance matrix of self and mutual terms. Randy noted that the [Package Model] inductance matrix is used incorrectly by many EDA software vendors when modeling a single pin, because the return current path is not modeled.

Anders Ekholm asked if the loop inductance analyzer took into account the effects of current flowing in return paths closest to the signal. Randy responded that this is handled by the mutual terms between the signal and all of the return path options. One comment was that Loop

Inductance should be added to the IBIS specification so that it is clear to model makers what they should include in the [Pin] list.

AN INTRODUCTION TO MODEL CONNECTION PROTOCOLS

Brad Brim, Sigrity

Brad Brim presented on the IBIS Model Connection Protocol (MCP). This is a vendor-neutral method to specify electrical and physical connectivity information to enable automated connection of electrical models. Brad showed a simple system of a chip connecting to a package connecting to a board. The MCP for this system was shown. He then showed examples for multiple die/package/board connections.

Randy Wolff asked if this proposal extended well to larger systems. Brad explained that there were no limitations. Walter Katz felt that this was a good replacement for the earlier EMD concept. Some details are still being discussed in the Interconnect task group committee.

QUALITY METRICS FOR S-PARAMETER MODELS

Yuriy Shlepnev, Simberian

This presentation introduced metrics to distinguish good S-parameter models from bad ones and a methodology to improve the model quality for consistent frequency and time-domain analyses. Yuriy Shlepnev discussed reciprocity, whereby scattering matrices are symmetric. Sometimes averaging can be used to enforce reciprocity. Passivity can be enforced by normalization at each frequency point for minor violations. Two causality estimations were introduced. Causality can be improved by fitting the response with causal rational basis functions such as the rational compact model (RCM). RCMs can improve the quality of tabulated Touchstone models, produce broadband Spice models and compute the time-domain response of a channel. Yuriy discussed quality metrics for passivity, reciprocity and causality. He showed two examples of measurements of vias and corresponding quality metrics. An RCM was used to improve the models.

Richard Mellitz asked if RCMs could be used to improve models of structures with large delays separating small impedance mismatches. Yuriy said that this was challenging but possible. It was asked if there was a preference of fixing passivity or causality first. Yuriy said that causality must be fixed first before enforcing passivity.

SI/PI CO-ANALYSIS AND LINEARITY INDICATOR

Myoung Joon Choi, Vishram Pandit, Intel

Joon began by noting three major noise sources in channel analysis: crosstalk, ISI and SSO. SI analysis has been used for crosstalk and ISI analysis and PI analysis for SSO. Separate analysis is no longer sufficient for high speed, low cost systems. Joon showed the models needed for a full SI/PI co-simulation. Simulations were done for 8 cases controlling variation of ISI, crosstalk and SSO effects. Eye diagram measurements were used to summarize the results. A Linearity Indicator (LI) was defined as a metric of the ratio of degradation when analysis is done separately to that when it is done combined. It will indicate overestimation or underestimation of noise. The LI indicated that it was more important to do co-simulation for single-ended channels than for differential channels.

Arpad Muranyi asked if the reason for the difference was the differential drivers being less noisy. Joon indicated that there was less SSO noise in the differential buffer by design. Richard Mellitz noted that the name Linearity Indicator might be confusing, because the channel is still a linear system. Vishram Pandit noted that it is only indicative of the SI/PI relationship in the driver. The term could be better defined.

IBIS-ATM TASK GROUP REPORT

Arpad Muranyi, Mentor Graphics

Arpad Muranyi gave an overview of the recent work in the task group. The IBIS Interconnect Spice Subcircuit (IBIS-ISS) specification is in draft form but needs more work. The group is actively working on a BIRD to fix problems with the IBIS-AMI specification. Once the IBIS-AMI BIRD is completed, the group will return to working on the IBIS-ISS specification as well as discussing the EBD/EMD/Model Connection Protocol proposals.

Kumar Keshavan asked about the impetus behind the IBIS-ISS specification. Walter Katz explained the need for creating a common Spice language for use in improving EBD and package models.

PREDICTING BER WITH IBIS-AMI: EXPERIENCES CORRELATING SERDES SIMULATIONS AND MEASUREMENT

Todd Westerhoff*, Mike Steinberger*, Walter Katz*, Barry Katz*, Adge Hawes**, Kent Dramstad**, SiSoft*, IBM**

Adge Hawes began by defining the SerDes simulation problems of slow simulation in Spice and limited interoperability of models. He discussed the IBIS-AMI solution. IBIS-AMI does allow for pure statistical simulation as well as ~1,000,000 bits/minute time domain simulation. Adge discussed IBM's modeling strategy. They are supporting IBIS-AMI models that are correlated to their internal simulation tool. He discussed IBM's internal tool, HSSCDR, and noted that he expected an IBIS-AMI simulator to offer similar options and comparable results while allowing for interoperability with other vendor's Rx or Tx models.

Todd Westerhoff then presented results of a correlation study between HSSCDR and an IBIS-AMI simulator. The correlation strategies were to correlate everything up to the Rx pad by overlaying waveforms, and then correlate Rx behavior based on eye height/width at different probability levels, and then include jitter/noise sources once Tx/channel/Rx behaviors were correlated. Rx simulation results showed very good correlation. Todd briefly discussed methodologies for modeling jitter and noise. Simulation performance was also very comparable between the internal tool and the IBIS-AMI simulator.

Richard Mellitz asked if IBIS-AMI addressed high frequency versus low frequency jitter effects. Mike Steinberger noted that this was not standardized yet. The question was asked of how to handle modeling of non-LTI effects in the analog portion of the AMI model front end. Todd commented that there are some enhancements in the works to improve the analog modeling, but these solutions need to be brought to committee and standardized. Lynne Green asked if tools were starting to implement impulse responses for channel characterization. Todd thought that this was completed in EDA tools, but implementations are different.

CONDITIONAL EXPRESSIONS IN IBIS-AMI

Adge Hawes, IBM

Adge Hawes introduced the need for conditional expressions in IBIS-AMI. Different configuration setups may be required for corners, and many parameters may need to be tweaked. SerDes vendors must supply these parameters in additional data. Conditional expressions would give the AMI configuration a pre-process facility. Three corners may not be enough, and other configurations may be required. The DLL is not the place for simulator directives such as Usage Info. The EDA tool is also not the place for this information. Types of preprocessing that might be needed include substitution, case or switch statements, unit conversion, thresholds for parameter selection, and piecewise linear approximation for calculation of values based on linear interpolation between measured values. Adge suggested some rules for implementing conditional expressions. The DLL must implement resolution of conditional expressions, and the language used is the choice of the DLL developer. Possible interpretive languages for implementation in the DLL include Perl, Forth, and others. Adge showed an example using Forth. He hoped to remove the need for EDA tool-specific vendor wrappers for models.

Kumar Keshavan asked why there was a need for a new flow to handle this. Walter Katz presented some variables that need to be defined to enhance models. Arpad Muranyi asked if it would be more sensible to put this in the EDA software so as not to burden the model developer. Adge thought there were valid reasons for the model maker to do this, and he would be happy to publish examples to aid model makers.

GROWING PAINS WITH IBIS-AMI MODELING

Arpad Muranyi, Mentor Graphics

Arpad Muranyi began with a brief historical overview of IBIS-AMI development and the condition of the IBIS-AMI specification. The AMI parser has been updated to fix some issues. AMI is relatively new and a lot of education is needed. An IBIS-AMI cookbook would help a great deal. Not all AMI files are delivered with all of the necessary ingredients. The analog portion of the IBIS-AMI model needs improvements. This includes C_comp topologies, differential Cdiff and Rdiff, and package model improvements. These problems motivate vendors to write IBIS-AMI models that are not IBIS compliant. There is work in progress on a new interconnect specification and electrical model connectivity. Some differential buffer modeling issues are still not addressed. Arpad gave a plea for seriously addressing shortcomings in the legacy portions of the IBIS specification.

Todd Westerhoff asked if Arpad saw DLLs that are not specification compliant. Arpad said that he has only seen .ibs and .ami files that are not compliant, but the .ami file is the only place to understand how to pass information to the DLL.

OPEN DISCUSSION AND CONCLUDING ITEMS

Bob Ross closed the meeting by thanking the participants, presenters and co-sponsors and reminding those present of the dates for the next summit and teleconference meetings. The meeting was adjourned at approximately 4:00 PM.

NEXT MEETING

The next IBIS Open Forum teleconference will be held February 19, 2010 from 8:00 to 10:00 AM US Pacific Standard Time.

==========

NOTES

IBIS CHAIR: Bob Ross (503) 246-8048, Fax: (503) 239-4400
bob@teraspeed.com
Staff Scientist, Teraspeed Consulting Group
10238 SW Lancaster Road
Portland, OR 97219

VICE CHAIR: Lance Wang (978) 633-3388
lwang@iometh.com
President / CEO, IO Methodology, Inc.
PO Box 2099
Acton, MA 01720

SECRETARY: Randy Wolff (208) 363-1764, Fax: (208) 368-3475
rrwolff@micron.com
SI Modeling Manager, Micron Technology, Inc.
8000 S. Federal Way
Mail Stop: 01-711
Boise, ID 83707-0006

LIBRARIAN: Anders Ekholm (46) 10 714 27 58, Fax: (46) 8 757 23 40
ibis-librarian@eda.org
Digital Modules Design, PDU Base Stations, Ericsson AB
BU Network
Färögatan 6
164 80 Stockholm, Sweden

WEBMASTER: Syed Huq (408) 525-3399, Fax: (408) 526-5504
huqs@cisco.com
Manager, Hardware Engineering, Cisco Systems
170 West Tasman Drive
San Jose, CA 95134-1706

POSTMASTER: Mike LaBonte (978) 936-2147
milabont@cisco.com
Signal Integrity Engineer, Cisco Systems
Mail Stop BXB01/1/
1414 Massachusetts Ave
Boxborough, MA 01719

This meeting was conducted in accordance with the GEIA Legal Guides and GEIA Manual of Organization and Procedure.

The following e-mail addresses are used:

majordomo@eda.org

In the body, for the IBIS Open Forum Reflector:
subscribe ibis <your e-mail address>

In the body, for the IBIS Users' Group Reflector:
subscribe ibis-users <your e-mail address>

Help and other commands:
help

ibis-request@eda.org

To join, change, or drop from either or both:
IBIS Open Forum Reflector (ibis@eda.org)
IBIS Users' Group Reflector (ibis-users@eda.org)
State your request.

ibis-info@eda.org

To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the EIA-IBIS Open Forum as a full Member.

ibis@eda.org

To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

ibis-users@eda.org

To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda.org

To report ibischk parser BUGs as well as tschk2 parser BUGs. The BUG Report Form for ibischk resides along with reported BUGs at:

http://www.eda.org/ibis/bugs/ibischk/
http://www.eda.org/ibis/bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.eda.org/ibis/tschk_bugs/
http://www.eda.org/ibis/tschk_bugs/bugform.txt

icm-bug@eda.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/ibis/icm_bugs/
http://www.eda.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda.org/ibis/bugs/s2ibis/bugs2i.txt
http://www.eda.org/ibis/bugs/s2ibis2/bugs2i2.txt
http://www.eda.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eigroup.org/ibis/ibis.htm

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda.org/ibis/directory.html

IBIS CURRENT MEMBER VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

Organization	Interest Category	Standards Ballot Voting Status	December 11, 2009	January 8, 2010	January 29, 2010	February 4, 2010
Actel	Producer	Inactive				
Advanced Micro Devices	Producer	Active		√	√	
Agilent Technologies	User	Inactive				√
Ansoft	User	Inactive				
Apple Computer	User	Inactive				
Applied Simulation Technology	User	Inactive				
ARM	Producer	Inactive				
Cadence Design Systems	User	Inactive				√
Cisco Systems	User	Active	√	√	√	√
Ericsson	Producer	Active	√		√	√
Freescale	Producer	Inactive				√
Green Streak Programs	General Interest	Inactive				√
Huawei Technologies	Producer	Inactive				
Hitachi ULSI Systems	Producer	Inactive				
IBM	Producer	Active		√	√	√
Infineon Technologies AG	Producer	Inactive				
Intel Corp.	Producer	Inactive	√			√
IO Methodology	User	Active	√	√	√	√
LSI	Producer	Active		√	√	√
Mentor Graphics	User	Active	√	√	√	√
Micron Technology	Producer	Active	√	√	√	√
Nokia Siemens Networks	Producer	Active	√		√	
Samtec	Producer	Inactive				
Signal Integrity Software	User	Active	√	√	√	√
Sigrity	User	Inactive				√
Synopsys	User	Inactive				√
Teraspeed Consulting	General Interest	Active	√	√	√	√
Toshiba	Producer	Inactive				
Xilinx	Producer	Inactive				√
ZTE	User	Inactive				
Zuken	User	Inactive				√

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

INTEREST CATEGORIES ASSOCIATED WITH GEIA BALLOT VOTING ARE:

- USERS - MEMBERS THAT UTILIZE ELECTRONIC EQUIPMENT TO PROVIDE SERVICES TO AN END USER.
- PRODUCERS - MEMBERS THAT SUPPLY ELECTRONIC EQUIPMENT.
- GENERAL INTEREST - MEMBERS ARE NEITHER PRODUCERS NOR USERS. THIS CATEGORY INCLUDES, BUT IS NOT LIMITED TO, GOVERNMENT, REGULATORY AGENCIES (STATE AND FEDERAL), RESEARCHERS, OTHER ORGANIZATIONS AND ASSOCIATIONS, AND/OR CONSUMERS.