Capacitance Compensation

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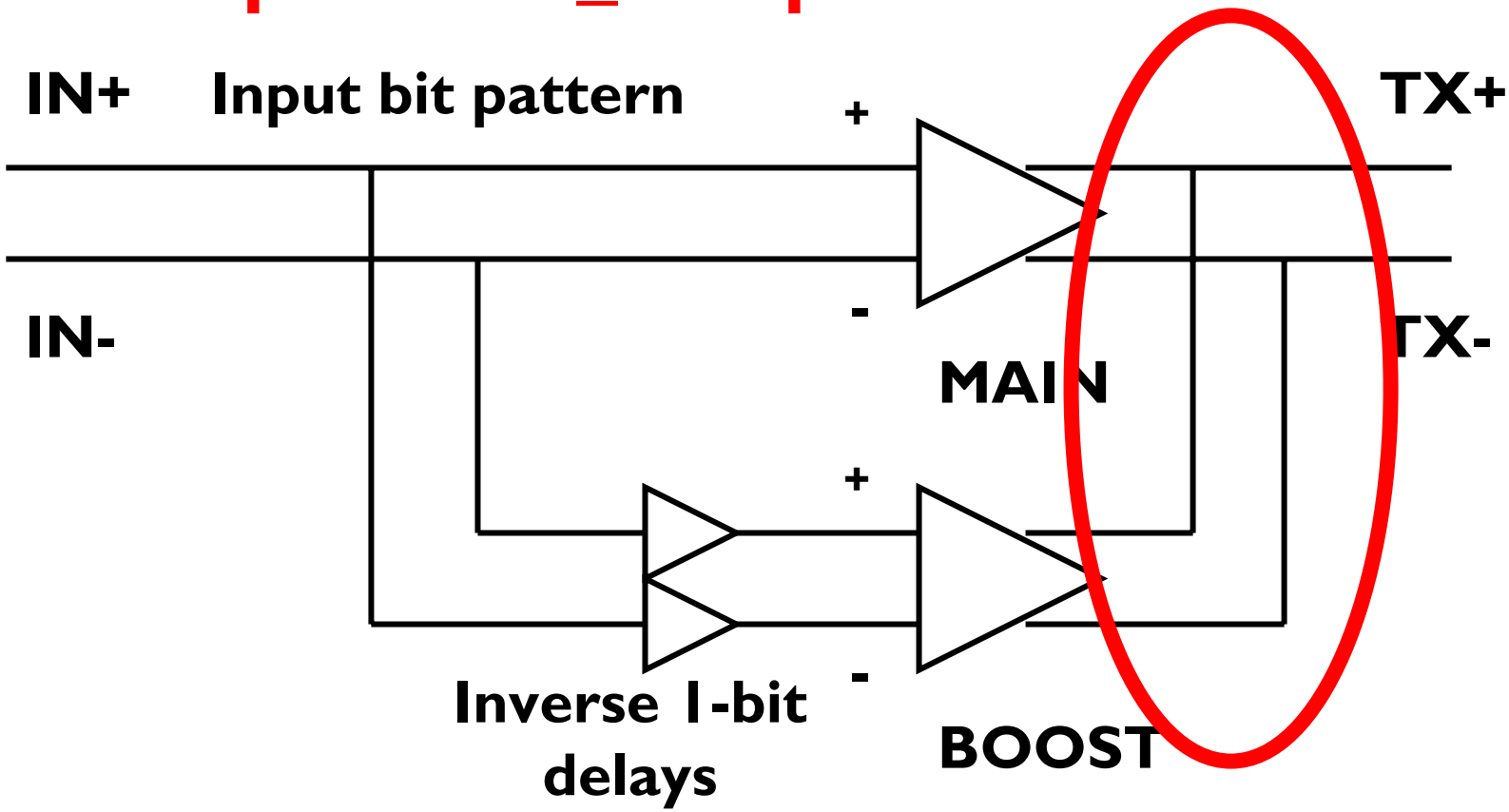
GROUP

Typical Problems

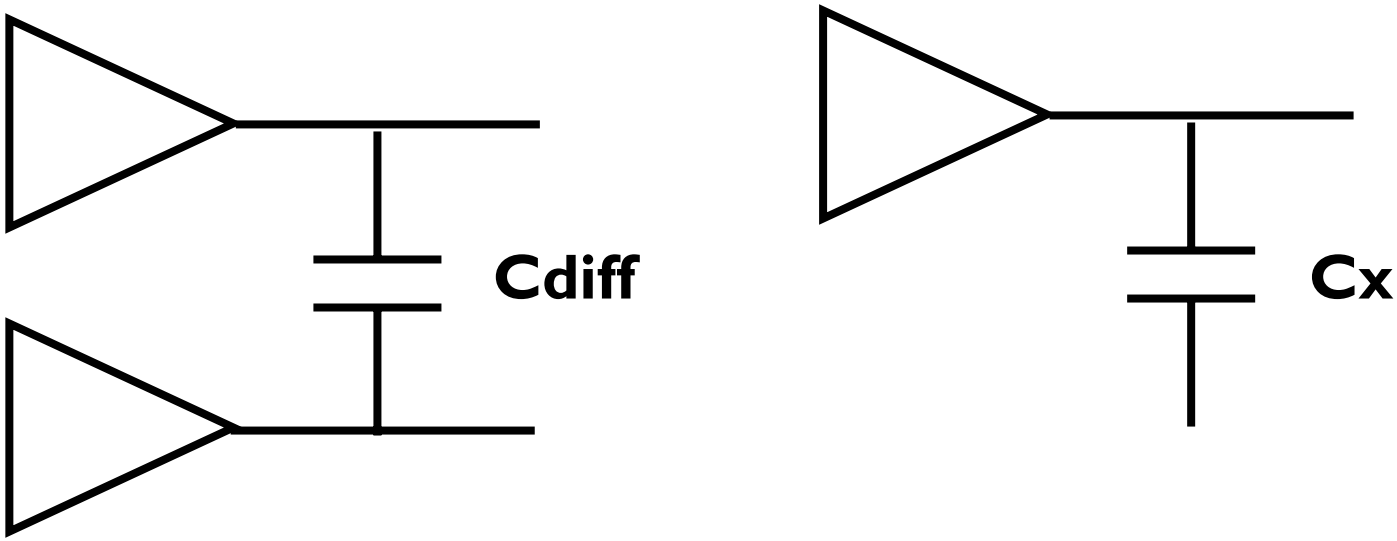
- Driver schedule
- Differential buffer
- External capacitance refinement
- Many other presentations either considered loading interactions or appeared to be impacted that interactions

Output Impedance and Top-level C_comp Interaction??




```
[Driver Schedule]
| Model_name Rise_on_dly Rise_off_dly Fall_on_dly Fall_off_dly
MAIN         0           NA           0           NA
BOOST        NA          0.47059ns    NA          0.47059ns
```

Differential Buffer Cdiff or Load Cx



Cdiff or Cx are extra capacitors that need compensation. They might be non-linear, but first order compensation better than no compensation

Possible Solutions

- Solutions
  - Ignore
    - Well within the range of expected drivers
    - Input is of primary concern
  - Adjusting V-T waveforms
  - Compensate by "C_fixture"
  - Also (not covered)
    - Other presentations
    - Or non-linear mathematical de-convolution – a whole new topic

Other Solutions Not Covered

- Language solutions
  - A. Muranyi,"Pre/de-emphasis Buffer Modeling with IBIS," March 11, 2005, European IBIS Summit – programmable state machine for each V-T combination
  - N. Rao, "De-emphasis Buffer Modeling Issues with IBIS", Nov. 14, 2008, Asian IBIS Summit (Japan) – Verilog AMS equation based model
- General problem and investigations – several presentations by M. Mirmak and A. Muranyi

Compensate by Adjusting V-T

- B. Ross, "IBIS Die V-T Tables from Part or Board Measurements," Feb. 9, 2004, DesignCon IBIS Summit
- Apply technique for Cx instead of just package or board
- A time-domain approximation solution that would give first order correction for non-linear C

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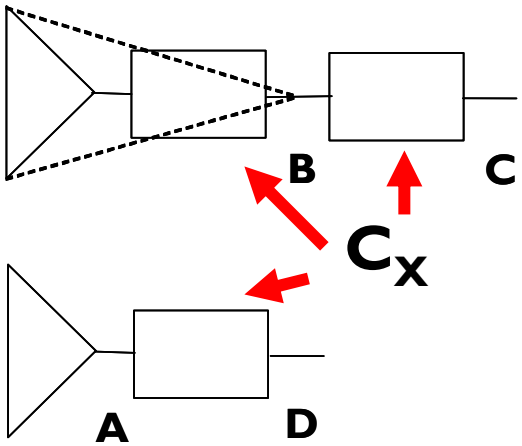
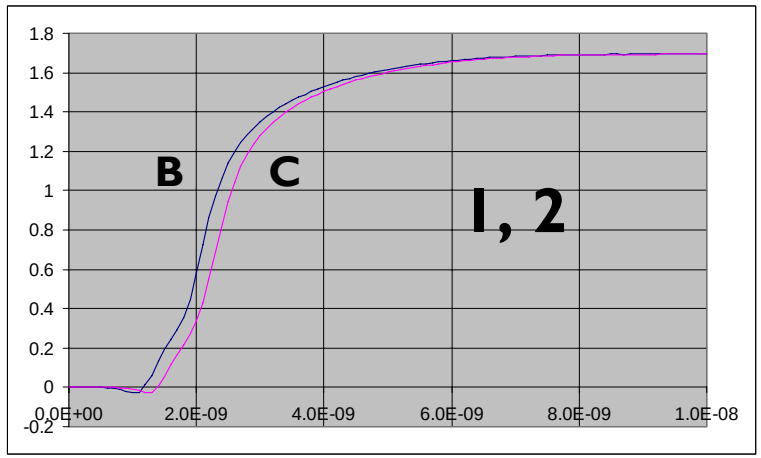
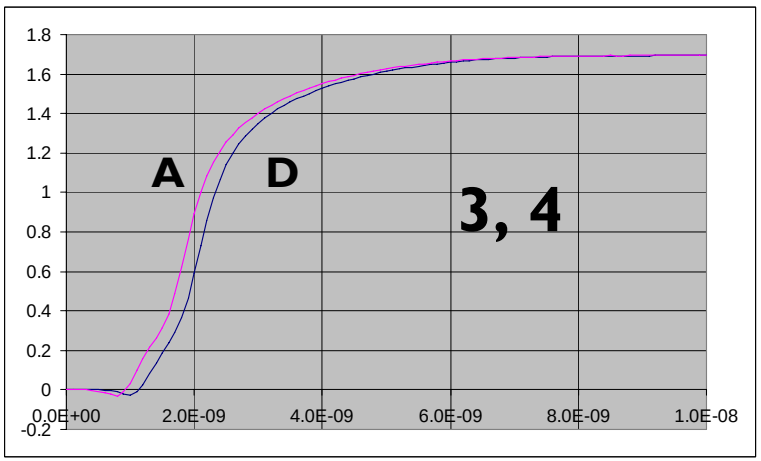
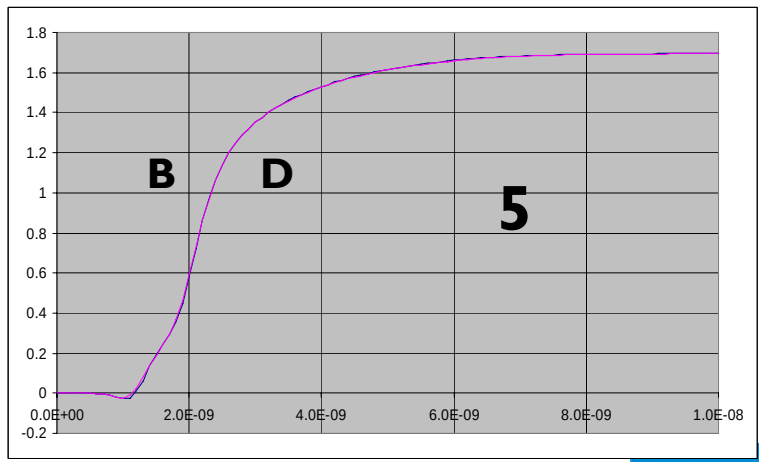
Could use Capacitor Instead of Package or Board Measurement (50 Ω to Gnd)









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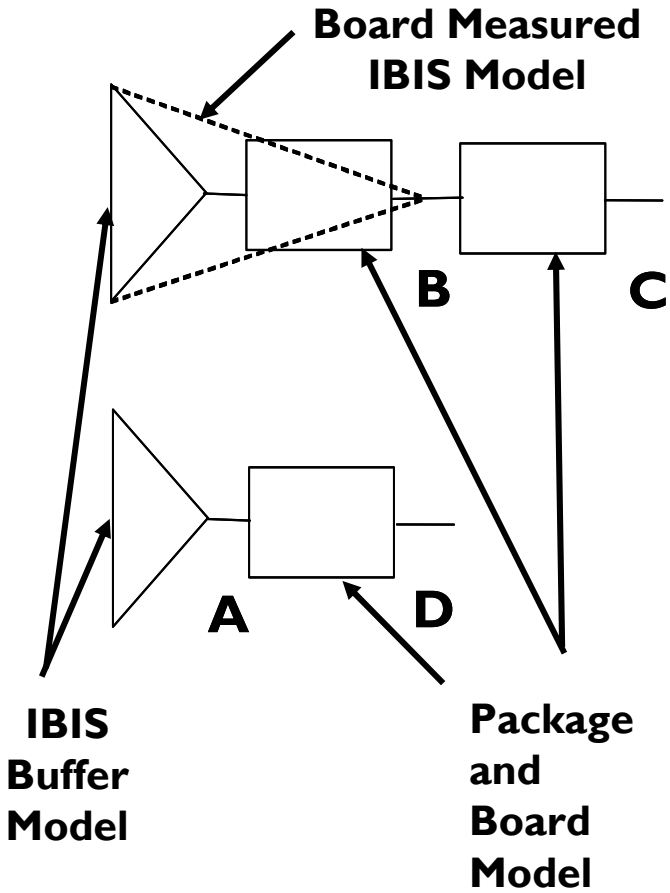
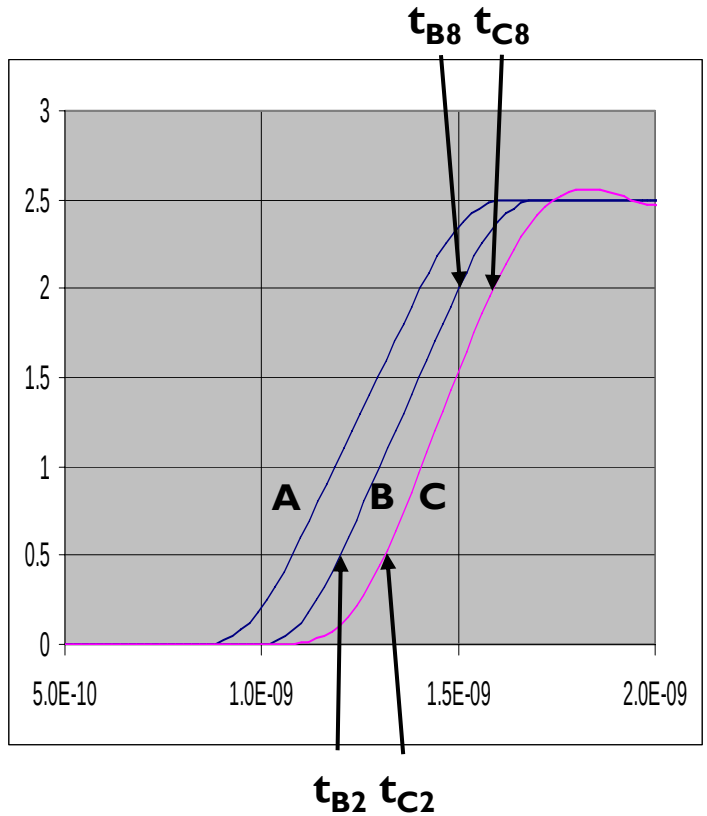
Steps for "Delta" Process IBIS Die V-T Tables from Pin/Board V-T Tables



1. Create IBIS model using MEASURED V-T tables at **B**
2. Simulate **B**, then add package/ board and simulate "delta" **C**
3. Use inverse of linear transform of **B** time axis to derive new IBIS model DIE V-T table **A**
4. Add package/board to simulate V-T response at **D**
5. Compare **B** and **D**

Step 3: Inverse Linear Transform to Find V-T table A from B

- Find times for 80% and 20% points of **B**, **C**: t_{B8}, t_{B2}, t_{C8}, t_{C2} (interpolate for accuracy)
- Solve transform for p and q:
  $\mathbf{t_C} = p * \mathbf{t_B} + q$
  (& assume $\mathbf{t_B} = p * \mathbf{t_A} + q$)
- Inverse transform time axis $\mathbf{t_B}$ to time axis $\mathbf{t_A}$ using:
  $\mathbf{t_A} = (\mathbf{t_B} - q) / p$
- $\mathbf{t_A} = t_{B8} + (\mathbf{t_B} - t_{C8}) * (t_{B8} - t_{B2}) / (t_{C8} - t_{C2})$



Compensate with C_fixture

- B. Ross, "C_comp and Buffer Scaling Observations," Feb. 9, 2006, DesignCon IBIS Summit
- X.F. Chen, "IBIS Algorithm Including Reactive Loads," Sept. 11, 2007, Asian IBIS Summit (China)
  - Shows C_fixture support algorithm
- C_fixture provides peaking without changing the actual buffer capacitance

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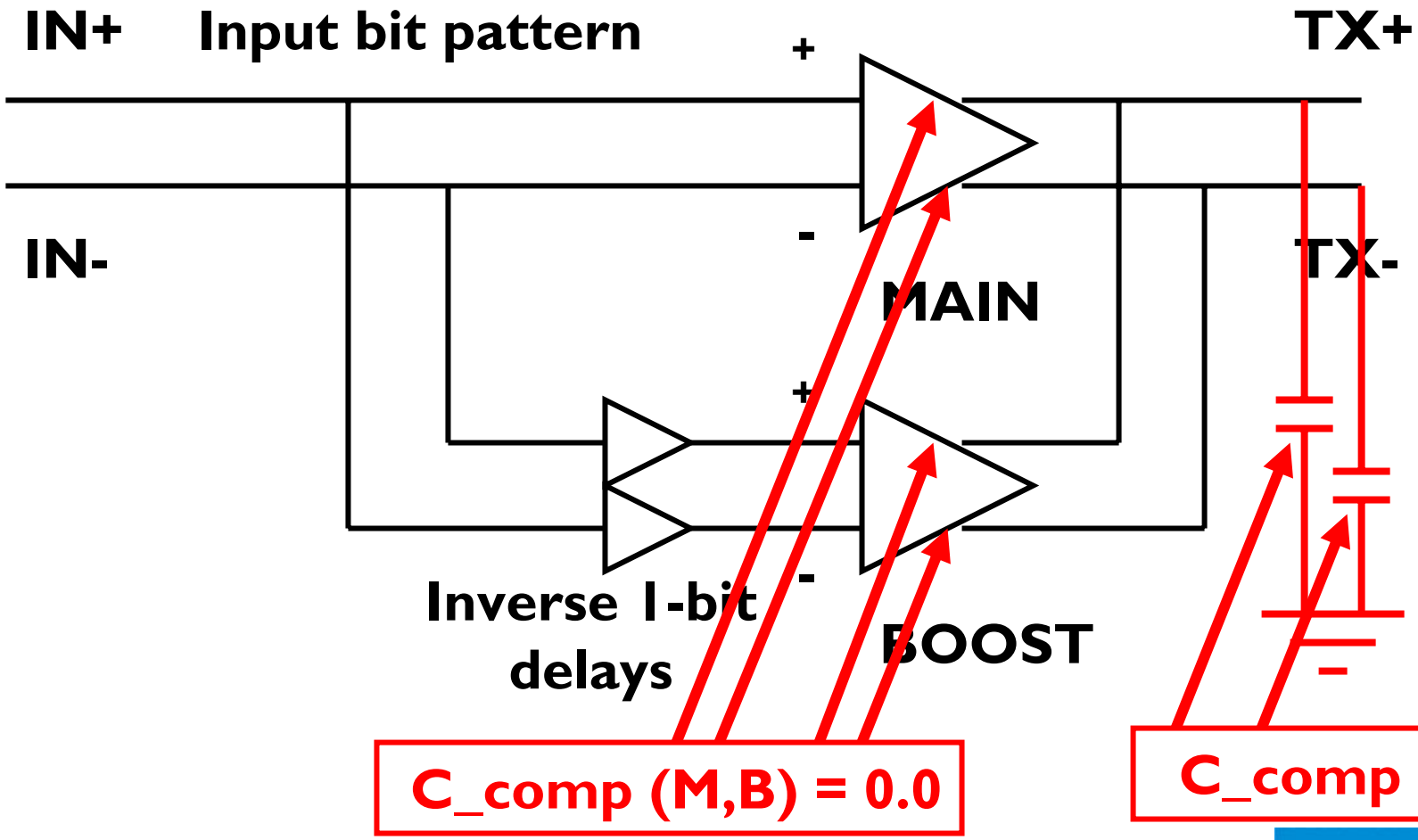
IBIS Solution - C_comp as Load with [Driver Schedule]



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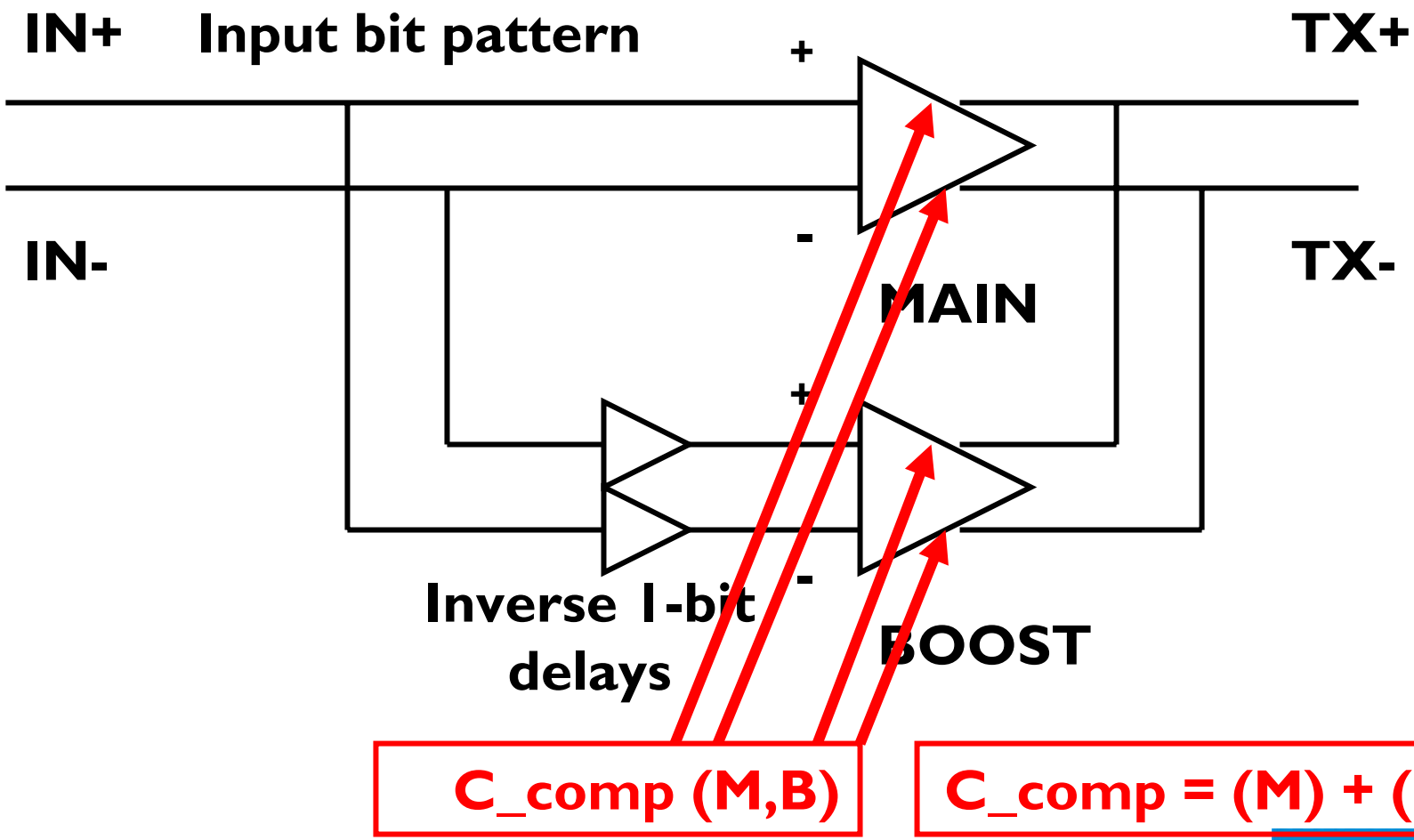
Macro Model – Buffer Scaling Solution



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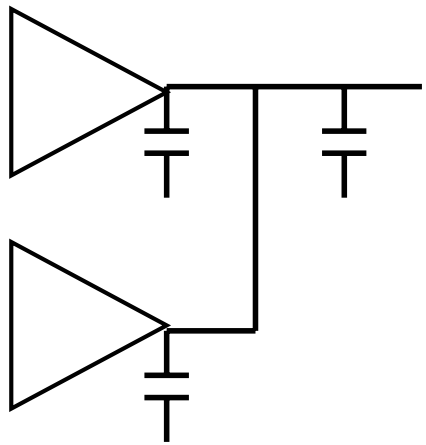
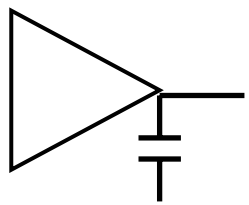
Both Approaches Have Limits - Ideal Buffer Test Case

- Summation
  - 100 ps ideal ramp
  - 25 Ω ideal buffer (in connected mode)
  - C_comp = 3.0 pF
  - Vcc = 1.5 V
- Each one-half scaled
    - 50 Ω ideal buffer
    - 100 ps ideal ramp
- 50 Ω R_fixture
- 50 Ω load





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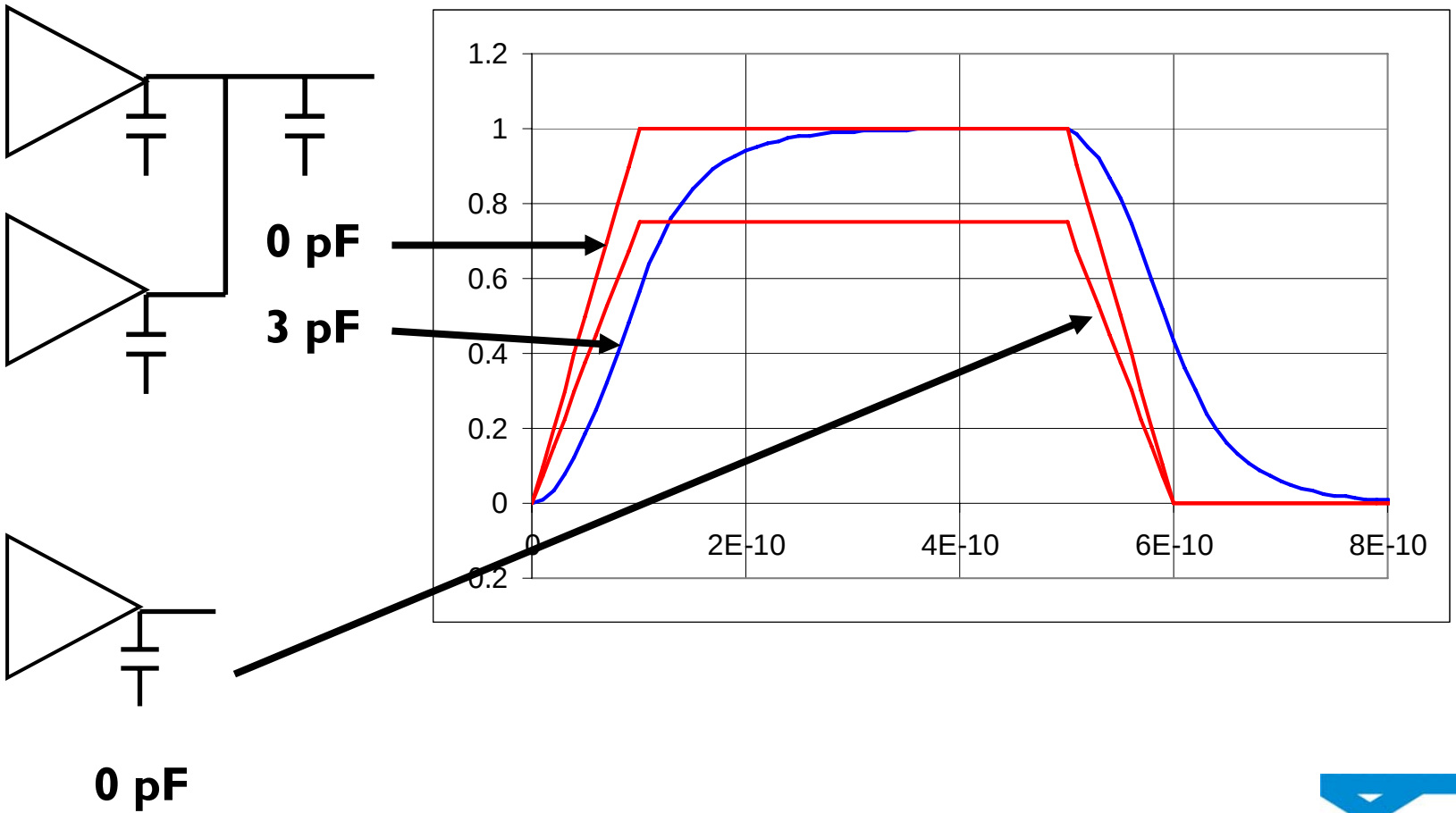
IBIS [Driver Schedule] Setup with/without C_comp = 3 pF



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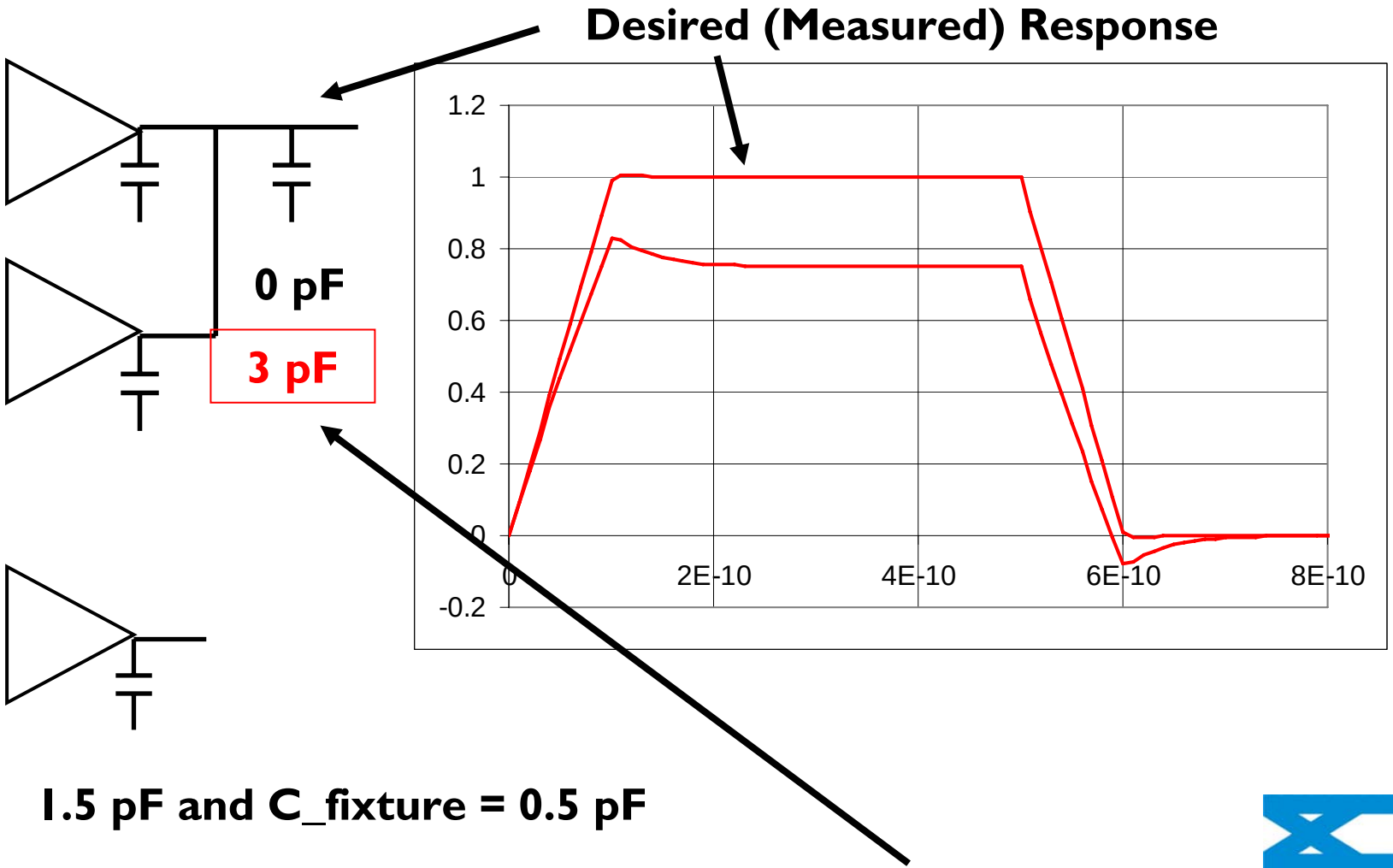
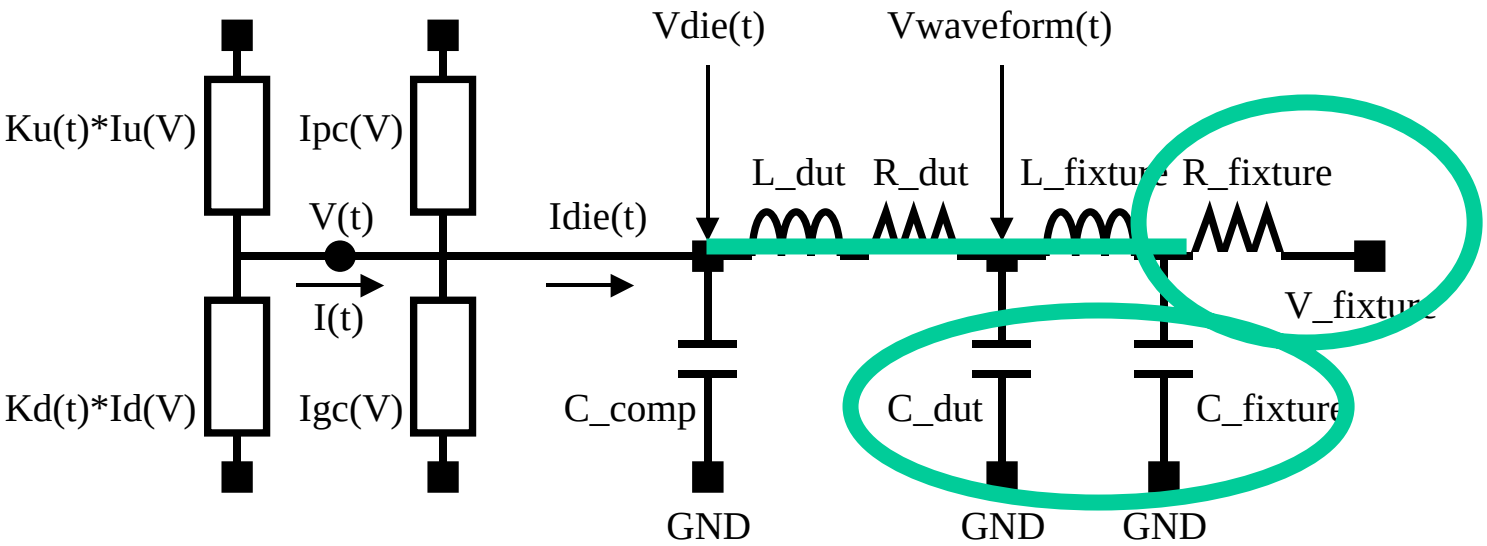
C_fixture Peaking Works in All Cases with Original Scaled Waveforms



1.5 pF and C_fixture = 0.5 pF

or 0 pF and C_fixture = 2.0 pF for [Driver Schedule] setup

Proposed Expanded Subset of IBIS Version 2.1



C_comp* = C_comp + C_dut + C_fixture

K-table Extraction algorithm UNCHANGED

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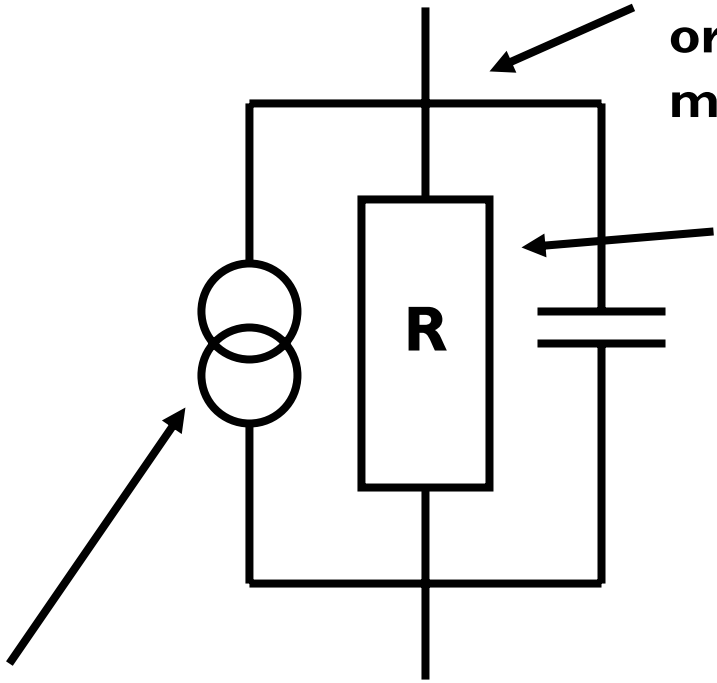
One Node Norton Equivalent of Ideal 2-waveform Buffer Used for Testing



Buffer voltage for ideal ramp or peaked ramp when measured into a 50 Ω load

50 Ω

C_comp settings for buffer

SPICE PWL Current source ramp plus fixed switched charging current for buffer C_comp and any additional C_fixture

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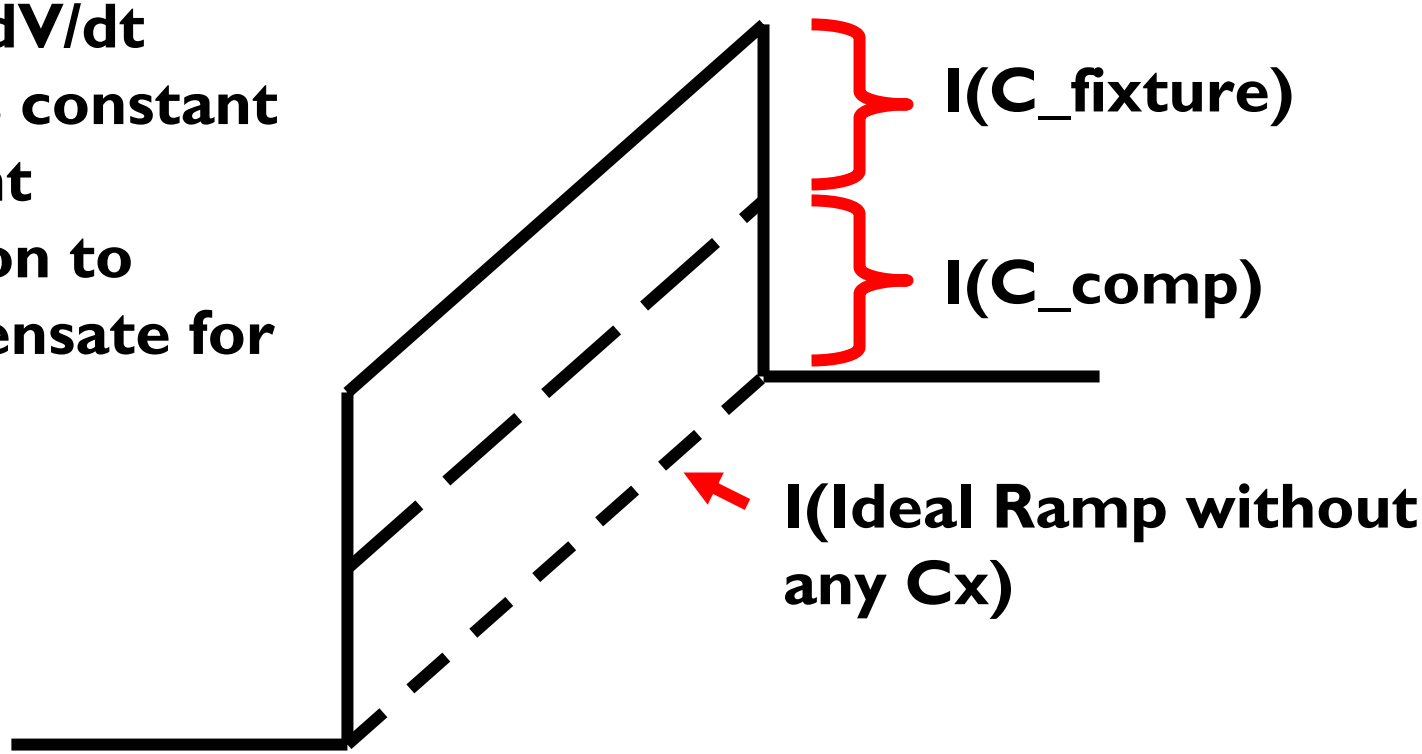
I-Source (Current Source Driver)

I = C*dV/dt means constant current addition to compensate for Cx



Charging currents calculated or found by experimentation

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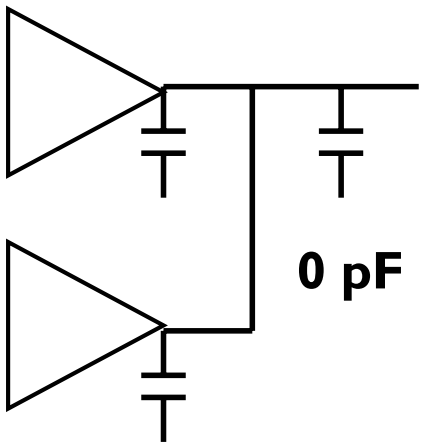
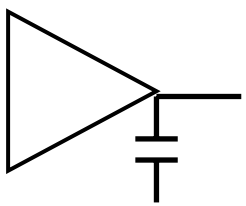
Comments on Simple Model

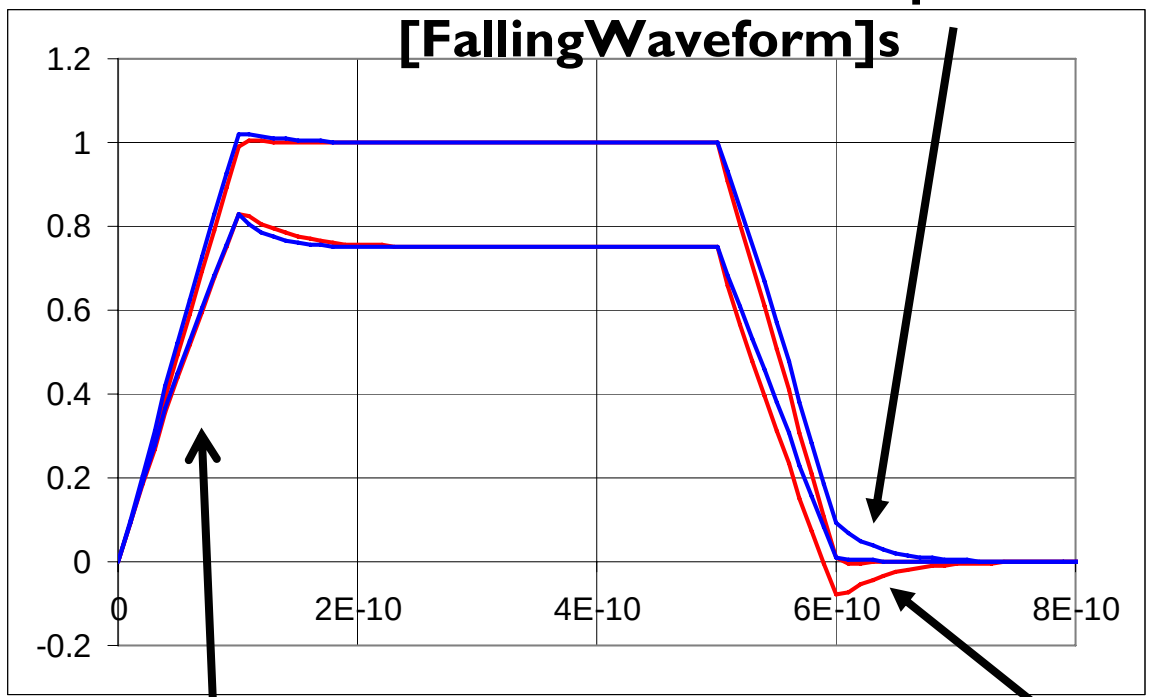
- Current source was one PWL
  - Separate PULSE adding together could have been used
  - Parameterized input could have been used
- Overshoot/Undershoot implies do NOT clip K tables in IBIS model
  - Even C_comp not fully compensated leading to rolled up responses (charging current starvation)
  - So would not work with C_fixture
- Could work for relatively constant high impedance current mode logic
- Open_drain, Open_source buffers non-linear, best done with real buffer for ramp (but constant charging current addition)

Ideal Test Buffer (Red) Duplicated in SPICE (Blue)





1.5 pF



Ideal buffer, SPICE C_fixture = 0.5 pF on [Rising Waveform]s

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Conclusions

- Driver needs to compensate for external Cx load
  - Change V-T waveform
  - Use C_fixture (but inconsistent industrial support)
- Techniques still keep correct input C_comp or Cx or Cdiff
- Do NOT clip K-tables – can cause IBIS simulation error with correct IBIS model

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