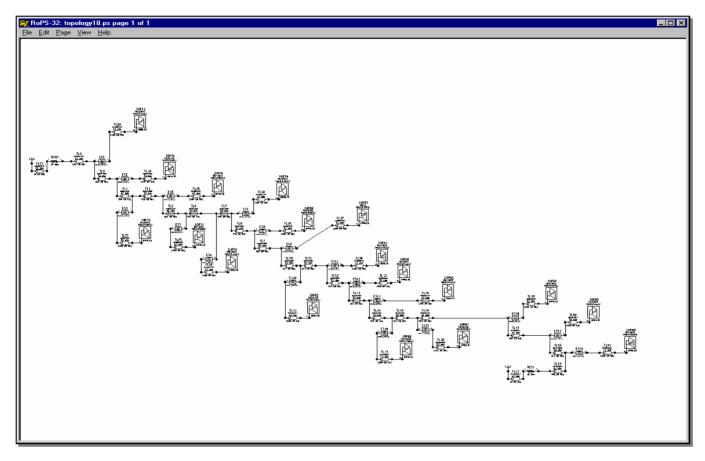
How IBIS Models Relate to SI, PI, and EMI-EMC

Roy Leventhal DesignCon 2009 IBIS Summit Meeting Santa Clara, CA February 5, 2009



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An Example of a Complex Network

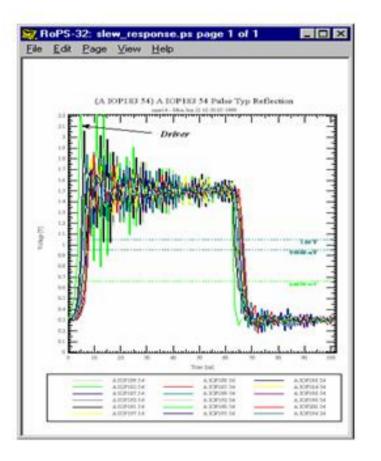


An 18-Slot Bi-Directional Backplane Bus





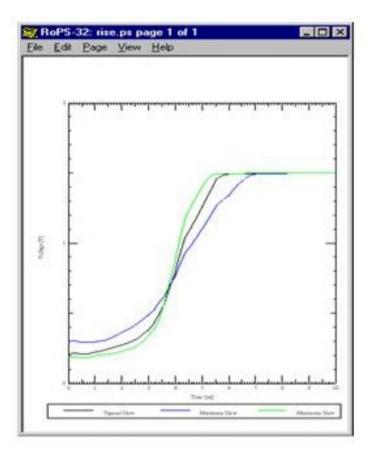
Simulation Results from too Simple a Model



- Complex nets are hard to terminate and have many reflections
- Simple dV/dt modeling and device behavior is inadequate
- V-T curves need to be modeled for correct results in GTL/GTLP busses

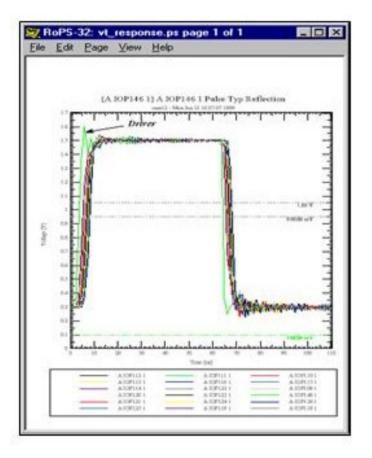
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IBIS Modeling of V-T Curves How GTLP Really Behaves



- This slide shows how to correctly model GTL/GTLP
- Soft turn-on/turn-off removes many highfrequency components (think about Fourier transformation) from driving the line
- The results of the change in modeling detail are shown next:

Better Models Give Better Results



"Everything should be as simple as possible *and no simpler*."

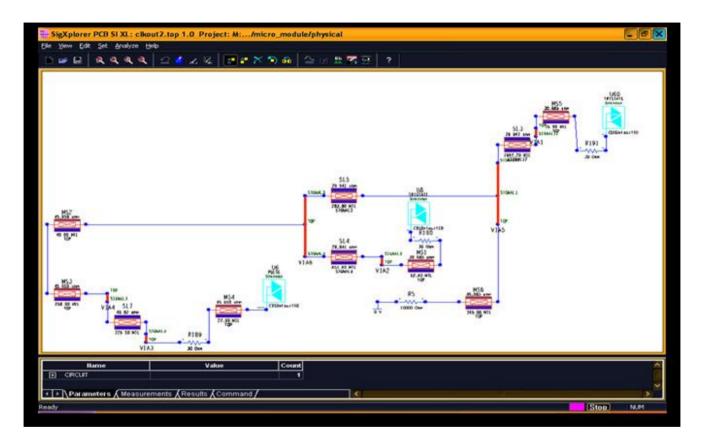
-----Albert Einstein



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Test Net for SI and EMI

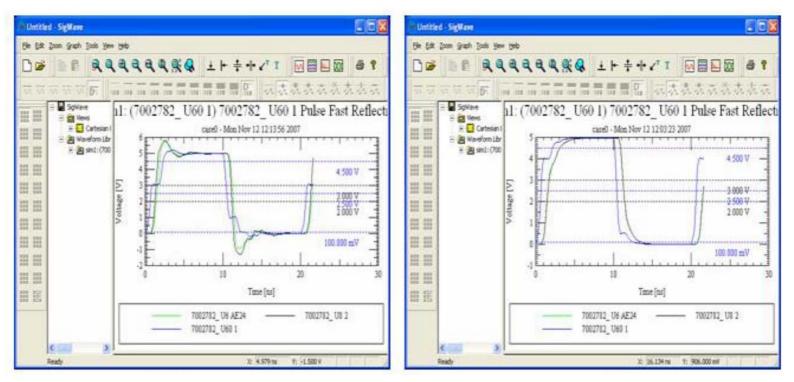


66MHz Clock Topology as Modified

Courtesy of Hamilton-Sundstrand



How SI is Affected by Overshoot



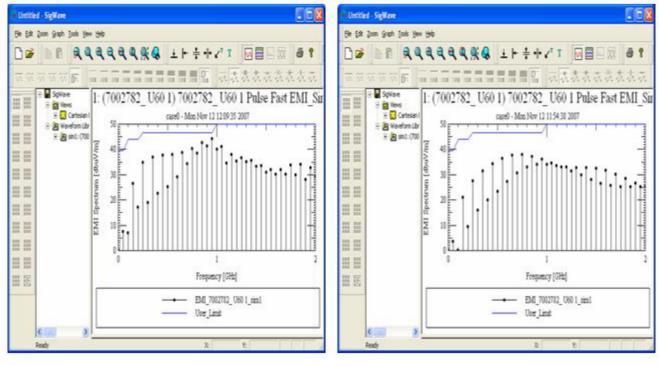


After Termination

Before termination, SI and stress on the receiver is not a high concern – the real payoff will be in EMI control as shown in the next slide.



How EMI is Affected by Overshoot



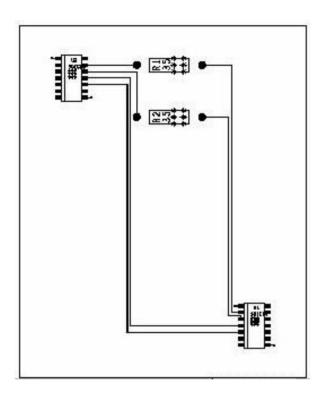
Before Termination

After Termination

The SI Engineer has to manage harmonics out to about the 5th. The EMI engineer has to manage harmonics out to, perhaps, the 100th.



Example of Virtual Test Board



The board on the left has the following stackup:

> top: 1.2 mil Cu signal Zo = 89Ω next: 12 mil FR4 ($\varepsilon r = 4.5$) next: 1.2 mil Cu shield Vcc next[.] 12 mil FR4 next: 1.2 mil Cu shield GND next: 12 mil FR4 bottom: 1.2 mil Cu signal Zo = 89Ω Etch width is nominally 6 mils

For the shielded version outer shield layers of 1.2 mil Cu spaced by 12 mils of FR4 were added

> The nominal 6 mil etch on such an inner layer results in Zo = 59.6 Ω

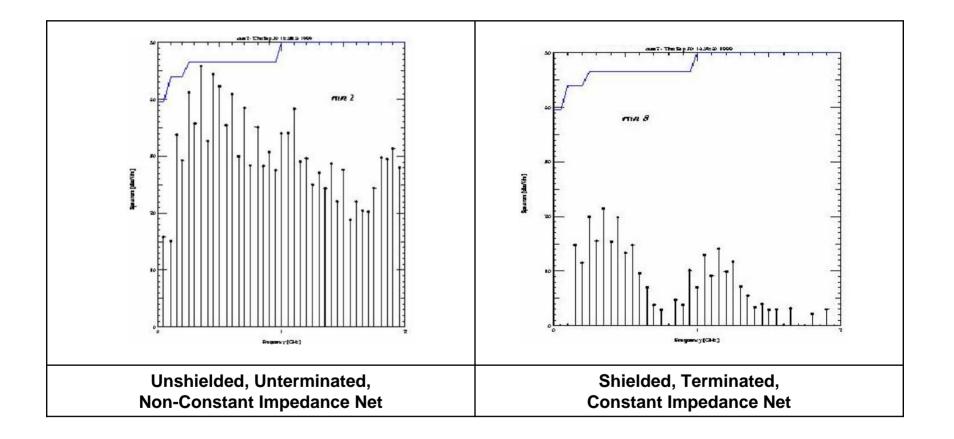
The board is about 3 inches long.

Layout of the Test Board

Stackup of the Test Board



Virtual Test Board Before and After EMI Treatment



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Near Field EMI Simulators

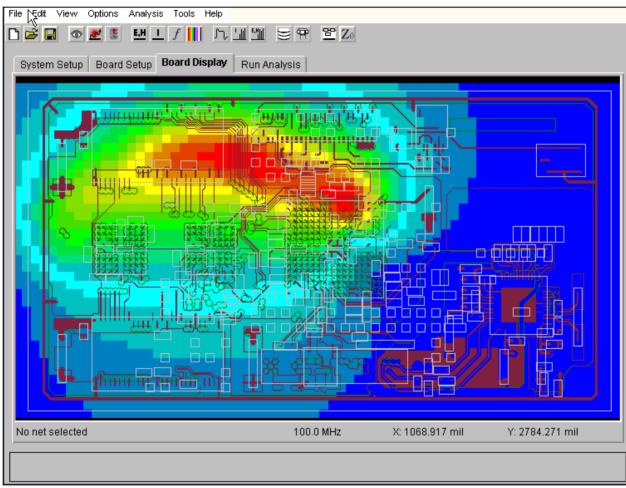
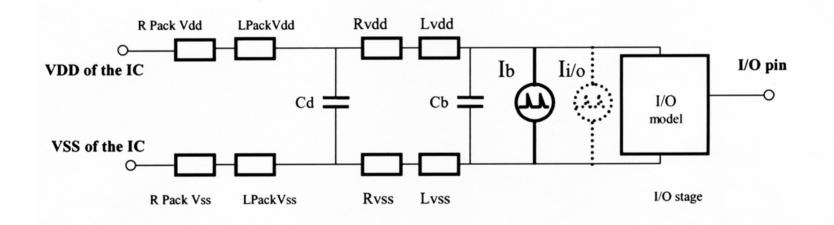


Image Courtesy of Johnson Controls Automotive, Inc. Used with permission



PI and the IEC 62014-3 Proposal



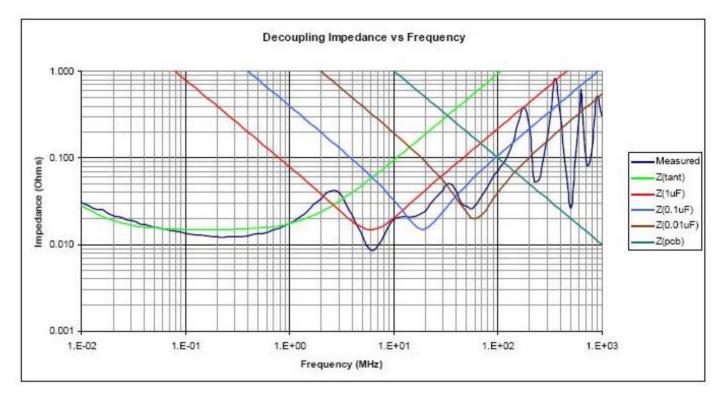
Slide courtesy of Etienne Sicard, INSA-Toulouse

What is happening with IEC 62014-3?

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Bypassing the Power Supply for PI



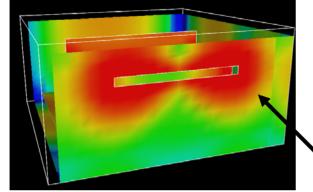
Slide courtesy of Lee Ritchey, Speeding Edge

Reminder to myself: Let's have a discussion of some of the latest PCB techniques for controlling power plane bounce, crosstalk, and emissions

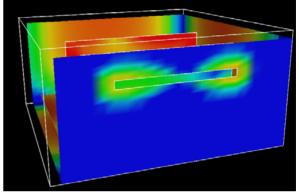


3D Full-Wave EMI Simulators

Baseline

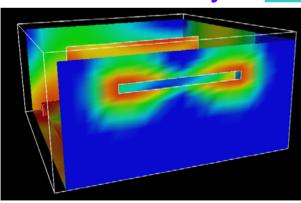


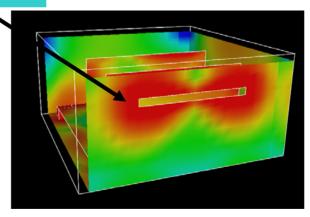
Ground Pins Only



Strong Coupling to Slot-WHY? Pins and Standoffs

Standoffs Only

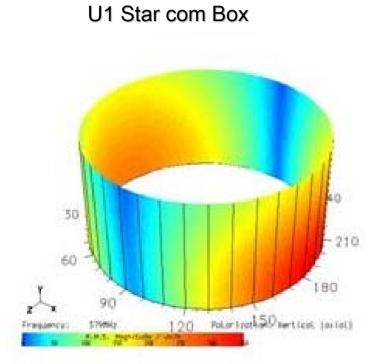




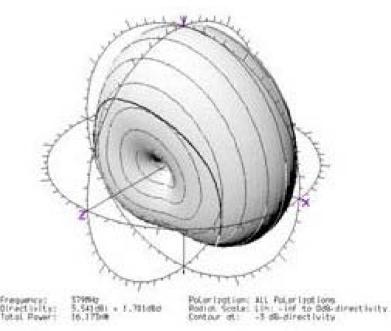
Slide courtesy of FloEMC used with permission



Far-Field EMI Simulators



U1 Star com Box



3m cylinder scan

Far-Field radiation

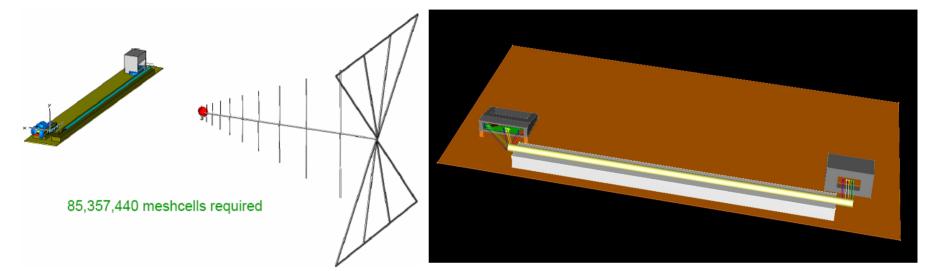
Slide courtesy of FloEMC used with permission



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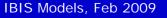
The Virtual Test Bench





Slide courtesy of Jerry Meyerhoff, Continental AG, and CST/FloEMC. Used with permission.

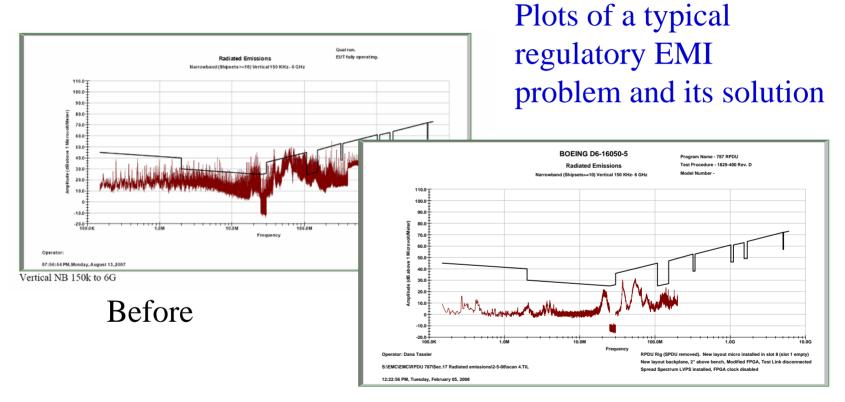
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Modelers Need to Use the Language of the Frequency Domain in Talking to EMI Engineers



After

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Summary

EMI

- Is driven by the strength and speed of the output driver
- Is driven by the discontinuities of the transmission net
- Extends to much higher harmonics than SI issues
- EMI can be controlled by sophisticated techniques for resolving the problems created by high-speed drivers
- EMI issues at the PCB, enclosure, and system level can be studied with sophisticated CEM tools. CEM facilitates the study of EMI design tradeoffs related to models and net design.
- Modelers use time domain concepts. EMI Engineers use frequency domain concepts. They need to communicate in each other's language.





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