Xilinx IBIS Model Quality Update

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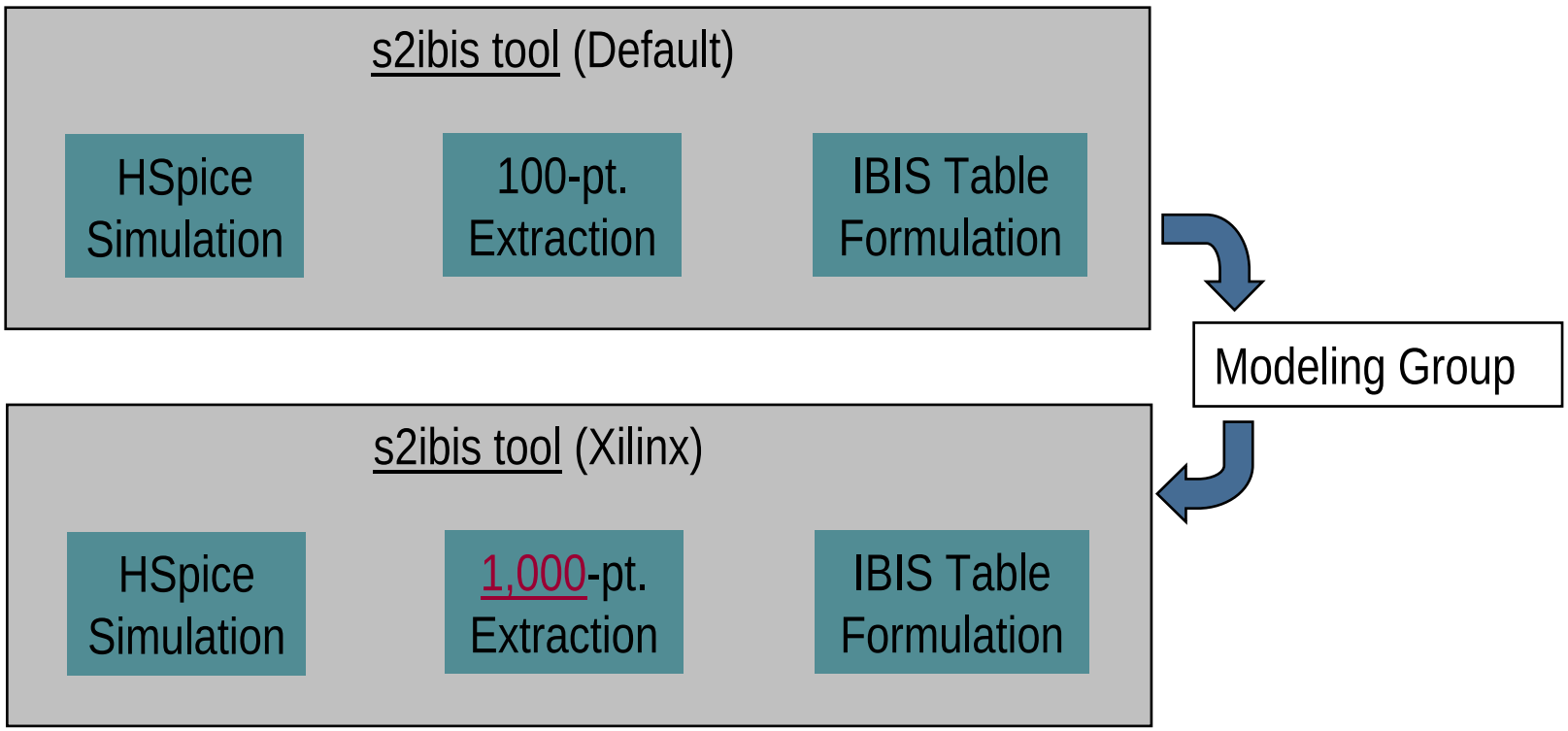
Xilinx IBIS Model Quality Update

- Correlation to Spice models
- Correlation to bench measurements
- Virtex-5™ model IQS conformance
- New activities

Xilinx IBIS Model Quality Update

Correlation to Spice models

- Improved s2ibis extraction procedure



Finer granularity yields smoother curves and better correlation.

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Correlation to Spice models

- Automation of correlation testing
  - do_sims.pl – Perl script that governs the process of fetching, patching, and running the standard I/O Spice models, for a given set of standards, in order to make automated “IBIS vs. Spice” comparison measurements.
    - do_patch – Bash shell script that does the actual patching of the Spice decks.
  - get_results.pl – Perl script that fetches the results of the Spice simulations run by *do_sims.pl*, and reformats them into *.CSV format for import into *MSExcel*.

Automation has saved much time and prevented many errors.

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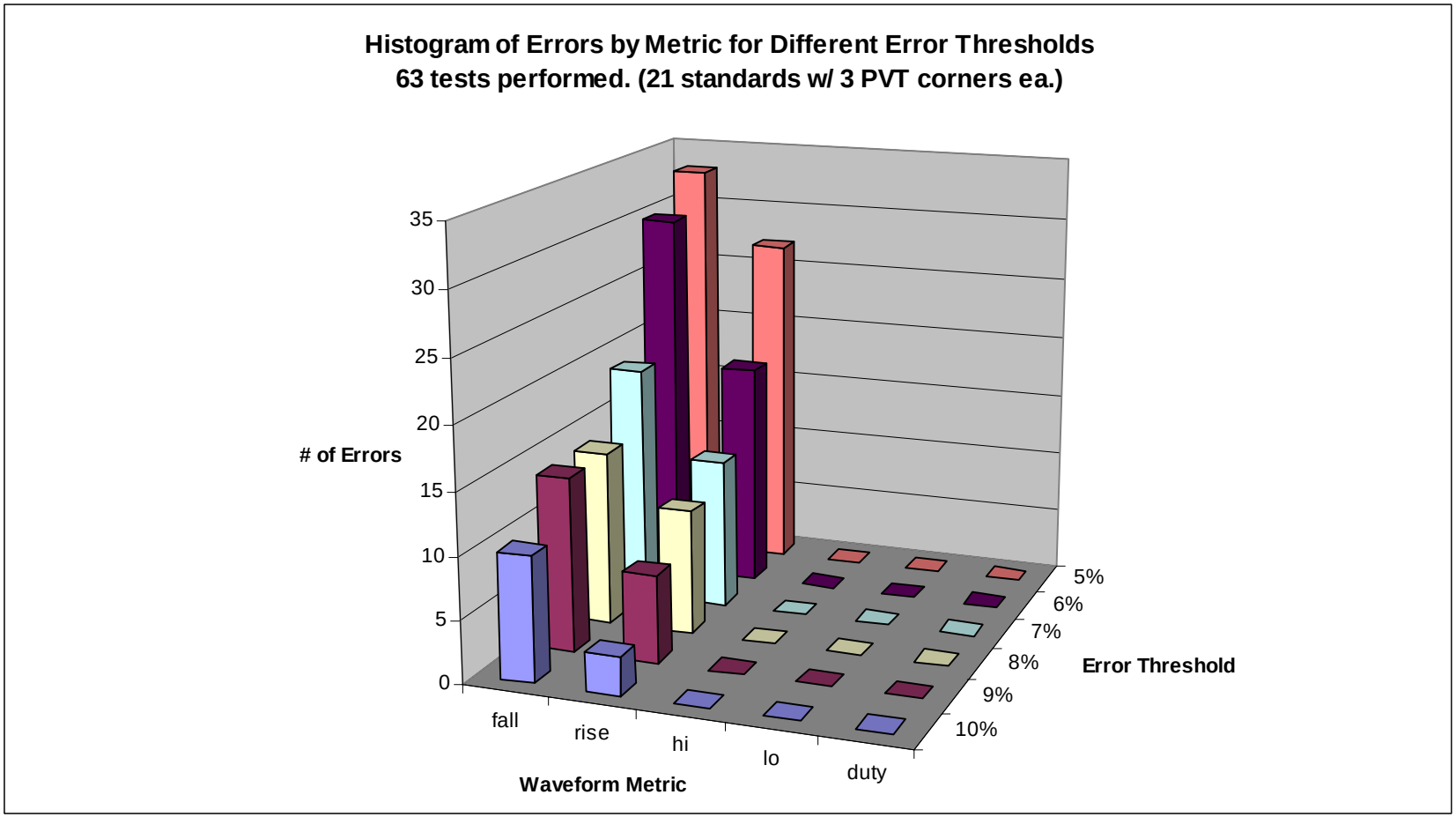
Correlation to Spice models for *virtex5.ibs* v1.9



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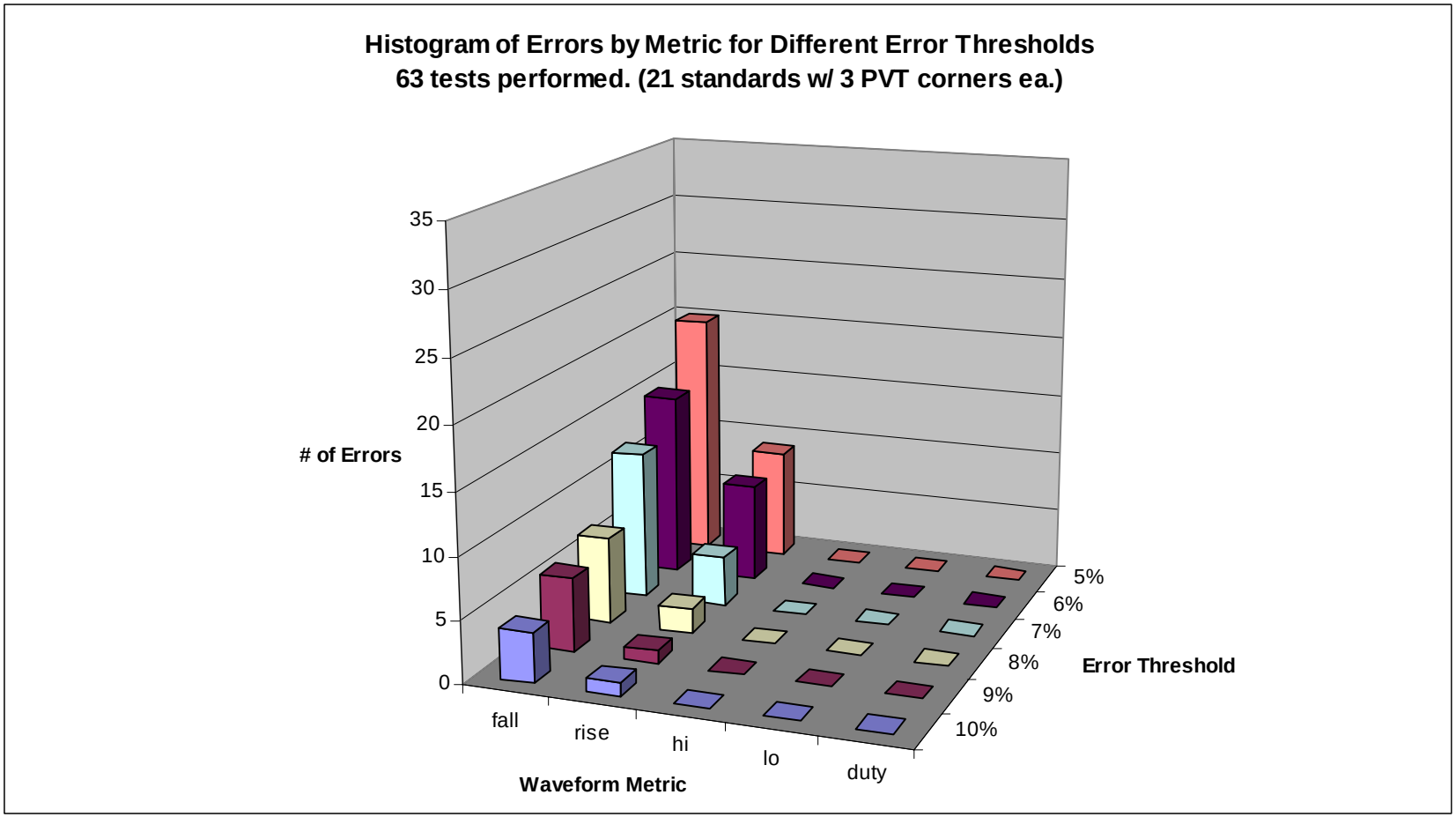
Correlation to Spice models for *virtex5.ibs* v2.6



Showing improved correlation to Spice models. Questions?

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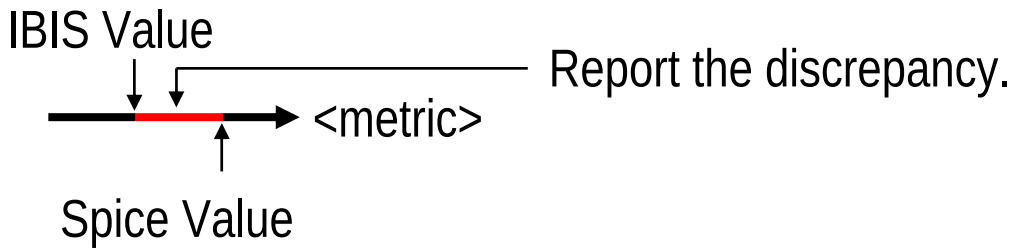
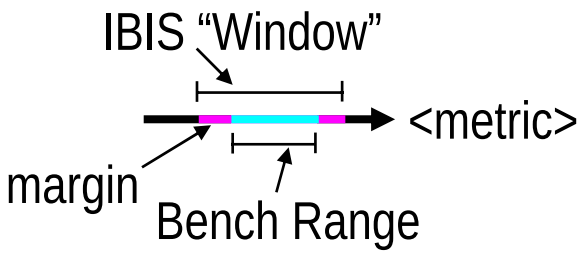
Correlation to bench measurements - Methodology

- IBIS-to-Spice:



- IBIS-to-Bench:



Check that bench range falls within IBIS window.

Two fundamentally different methodologies are used.

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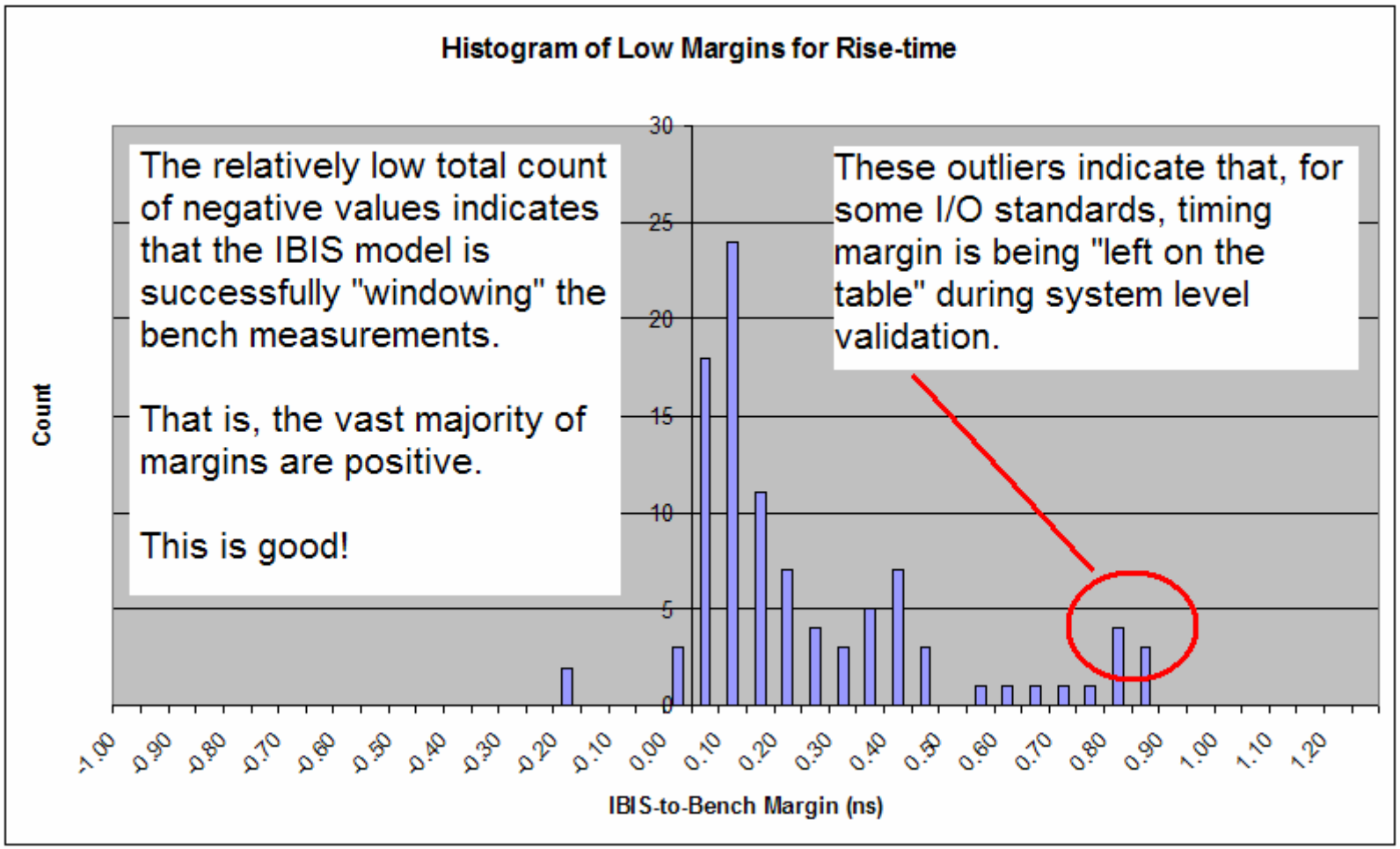
Correlation to bench measurements - Results



With the exception of the large positive outliers, this histogram is ideal.

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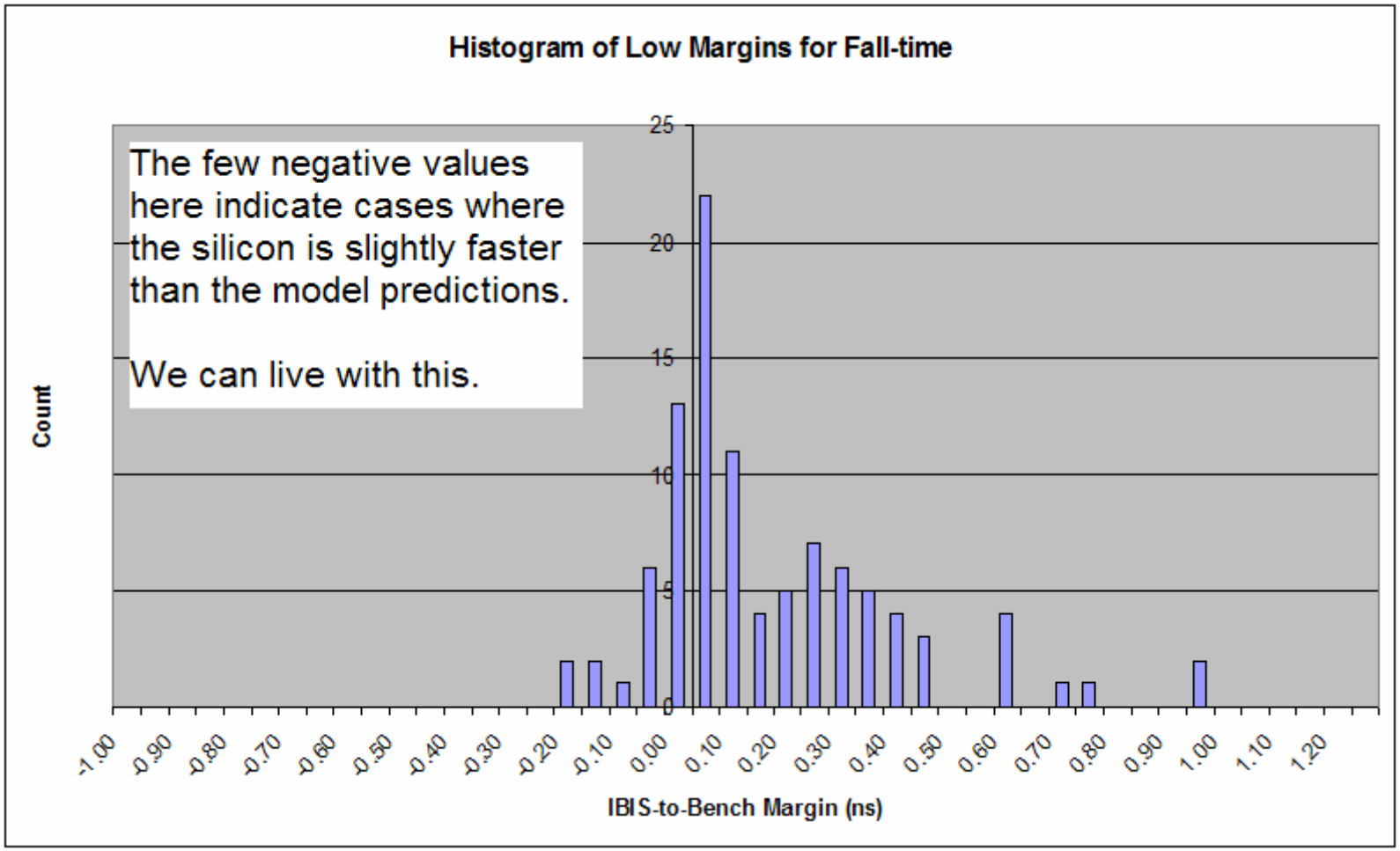
Correlation to bench measurements - Results



Negative LOW margins indicate that silicon is FASTER than the model.

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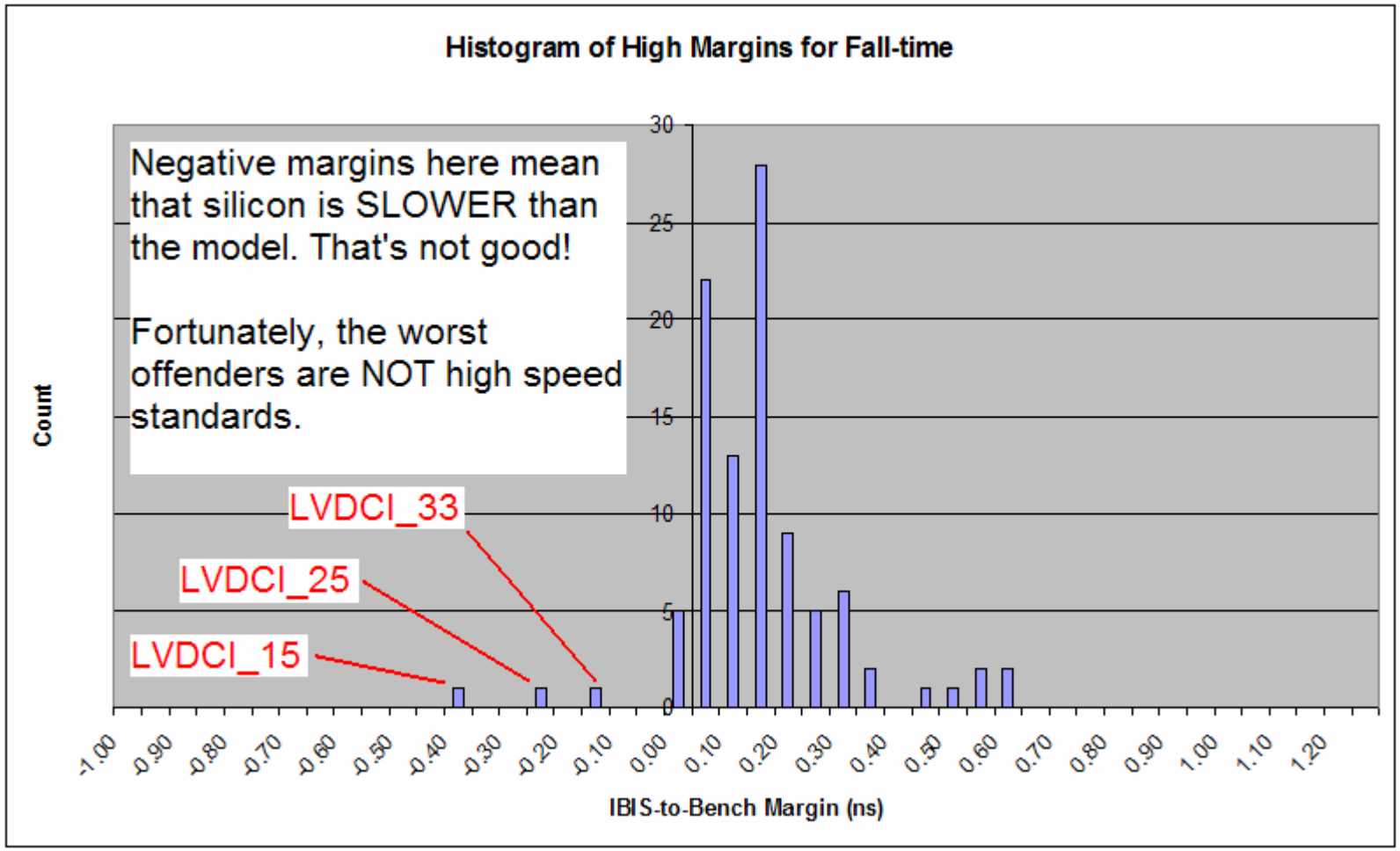
Correlation to bench measurements - Results



Negative HIGH margins indicate that silicon is SLOWER than the model.

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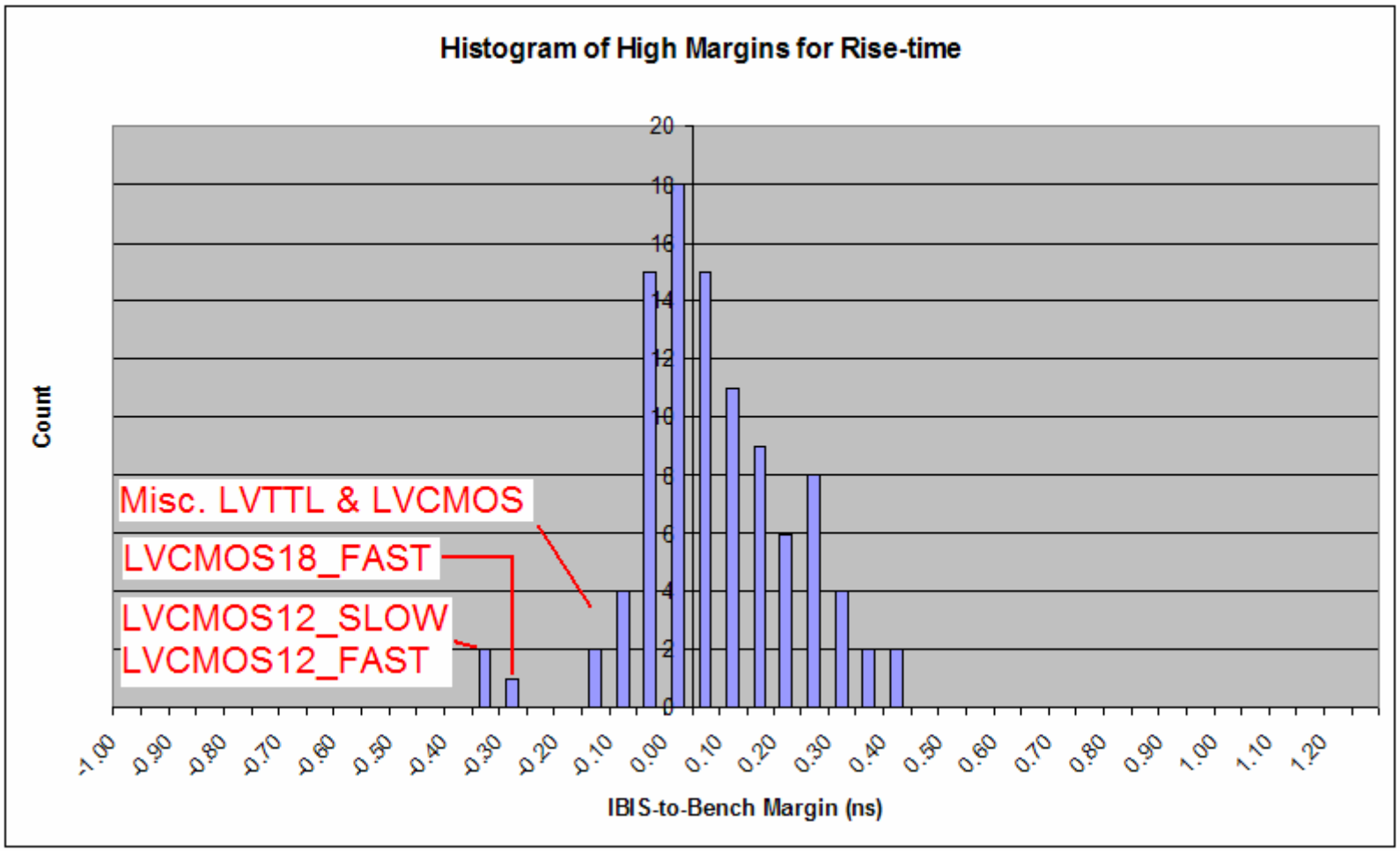
Correlation to bench measurements - Results



Again, none of the offenders are high speed standards.

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Correlation to bench measurements - Results

Questions?

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Xilinx IBIS Model Quality Update
IQS conformance

- The new standard (“v1.1”) defines 5 levels:
  - IQ0 - No checking at all.
  - IQ1 - Passes IBISCHK without errors or unexplained warnings.
  - IQ2 - IQ1 + data for basic simulation checked.
  - IQ3 - IQ2 + data for timing analysis checked
  - IQ4 - IQ3 + data for power analysis checked
- and 4 modifiers:
  - M - correlated against hardware measurements
  - S - correlated against Spice simulation
  - G - Has “golden” waveforms.
  - X - Has exceptions, commented in file.

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IQS conformance

- According to IQS v1.1ah, our current Virtex-5™ IBIS models file qualifies as IQ3SM:
  - IQ3) We pass all requirements, up to and including the new level 3 checks.
  - ‘S’) We have correlated against Spice.
  - ‘M’) We have correlated against bench measurements.

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IQS conformance

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Xilinx IBIS Model Quality Update

New activities – *release report automation*

Xilinx IBIS models file release report for: *virtex5.ibs* v2.6

Produced by: /virtex5_ibis/gen_report.pl v1.6 (Rel_2008-07-10-01)
Produced on: Tue Sep 9 12:36:07 PDT 2008

Tool version/label identified.

File name and version identified.

Contents:

- IBIS Parser Results
- Spice Correlation Results
- Bench Correlation Results

Hyperlinks to report sections.

IBIS Parser Results:

```
IBISCHK4 V4.2.0

Checking virtex5.ibs for IBIS 3.2 Compatibility...

Errors  : 0

File Passed
```

Results of parser run.

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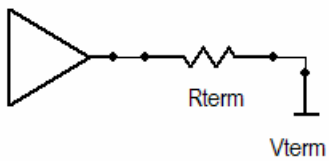
Xilinx IBIS Model Quality Update

New activities – *release report automation*

Spice Correlation Results:

Produced by: /V5_IBIS_Spice_Correlation/OUTPUTS_ONLY/SINGLE-ENDED/spice_tools/get_results.pl v1.2 (Rel_2008-07-10-01)

The following effective schematic was used to perform the simulations that generate the results in this section:



The numbers in the following table give the error in the IBIS model predictions, relative to the Spice model predictions, for certain *features* or *metrics* of the test waveform.

Errors are normalized to the Spice prediction, and expressed as a percentage of that value. In cases where the low settling values were below 1 mV, no meaningful error calculations could be made. These cases are indicated by "(n/a)".

Standard/Corner	High Level	Low Level	Rise Time	Fall Time	Duty Cycle
GTL					
tt	+00.00%	+00.02%	-00.80%	+03.19%	+00.17%
ss	+00.00%	-00.00%	-05.97%	-13.60%	-00.04%
ff	+00.00%	+00.10%	-02.87%	+05.09%	+00.27%
*** Error reading data ***					

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Tool version/label identified.

Simulation model shown, for reference.

Meaning of tabulated data is explained.

Per-standard data, with large discrepancies highlighted in red.

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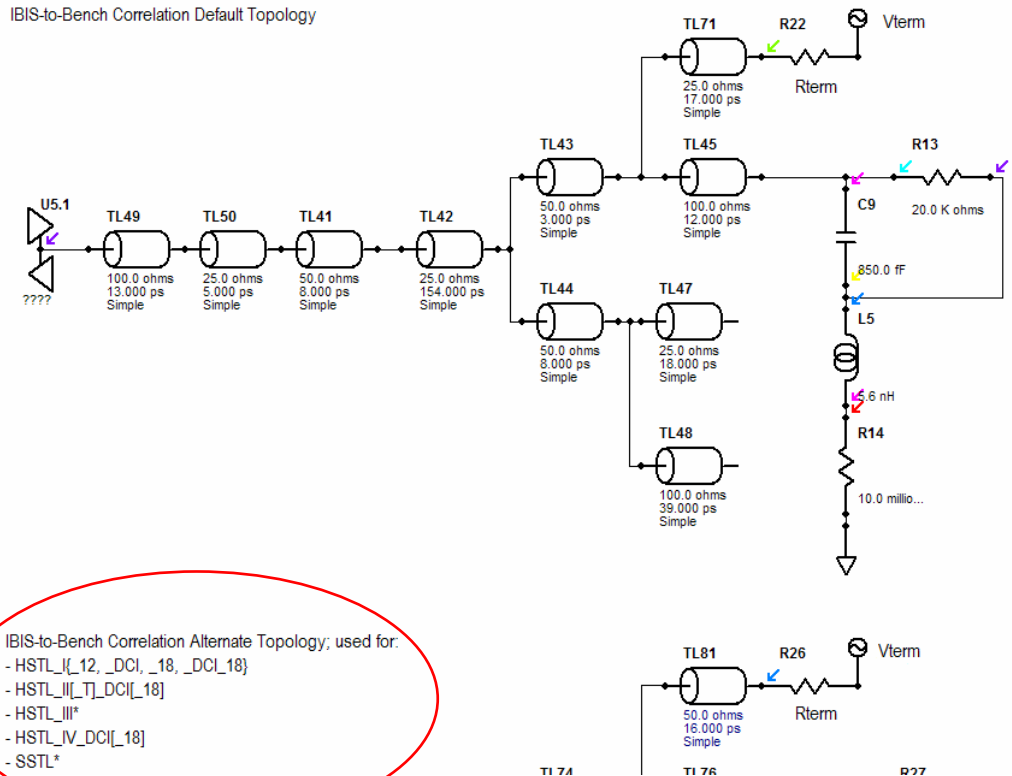
New activities – *release report automation*

Bench Correlation Results:

Produced by: /V5_IBIS_Bench_Correlation/OUTPUTS_ONLY/SINGLE-ENDED/spice_tools/get_results.pl v1.2 (Rel_2008-07-10-01)

The following effective schematics were used to perform the simulations that generate the results in this section:

IBIS-to-Bench Correlation Default Topology



IBIS-to-Bench Correlation Alternate Topology; used for:
- HSTL_I[_12, _DCI, _18, _DCI_18]
- HSTL_II[_T]_DCI[_18]
- HSTL_III*
- HSTL_IV_DCI[_18]
- SSTL*

Simulation models shown, with relevant standards identified.

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New activities – *release report automation*

The numbers in the following table give the min/max IBIS model predictions, and bench measurements, for 4 waveform *metrics*:

- High settling level
- Low settling level
- Rise-time
- Fall-time

Additionally, the *margins* between the IBIS model predictions and the bench measurements are also given. A positive margin indicates that the IBIS model prediction successfully encompassed the bench measurements, while a negative margin indicates that the bench measurements fell outside the IBIS *window*.

Finally, where available in the bench data, the predictions of the IBIS model, when run in HyperLynx, are compared to those, when run in HSpice. This provides some check on how differently the IBIS models behave when interpreted by two different IBIS simulators (i.e. – HyperLynx and HSpice's *B* element). The errors between the two are calculated as:

Error = (HyperLynx – HSpice) / HSpice

Note) voltages in Volts, and times in ns, throughout.

Standard/Metric	Low Margin	IBIS Low	Bench Low	Bench High	IBIS High	High Margin	Low Error	High Error
GTL								
Vol:	(-0.039)	(+0.191)	(+0.152)	(+0.241)	(+0.314)	(+0.073)	(-22.0%)	(-7.3%)
Voh:	No bench data available.							
Trise:	(+0.108)	(00.147)	(00.255)	(00.282)	(00.194)	(-0.088)	[n/a]	[n/a]
Tfall:	(+0.199)	(00.152)	(00.351)	(00.399)	(00.248)	(-0.151)	[n/a]	[n/a]
*** Error reading data ***								

End of Report.

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Meaning of tabulated data is explained.

Per-standard data, with negative margins highlighted in red.

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New Activities

Questions?