Modeling DDR3 with IBIS

Randy Wolff, Micron Technology

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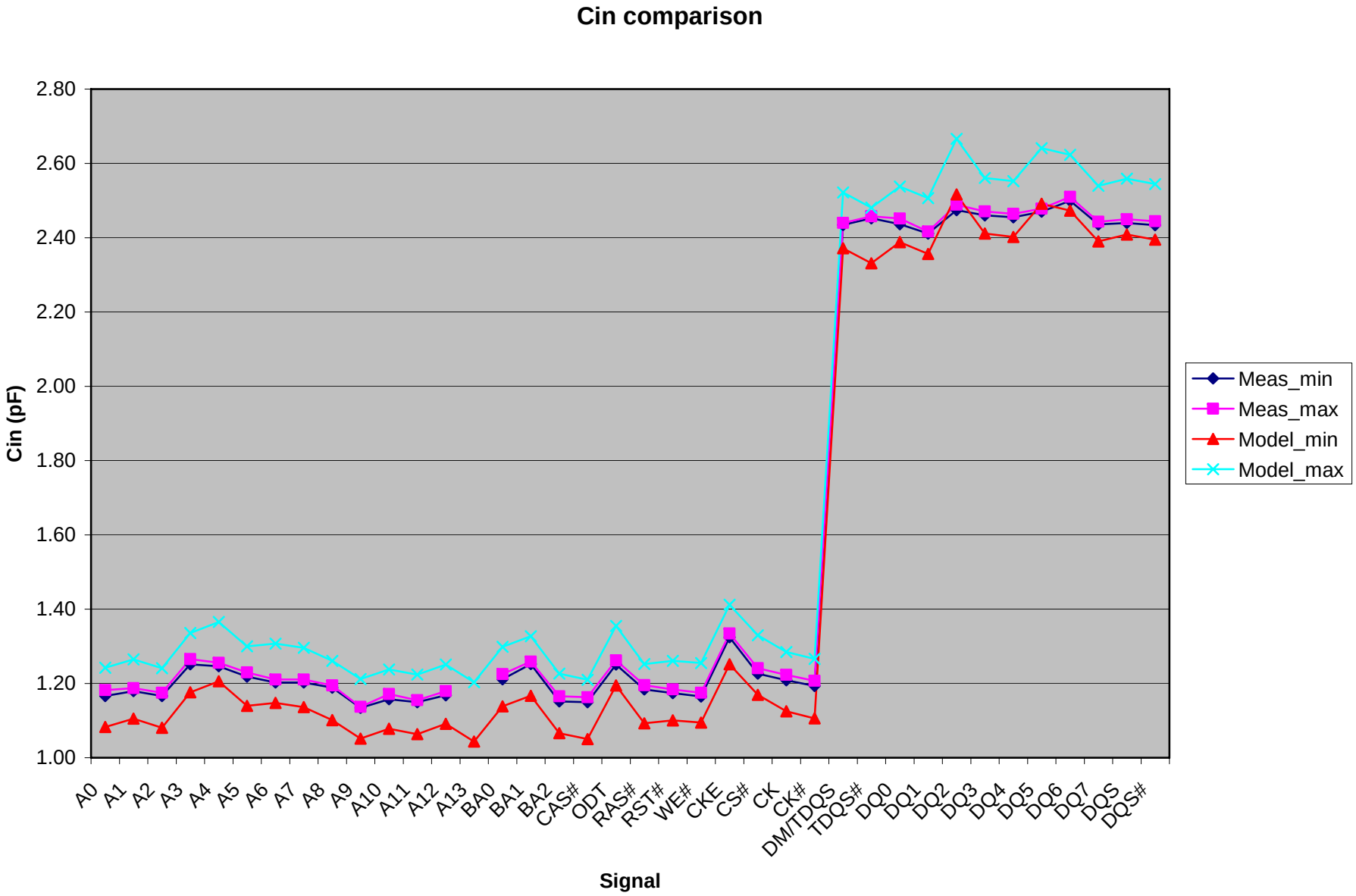
DDR3 Requirements

- Clock speeds of 400–800(+) MHz, Data rates of 800–1600(+) Mb/s
- Improvements to model accuracy needed
  - Include accurate package models
  - Properly model On-Die Termination
  - Describe V-t curves within appropriate time window
- Additions to IBIS specification

Package Models

- FBGA packages simulated with 3D Field Solver
- Custom script converts output RLC matrices to IBIS format
  - Needed to convert net names into ball names (DQ1 to A1, VSS to B1, etc.)
  - RLC matrix must then be sorted by ball ID
- Input capacitance correlated between simulation and measurement using a VNA
- Accuracy decreases if package includes on-die signal/power bussing

1Gb x8 DDR3 Input C Correlation

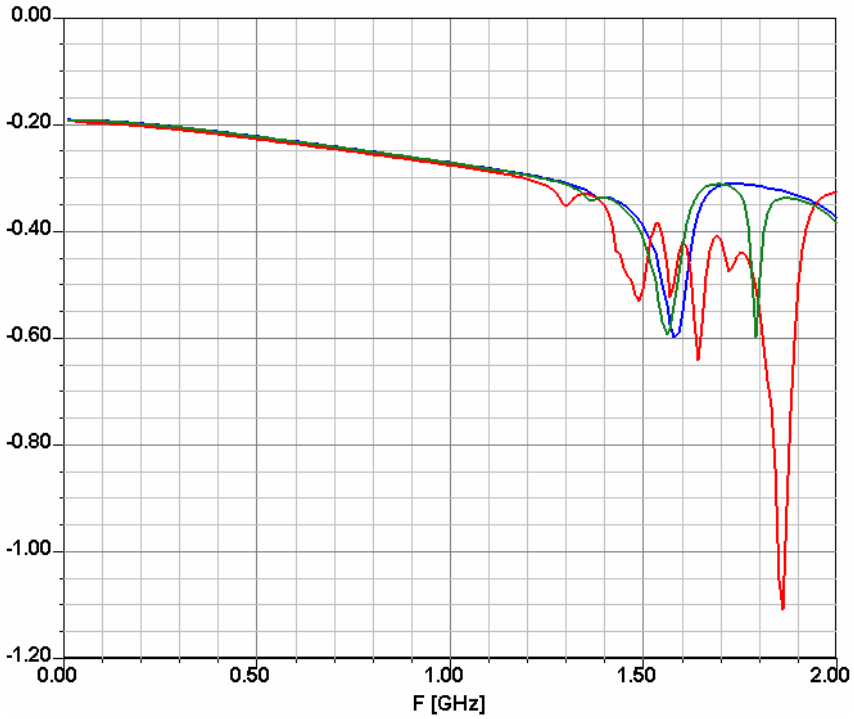


Package Models – Power supply terminal reduction

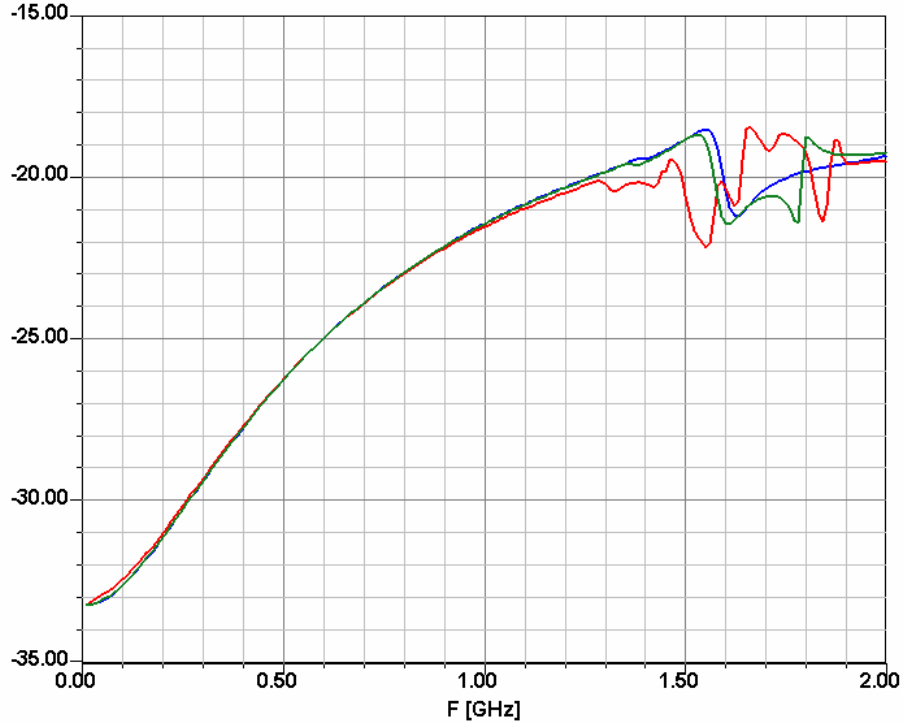
- Usually, the simulation setup used in 3D analysis is merged sinks on ball side of the package and separated sources on die pad locations.
- For IBIS modeling, multiple die terminals (sources) are not allowed
- 3D analysis completed with the following setups:
  - Regular – die pads as sources, balls as sinks (merged)
  - Reverse sink – die pads sinks (merged), balls as sources
  - Merged all – die pads as sources (merged), balls as sinks (merged)
- Frequency Domain comparison

Results (DQ0 Characteristics)

Transmission

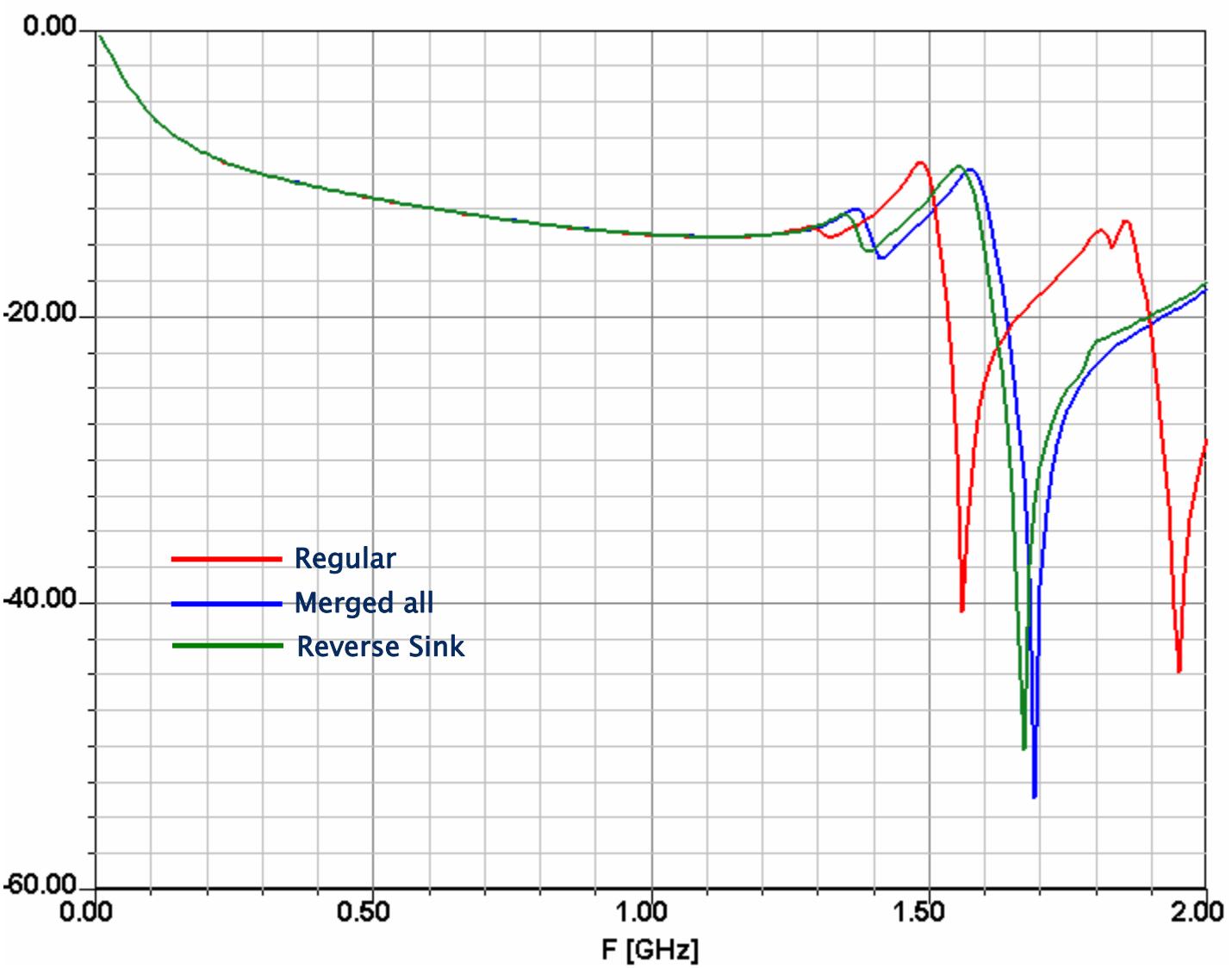


Reflection



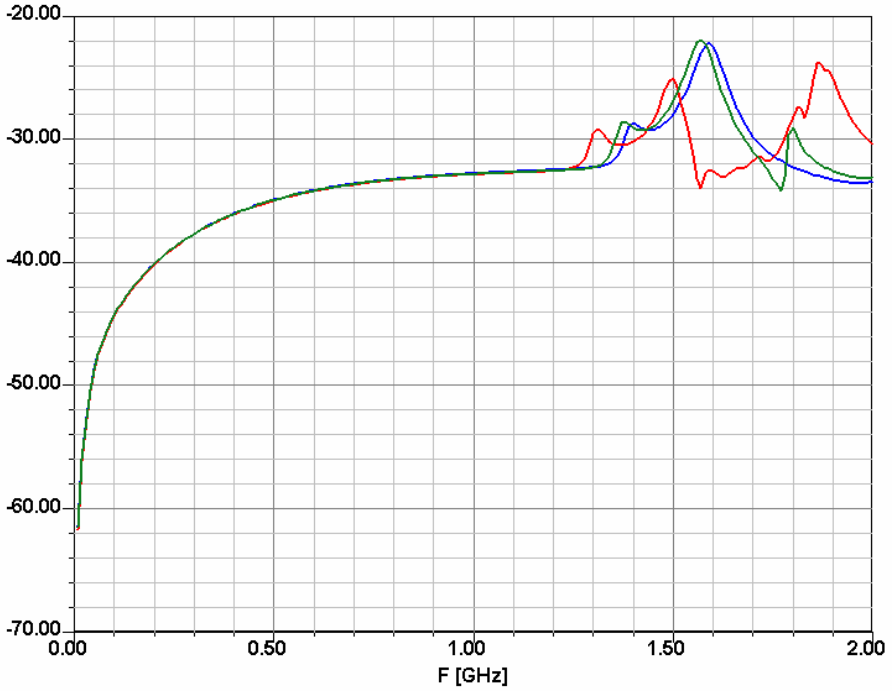
Regular
Merged all
Reverse Sink

Results (VDDQ Transmission Characteristics)

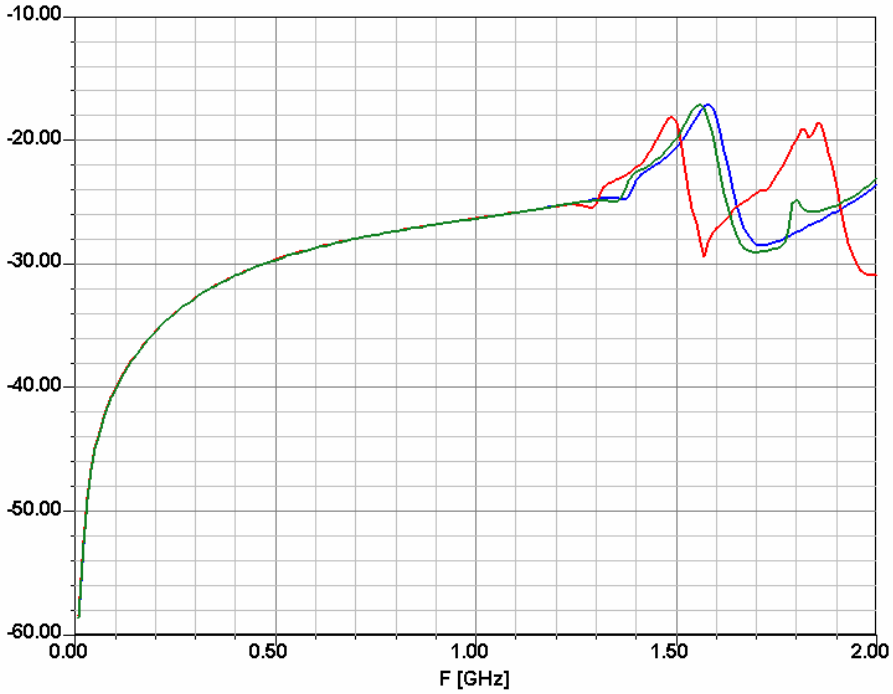


Results (DQ0–VDDQ Coupling)

Far End

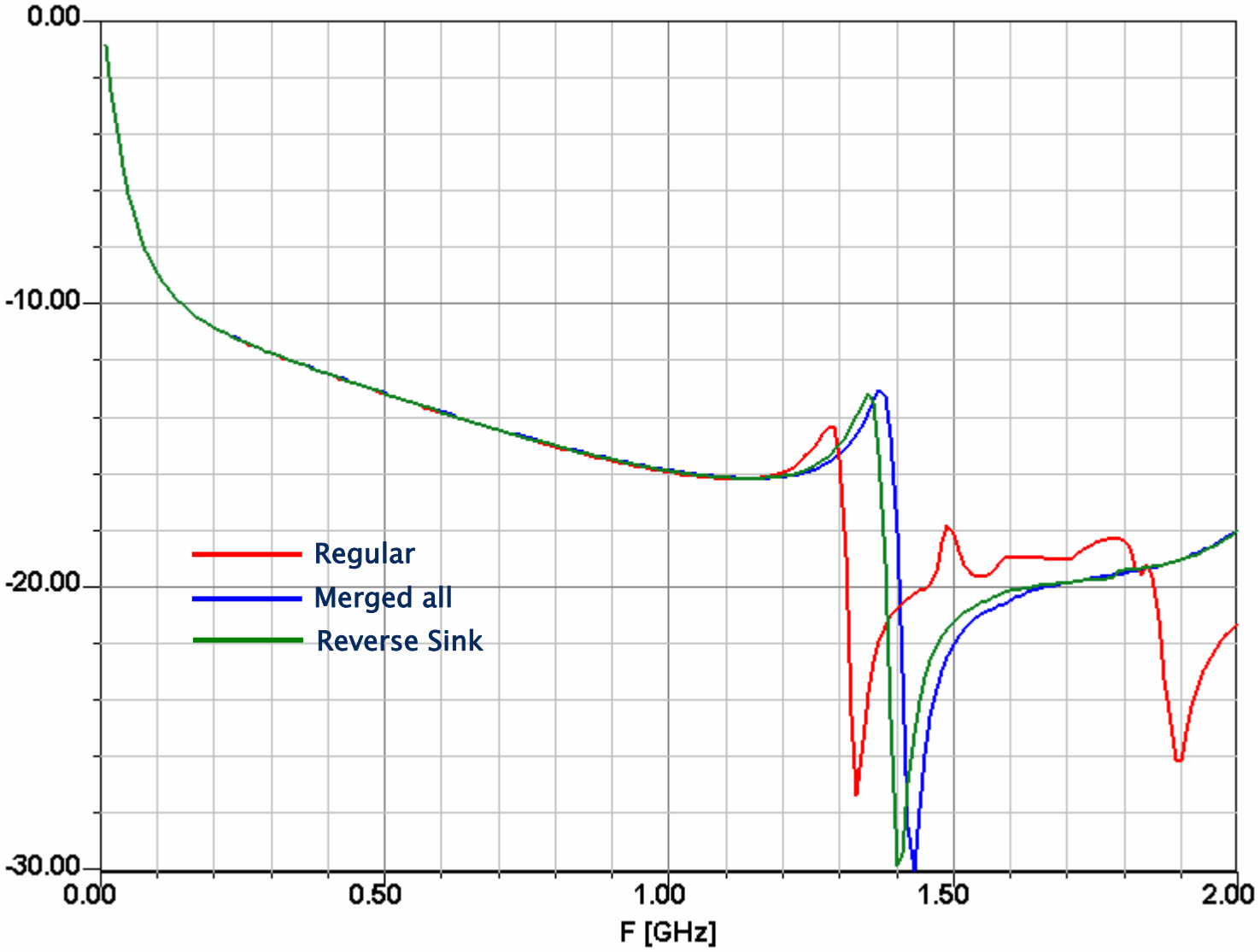


Near End



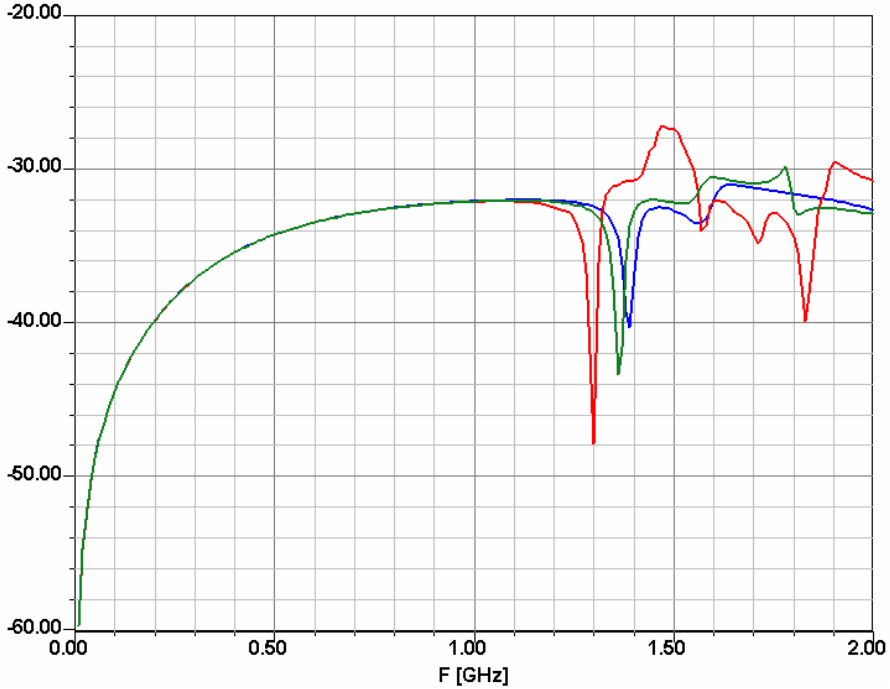
Regular
Merged all
Reverse Sink

Results (VSSQ Transmission Characteristics)

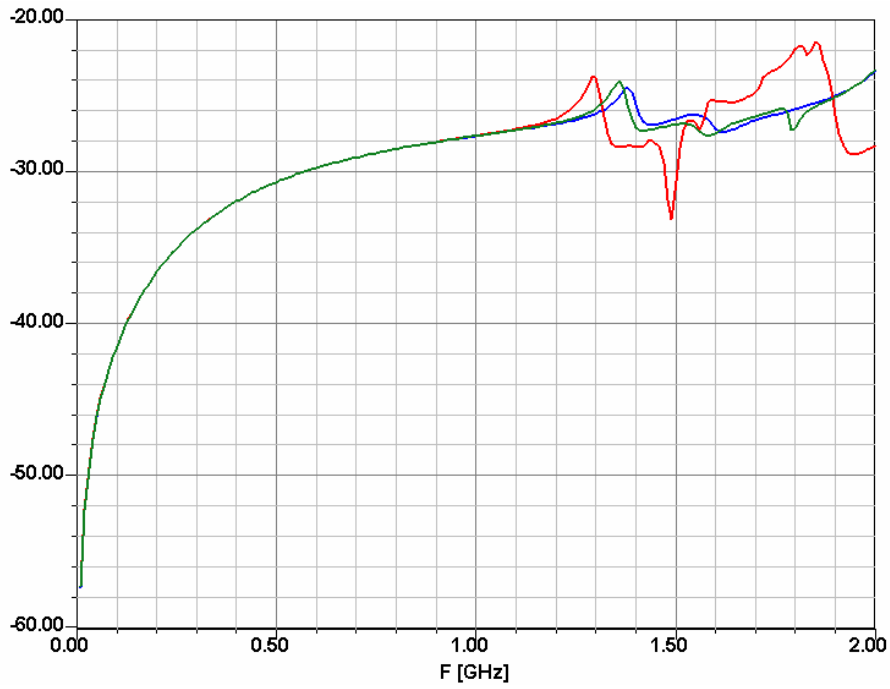


Results (DQ0–VSSQ Coupling)

Far End



Near End



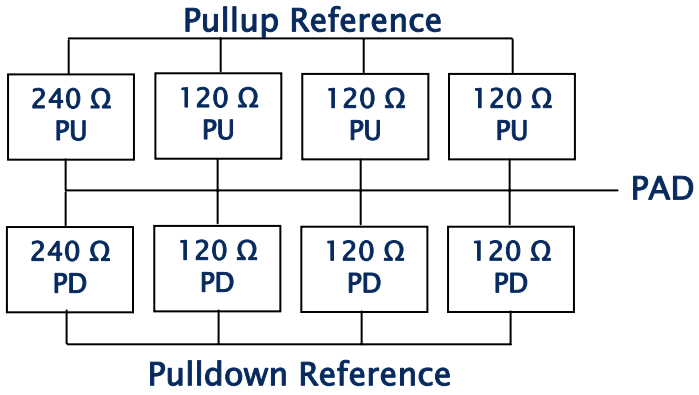
Regular
Merged all
Reverse Sink

Package Modeling Conclusions

- The three setups give very similar results up to ~1GHz
- High frequency effects are more prominent in a setup with more terminals because a model with greater number of mutual terms represents the system better.
- Merging sources and/or sinks results in sufficient accuracy

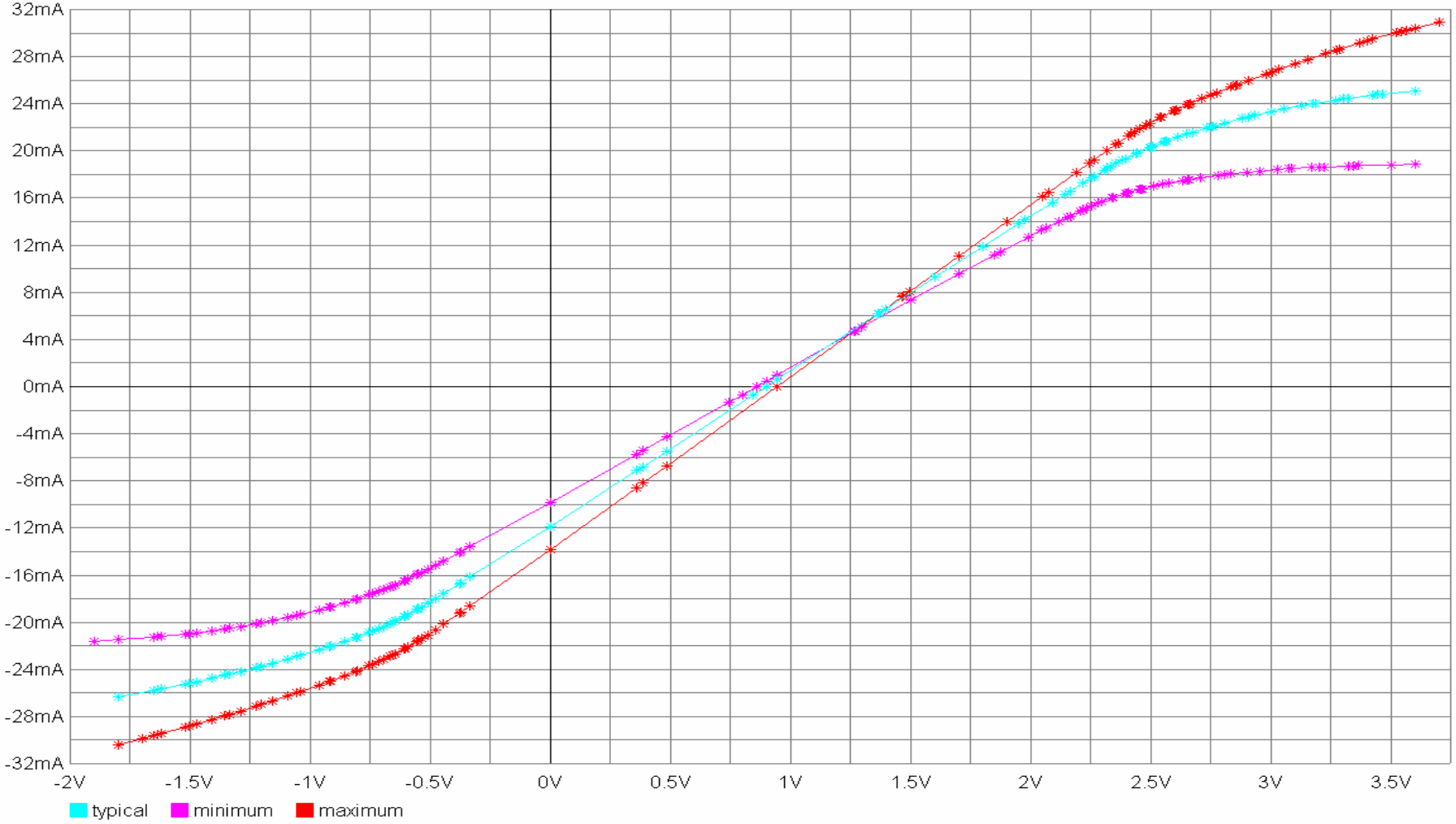
On-Die Termination Modeling

- ODT model improved with recommendations from Bob Ross' presentation "Extracting On-Die Terminators" – DesignCon East 2005
- Old methodology used Clip-and-Extend
- New methodology correctly models ODT structure for proper power supply referencing



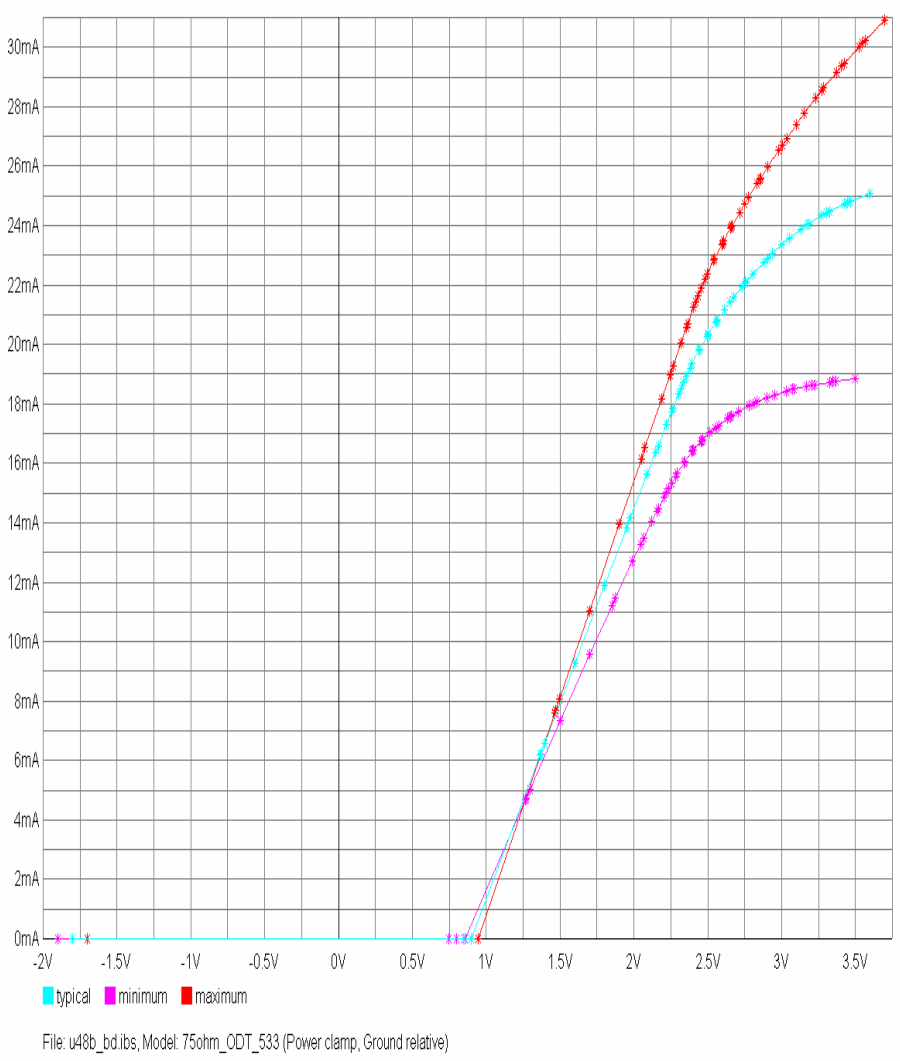
ODT Modeling – DDR2

Combined Clamp Curves

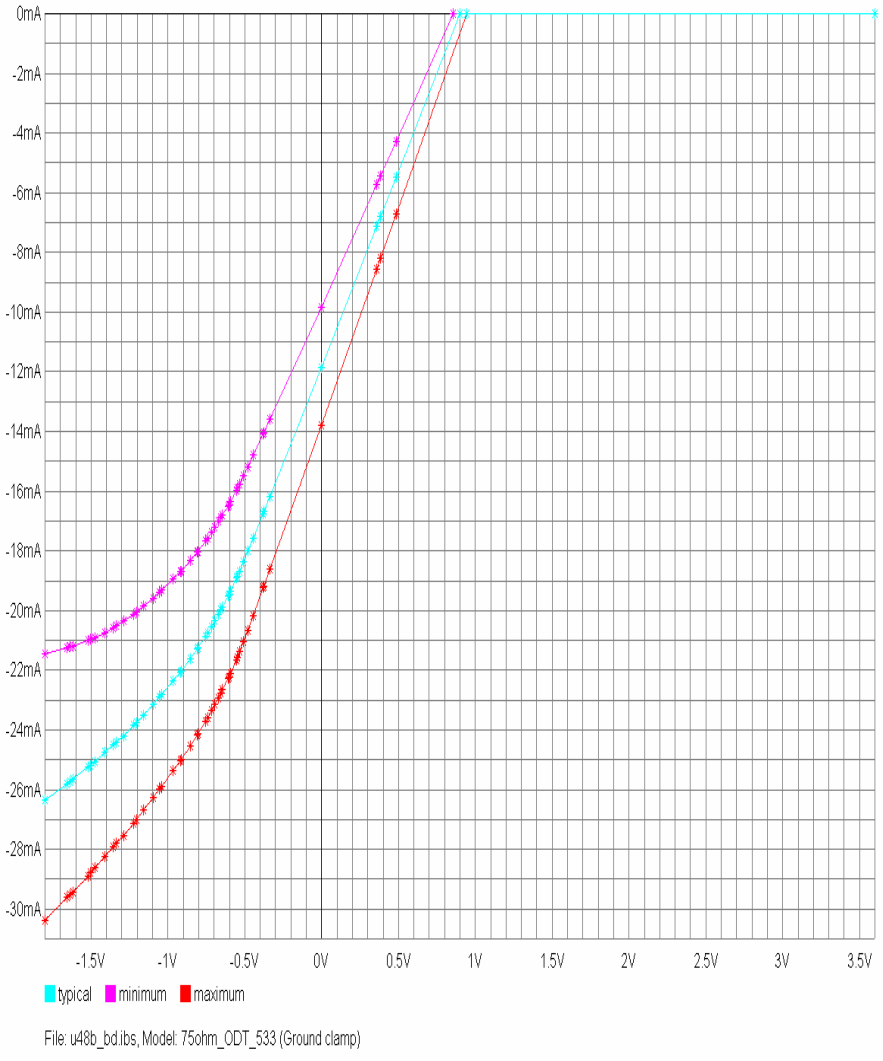


ODT Modeling – DDR2

Power Clamp

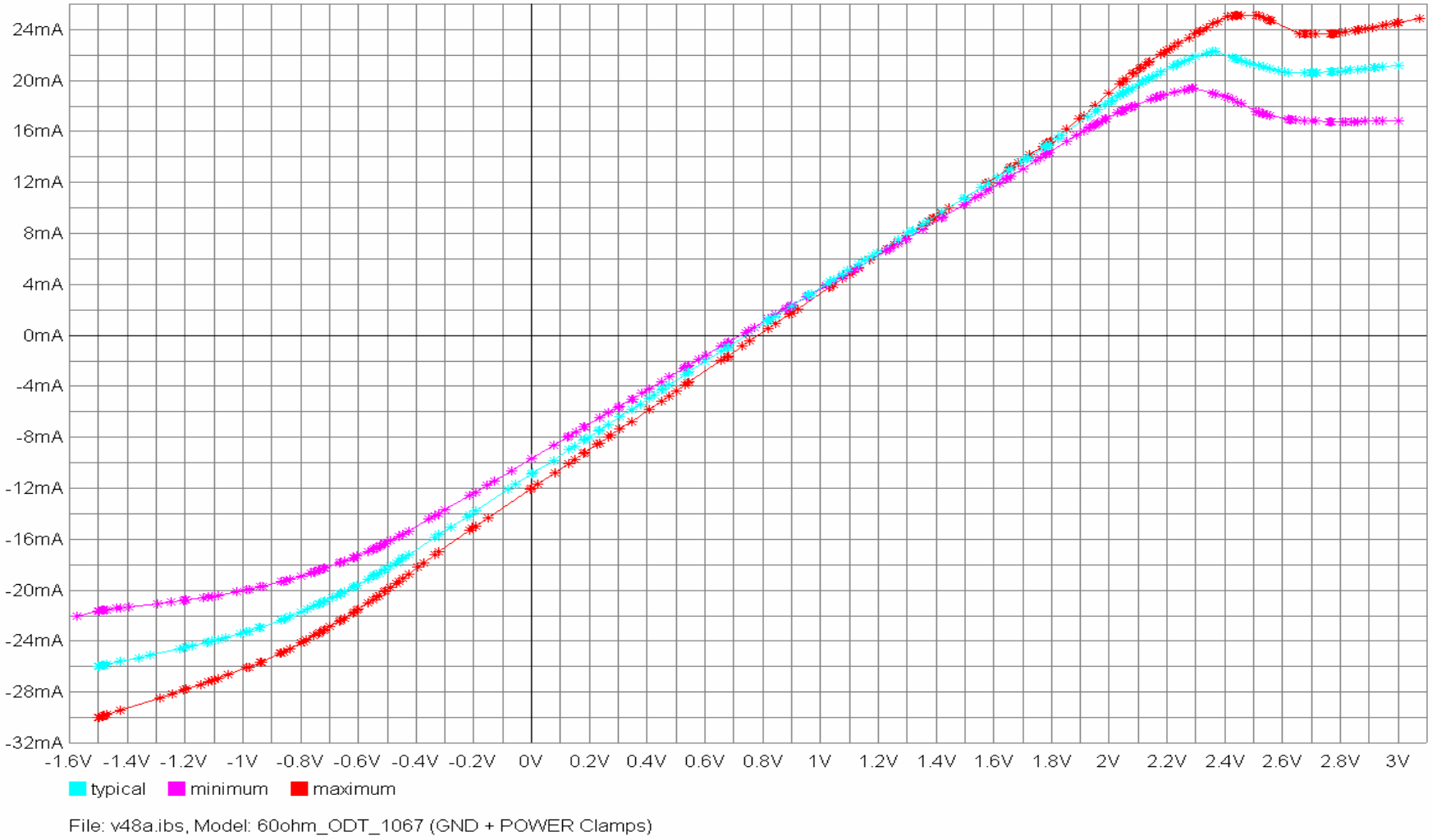


Ground Clamp



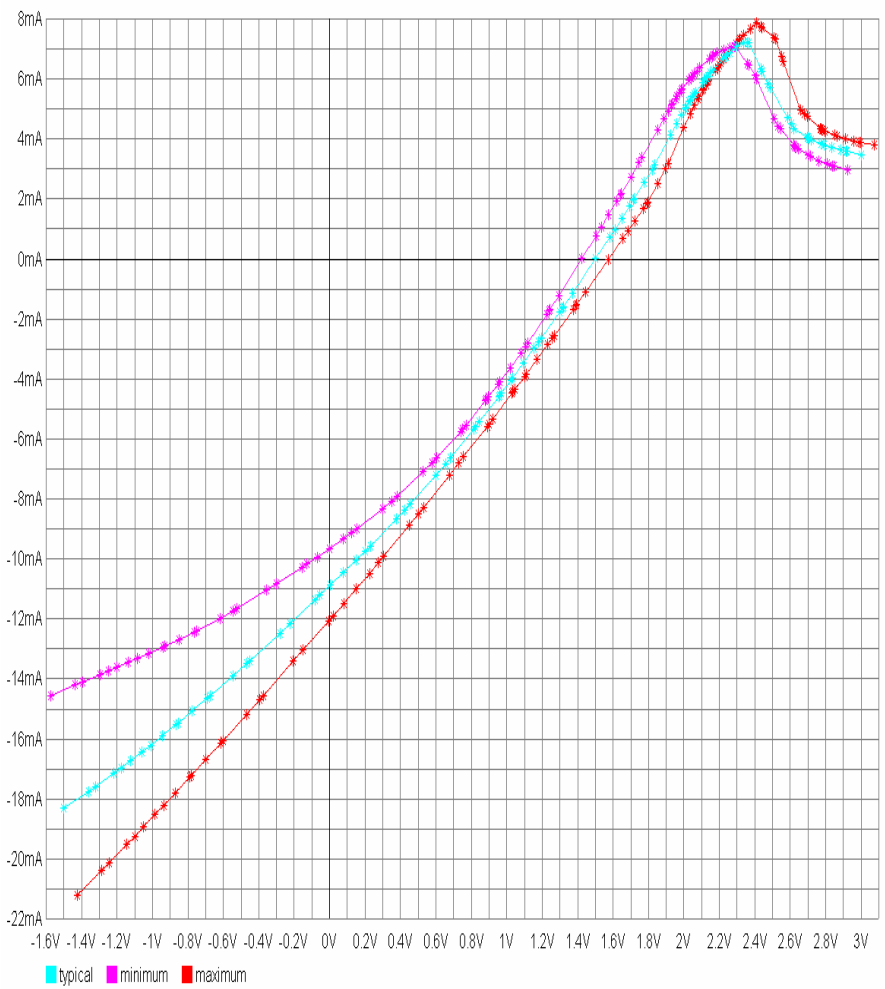
ODT Modeling – DDR3

Combined Clamp Curves



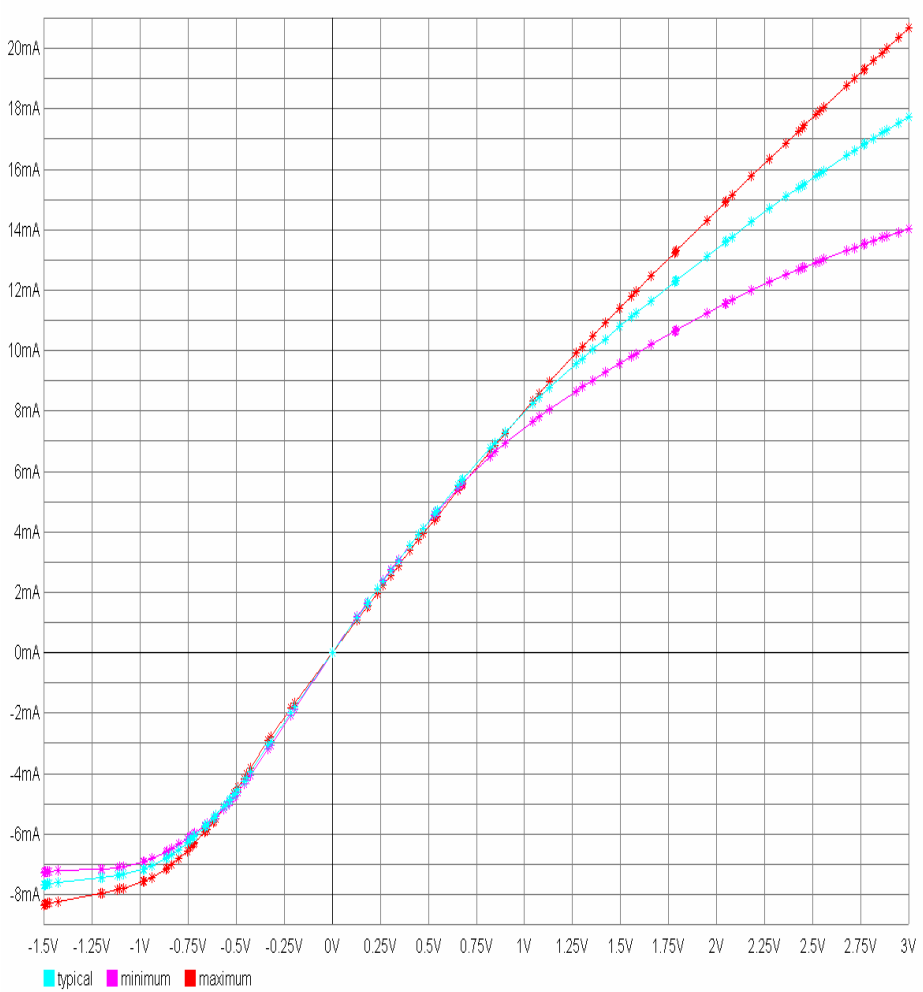
ODT Modeling – DDR3

Power Clamp



File: v48a.ibs, Model: 60ohm_ODT_1067 (Power clamp, Ground relative)

Ground Clamp



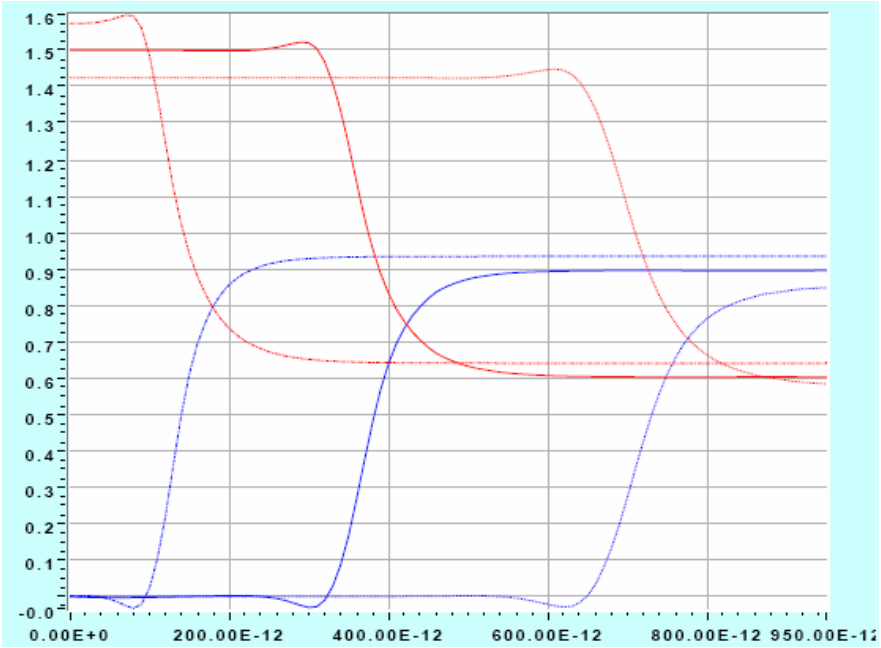
File: v48a.ibs, Model: 60ohm_ODT_1067 (Ground clamp)

V-t Curve Time Shifting

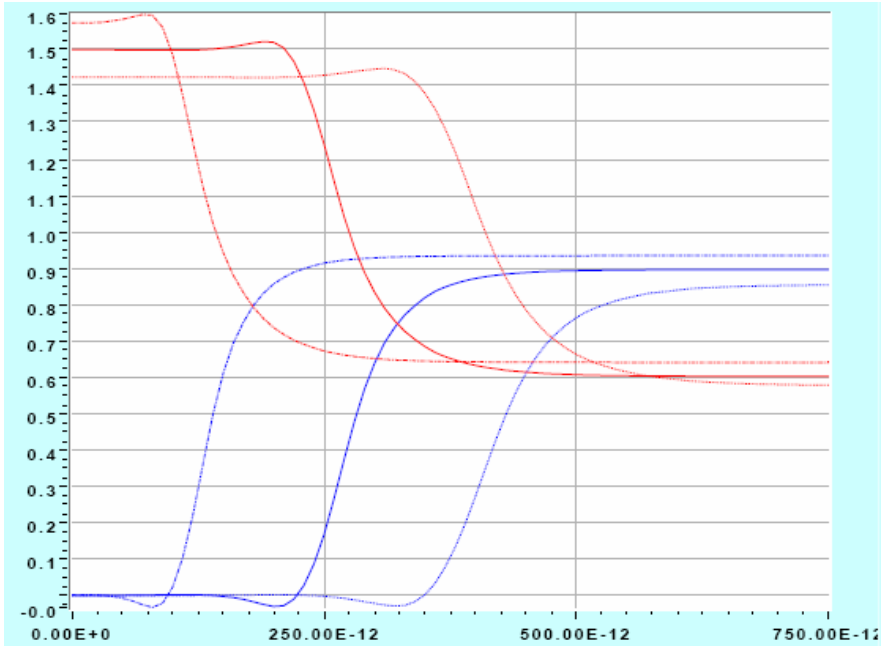
- V-t curve time window for DDR3-1333 is 750ps
- Typical V-t curve extraction (correlated across slow/typ/fast to the same clock stimulus) requires ~950ps to capture all corner cases
- 950ps reduces effective data rate to 1050 Mbps
- Time shifting all typical and minimum waveforms by t_{shift}(typ) and t_{shift}(min) reduces time window to 750ps
- To correlate with original SPICE model, IBIS stimulus is delayed by t_{shift}(typ) or t_{shift}(min)

V-t Curve Time Shifting

Original model with 950ps time window



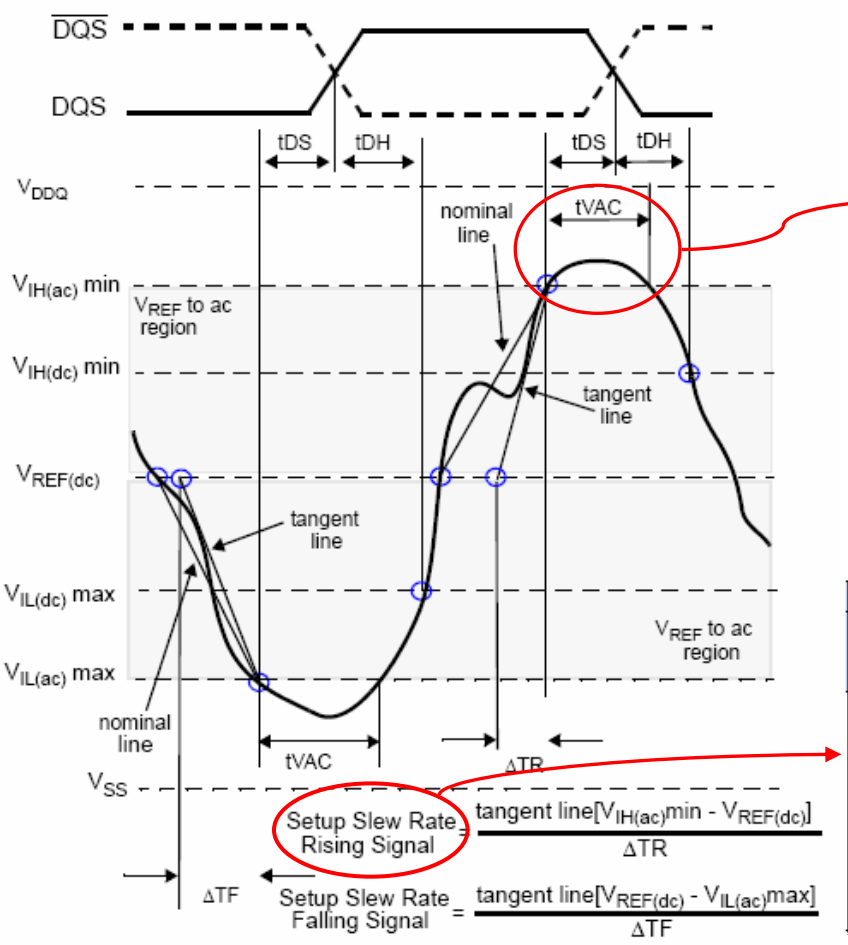
Time Shifted model with 750ps time window



DDR3 IBIS Spec Improvements

- IBISCHK 4.2 parser adoption
  - Fixes [Receiver Thresholds] differential measurement issues
- Lossy C_comp needed to improve correlation to SPICE and measurements
- Additions needed to the IBIS specification for DDR3 timing measurements
  - Slew rate derating
  - t_{VAC}

DDR3 t_{VAC} and Slew Rate Derating



Required time t_{VAC} above VIH(ac) {below VIL(ac)} for valid transition

Slew Rate [V/ns]	t_{VAC} [ps]	
	min	max
> 2.0	75	-
2.0	57	-
1.5	50	-
1.0	38	-
0.9	34	-
0.8	29	-
0.7	22	-
0.6	13	-
0.5	0	-
< 0.5	0	-

ΔtDS, ΔDH derating in [ps] AC/DC based [1]

		DQS, DQS# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	88	50	88	50	88	50	-	-	-	-	-	-	-	-	-	-
	1.5	59	34	59	34	59	34	67	42	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	-2	-4	-2	-4	6	4	14	12	22	20	-	-	-	-
	0.8	-	-	-	-	-6	-10	2	-2	10	6	18	14	26	24	-	-
	0.7	-	-	-	-	-	-	-3	-8	5	0	13	8	21	18	29	34
	0.6	-	-	-	-	-	-	-	-	-1	-10	7	-2	15	8	23	24
	0.5	-	-	-	-	-	-	-	-	-	-	-11	-16	-2	-6	5	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-30	-26	-22	-10

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- Comments?
- Questions?