EIA IBIS Open Forum Summit Minutes

Meeting Date: **February 7, 2008**

GEIA STANDARDS BALLOT VOTING STATUS
See last page of the minutes for the voting status of all member companies.

VOTING MEMBERS AND 2008 PARTICIPANTS

Agilent	Sanjeev Gupta*, Radek Biernacki*, Amolak Badesha* Fangyi Rao*, Ian Dodd*, Yutao Hu*, Vuk Borich* Nobutaka Arai*
AMD	Nam Nguyen
Ansoft Corporation	Steve Pytel*
Apple Computer	(Bill Cornelius)
Applied Simulation Technology	(Fred Balistreri)
ARM	(Nirav Patel)
Cadence Design Systems	Terry Jernberg, Hemant Shah*, Ambrish Varma* C. Kumar*
Cisco Systems	Syed Huq*, Mike LaBonte, AbdulRahman (Abbey) Rafiq* Huyen Pham*, Emily Yao*, Susmita Mutsuddy* John Fisher*, Paul Ruddy*, Jun Li*, Jianmin Zhang* Luis Boluna*, Kelvin Qiu*, Jane Lim*, Ilyoung Park* Rick Brooks*, Chris Padilla*, Ehsan Kabir*
Ericsson	Anders Ekholm*
Freescale	Jon Burnett*
Green Streak Programs	(Lynne Green)
Hitachi ULSI Systems	Kazuyoshi Shoji*
Huawei Technologies	Tao Guan, Xiaoqing Dong*
IBM	Adge Hawes*
Intel Corporation	Michael Mirmak*, Rich Mellitz*
IO Methodology	Lance Wang*, Zhi (Benny) Yan*, Li (Kathy) Chen*
LSI	[Frank Gasparik], Brian Burdick, Kim Helliwell*
Mentor Graphics	Arpad Muranyi*, John Angulo*
Micron Technology	Randy Wolff*
Nokia Siemens Networks GmbH	Eckhard Lenski
Panasonic	(Atsuji Ito)
Samtec	Jim Nadolny*, Justin McCalister*
Signal Integrity Software	Mike Steinberger*, Walter Katz*, Todd Westerhoff* Doug Burns*, Mike Mayer*, Barry Katz*
Sigrity	Sam Chitwood*
STMicroelectronics	(Anil Kalra)
Synopsys	Ted Mido*
Teraspeed Consulting Group	Bob Ross*, Tom Dagostino*, Al Neves*
Texas Instruments	Richard Ward*

Toshiba	(Yasumasa Kondo)
Xilinx	David Banas*, Ajay Shah*, Suzanne Yiu* Mustansir Fanaswalla*
ZTE	(Ying Xiong)
Zuken	(Michael Schaeder)

OTHER PARTICIPANTS IN 2008

Aeroflex Metelics	David Nguyen*
Aica Kogyo	Akihiro Tanaka*
Altera	Ravindra Gali*, Jing Wu*, John Oh*, Hui Fu*
Avago Technologies	Minh Quach*, Sari Tocco*
Bayside Design	Elliot Nahas*, Kevin Roselle*
Celestica	Ihsan Erdin*
ECL Advantage	Thomas Iddings*
Elma Bustronic	Michael Munroe*
Exar	Helen Nguyen*
Flextronics	Hasnain Syed*
GEIA	(Chris Denham)
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ICT Solutions	Steven Wong*
NetLogic Microsystems	Eric Hsu*
Nuova Systems	Zhiping Yang*
Physware	Marc Kowalski*
Siemens AG	Manfred Maurer*
Simberian	Yuriy Shlepnev*
Tektronix	Steve Corey*
Tyco Electronics	Chad Morgan*
Vertical Circuits	Mark Egbers*
Xsigo Systems	Robert Badal*
Independent	Guy de Burgh*, Ardy Forouhar*, Dave Galloi* Kazuhiko Kusunoki*

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Telephone Number	Meeting ID
February 22, 2008	1-866-432-9903	1-2192-6609
March 14, 2008	-- IBIS Summit at DATE; no teleconference --	

All meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically

distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, press 1 to attend the meeting, then follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

INTRODUCTIONS AND MEETING QUORUM

The IBIS Open Forum Summit was held in Santa Clara, California at the Santa Clara Convention Center during the 2008 DesignCon Conference. About 90 people representing 41 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.eda-stds.org/ibis/summits/feb08/

Michael Mirmak opened the meeting by welcoming the attendees. He thanked Cisco for sponsoring the event and Mentor Graphics for help with the booth. He then asked people to identify if they were from EDA companies, were model producers or were system designers. In total, 89 people from 40 organizations attended the summit.

Michael then reviewed the agenda. Arpad Muranyi asked about the official date listed for the DATE summit meeting. Michael confirmed that the correct date is Friday, March 14, 2008.

IBIS CHAIRS REPORT AND ROADMAP

Michael Mirmak, Intel Corporation

Michael began by highlighting recent achievements. He noted approval of BIRD104.1 and BIRD98.3. Touchstone 2.0 is in final review with a vote likely before Q2'08. Progress continues on the IBIS Quality Specification 1.1. Successful summits were held in Beijing and Tokyo. A Taipei summit is part of the 2008 summit series. He then talked about organizational status. He noted changes to EIA including a merger of GEIA and ITAA. 2007 closed with a positive budget and 32 members. 2008 dues are increased to $900 per organization.

Michael then discussed IBIS 5.0. He showed a list of BIRDs that have been approved and proposed BIRDs under development. Proposed BIRDs include ICM-IBIS linking, improved differential measurements, [External Model] under [Circuit Call], and SPICE parameter passing. Michael wants to target a draft specification by Q3'08. Arpad Muranyi commented that in previous versions, the x.0 specification usually was a major revision but may have BUGs that are fixed in minor revisions. Arpad thought we could target IBIS 5.0 to include the approved BIRDs and cover other BIRDs in a minor revision. This would be a similar approach to IBIS 4.0 and IBIS 4.2. Michael noted that this may create difficulties in creating the parser. Hemant Shah suggested that our development is too slow and we should start on IBIS 5.0 immediately. Jon Burnett asked if all the approved BIRDs in the list cover power integrity improvements. Michael thought that they did. Michael encouraged further comments.

WAVEFORM COMPARISON AND S2IBIS3 ROADMAP

Lance Wang, IO Methodology

Lance began by talking about waveform comparisons between SPICE and IBIS models as a way of determining and improving IBIS quality. In waveform comparisons, one is interested in vertical differences such as voltage or current and horizontal differences of timing. He defined peak difference value, index and average difference value, and index. Lance noted that his formulas for these parameters are patent pending. He then showed the formulas for Differential Peak (DP), Differential Peak Index (DPI), Differential Average (DA), Differential Average Index (DAI), Timing Differential Peak (TDP) and Timing Differential Average (TDA).

Lance then shifted topics to discuss the S2IBIS3 roadmap. S2IBIS3 was developed and supported by NCSU, but IO Methodology is taking over support of the software. The software will remain free. Lance plans to enhance S2IBIS3 to support [Model Selector], Submodels, manipulating V-t and I-V curves with a best–fit algorithm, single corner generation, BIRD95 and BIRD98, differential pairs, a GUI addition, and parser integration. Arpad Muranyi suggested adding capability to create corner cases by scaling a typical corner. Anders Ekholm suggested adding capability to create a golden waveform. Rich Mellitz suggested looking at a Lissajou pattern comparison metric.

MODELING DDR3 WITH IBIS

Randy Wolff, Micron Technology

Randy began by noting the need for increased accuracy with DDR3 models due to the faster data rates of DDR3 in comparison to DDR2. One area of improvement in Micron's DDR3 models is the addition of package models including RLC matrices. He showed that the 3D field solver used to model the package parasitics shows excellent correlation to VNA measurements. He then showed results of a study of reduction of power supply terminals. He noted that packages include multiple power supply connections at the die side, but IBIS allows only one die-side connection for each power supply. A 3D analysis was completed with different combinations of source and sink nodes merged. The results showed that merging the die side nodes agreed with the non-merged case up to about 1 GHz. High frequency effects were more prominent in a setup with more terminals, because a model with greater number of mutual terms represents the system better.

Randy then gave recommendations on how to model On-Die Termination properly for DDR3. He referenced a presentation made by Bob Ross at DesignCon East 2005. He compared DDR2 models using a clip-and-extend methodology with the new DDR3 models. The new methodology correctly models ODT structure for proper power supply referencing.

Randy noted that DDR3 models require short V-t time windows – 750 ps for DDR3-1333. A typical V-t extraction across slow, typical and fast corners requires about 950 ps to capture all corners. By time shifting the typical and minimum corners, the time window can be reduced to 750 ps.

Randy then covered improvements needed to the IBIS specification to cover DDR3 models. These include slew rate derating, t_{VAC}, lossy C_comp, and full support of IBISCHK4.2 from EDA software vendors.

David Banas asked if there is momentum in the industry to move towards timing at the device pad instead of the current timing at the pin. Randy commented that he was not aware of any industry groups working towards this.

PROPER IBIS PACKAGE MODELING TECHNIQUES AND USAGE IN IDEAL PDS AND SSO SIMULATIONS

Sam Chitwood, Sigrity

Sam began by reminding the audience of assumptions in IBIS package models. These include the 1:1 relationship between die pads and board pins, RLCs allowed for power and ground pins, and [Pin Mapping] connecting pullup, pulldown, and clamps to actual power and ground locations. He noted that his talk focuses on techniques applied to BGA type packages that have multiple power and ground nets with plane routing. He then covered use of the [Pin] list and limitations of using [Pin] for PDS modeling. PDS simulation is severely limited with the [Pin] list due to absence of mutual terms. He then discussed limitations of [Pin] for signal modeling. He detailed the proper methods for extracting [Pin] resistance, inductance, and capacitance. Use of the advanced package model allows for non-ideal PDS simulation when the RLC matrix format is used. It is important to ensure passivity if coupling terms are removed. He defined a methodology for proper [Model Data] extraction and correct usage of [Model Data]. He showed a chart of IBIS package model accuracy compared to more broadband models. A question was asked about how to include the effects of on-die decoupling. Sam stressed that this circuit must be added externally to the IBIS model.

TOUCHSTONE SYNTAX FOR VERSIONS 1.0 AND 2.0

Bob Ross, Teraspeed Consulting Group

Bob began by giving some background on the original Touchstone format. The version 2.0 document contains Touchstone “Version 1.0” format. Touchstone 2.0 advances include selectable reference resistance per port, explicit [Number of Ports] and [Number of Frequencies] keywords yielding more flexible data formats, symmetrical matrix format data reduction, and some reference normalization changes. He then detailed specific text formatting in the specification. He showed details of advances in Touchstone 2.0 including noise formats. He noted the IBIS-like keywords including [Version], [Number of Ports], [Number of Frequencies], [Reference], [Matrix Format] and [Number of Noise Frequencies]. He touched on data normalization changes from version 1.0 and IBIS and non-IBIS conventions. Bob thanked several people including Michael Mirmak and Radek Biernacki for their work on developing this specification.

Kim Helliwell asked about how to support mixed mode S-parameters. Michael Mirmak commented that it was not supported for two reasons. One is that Touchstone is meant to be used for passive devices, but there is a history of using S-parameters to characterize non-passive devices, and mixed model representations become very large. Also, single ended data is more easily converted to mixed mode, but not necessarily the other way around. Adge Hawes asked about port ordering and how to better specify port ordering without needing a decoder chart in each file. Bob commented that this is not addressed currently.

NEW INTERCONNECT MODELS REMOVE SIMULATION UNCERTAINTY

Chad Morgan, Tyco Electronics, Fangyi Rao, Vuk Borich, Sanjeev Gupta, Agilent Technologies

Chad Morgan began by talking about traditional passive component models. Modern models are more typically S-parameters. Disadvantages of S-parameters in time domain simulations

include conversion required to pole-residue macro-models or impulses and the difficulties this creates. He described simulation tools including traditional SPICE as well as custom and commercial ones. He noted that the paper focuses on impulse response usage in transient convolution. If one uses an impulse response, convolution is simple to accomplish. He described difficulties with converting S-parameters to an impulse response including iDFT leakage and windowing. He noted that it is easier to get frequency data from time data than the other way around. He proposed the need for a standard to share impulse response data.

Fangyi then began presenting on time domain convolution challenges. He detailed issues with causality and windowing including delay preservation and passivity. A rigorous approach for impulse response calculation should enforce causality with respect to time zero and delay and correct passivity violation in S-parameters while maintaining causality. He noted that S-parameters of a low impedance network are a tough case for convolution when normalized to 50 ohms. This requires a highly accurate impulse response. He showed results of a direct iDFT approach and a new approach for creating impulse responses. The new approach shows a better match to the original spectrum along with proper delay modeling. He detailed a vision of a way to exchange a multiport impulse response. He showed a proposed impulse response format and asked for comments.

A comment was made that the impulse response would always be inadequate for pole-zero analysis. Chad commented that this technique is very useful for simulation techniques such as algorithmic models. Length of response depends on resolution of the spectrum, and it will be up to the model creator to include enough data. Arpad Muranyi noted that it is difficult to get an ideal impulse response. C. Kumar noted that this helps different simulators produce the same results. Fangyi noted that the response must decay to zero to fix DC calculation. Chad summarized that the main interest here is to propose a format and not to debate the merits of different simulation techniques. He asked the IBIS committee to debate the format if they are interested in standardizing it.

MULTI-MODE MODELING

Bob Ross, Teraspeed Consulting

Bob explained that IBIS offers the ability to configure buffers in multiple ways. Current methods include [Model Selector], [Alternate Package Model]s, [Series Switch Group]s and [Add Submodel]. The tool or user selects options based on all the choices documented. Examples of missing configurability are differential versus single ended reconfiguration and 3-state versus I/O distinctions. He showed an example of an output clock with many configurations including various voltages and slew rates. He created four [Component] choices as well as [Model Selector] choices for individual [Pin]s. He also created four distinct [Diff Pin] assignments. He noted that in a differential model, Vdiff could be different for PECL and LVDS options. An IBIS limitation is no selection mechanism for re-configuration of single ended (matched pairs) to differential. The issue is that you must use different [Component]s for hard coded choices. He observed that configurability makes a strong case for moving differential parameters into the [Model] scope directly along with single-ended parameters.

Michael Mirmak noted that some issues are physical connection of multiple drivers to single nodes and selection of single ended versus differential modes under both input and output conditions. Arpad Muranyi noted that he did not think there was physical connection of more than one driver at a time as shown in the example. Anders Ekholm added that there could be cases of this occurring.

BUILDING ADVANCED TRANSMISSION LINE AND VIA-HOLE MODELS FOR SERIAL CHANNELS WITH 10 GBPS AND HIGHER DATA RATES

Yuriy Shlepnev, Simberian

Yuriy began by noting the need to use electromagnetic models for multi-gigabit data channels. He described major signal degradation factors in transmission lines and vias. He described an approach of breaking up a channel into multiple segments of W-element models for transmission lines and S-parameter models for vias. Both early system exploration and system verification can be done on the basis of decomposition into elements with localizable electromagnetic models. Also, hybrid simulation technology is used in his analysis. Summarizing conductor attenuation and dispersion effects, he showed the current distribution in a rectangular conductor at various frequencies. The frequencies for various technologies where skin effect is well-developed were shown. He also showed this information for metal roughness and how to model roughness with the effective surface impedance. An example of the transition to skin effect and roughness in a package strip-line was shown. This was followed by showing the effect of RoHS metal surface finish on PCB micro-strip line parameters. He showed several versions of broadband causal dielectric models with dispersion followed by the effect of dielectric models on PCB micro-strip line parameters. A table summarized the extracted transmission line parameters from various 2D and 3D solvers.

Yuriy switched topics to discuss modeling of differential via holes. He began by defining the differential mode in vias, noting that any 3D full-wave solver can be used to generate a model for localizable via holes. De-embedding and reference plane shift were discussed as well as the design of impedance controlled differential via-holes. He concluded that with via holes, one must distinguish between localizable and non-localizable cases and analyze each case properly.

ADVANCES IN 7.5GB/S SERDES MODELING USING IBIS 4.2 (VHDL-AMS AND VERILOG-AMS)

Luis Boluna, Ehsan Kabir, Susmita Mutsuddy, Kelvin Qiu, Daniel Ho, Cisco Systems, Inc.
Dr. Sang Baeg, Hanyang University

Luis began by noting that this project is a continuation of their presentation given at DesignCon 2006. He showed a demonstration of a full SerDes channel simulation using detailed vendor models. Case 1 was a 7.5Gbps channel through a backplane. Case 2 showed a 7.5Gbps chip to chip analysis. He showed correlation to SPICE models for a specific vendor as well as correlation to the vendor's internal MATLAB* tool. Luis then demonstrated a case showing Verilog-AMS to VHDL-AMS interoperability. He then showed results of a crosstalk simulation followed by a slide of model interoperability across several EDA tools. He observed that the results were not identical between the tools examined. He then showed the use of AMS for post processing of BER where MATLAB* post processing functions were ported into AMS. He shared learning experiences from using MATLAB*. Next steps in the project will be to use IP encryption, work with vendors for better multi-lingual support, develop AMS utilities, work with ASIC vendors for next generation AMS models and simulate higher data-rate SerDes devices. Adge Hawes asked what the issue with compiled models was. Luis replied that encryption would make the models easier to use, because compiling can tie the models to a specific tool as well as a specific operating system. Todd Westerhoff asked for clarification of how different models perform better than others. Luis said that the post processing part of the models was improved. Also, some vendors simulate much more quickly than others, but this is still under investigation.

IBIS-AMI WITH DIFFERENT LANGUAGES

Arpad Muranyi, Mentor Graphics

Arpad began with a summary of the IBIS-AMI specification status. He noted that BIRD 104.1 is expected to be part of the IBIS 5.0 specification. He noted that ANSI C is the function interface for AMI, but then expressed concern that system/circuit/RF designers are not necessarily good programmers. He reviewed a Tx model code example supplied with the public test kits, and he cited his own difficulty in understanding large sections of it. Todd Westerhoff asked whether many of the initial code excerpts Arpad identified as difficult to understand are not in fact type declarations. Todd also observed that VHDL-AMS is a strongly-typed language, meaning that all high-level languages require some overhead from the writer for type matching. Arpad responded by noting that pointers-to-pointers may still be difficult to understand and do not appear in the HDL-based languages. Walter Katz noted that MATLAB* allows direct export to C, per an earlier DesignCon presentation, which may resolve some of the typing and C-specific code issues.

Arpad noted that there are other language candidates for writing AMI models including VHDL-AMS, Verilog-AMS and MATLAB*. Arpad then summarized his implementation of the entire Tx demonstration code set in VHDL-AMS. He noted that no memory allocation is needed for VHDL-AMS, therefore hiding architecture and computer science issues from the model maker. He said that returning more than one vector was troublesome in VHDL-AMS if you don't start with a multi-dimensional vector. Todd Westerhoff commented that the cost of interoperability is some memory allocation overhead. AMI memory utilization is completely linear with runtime in the demonstration code, which may not be true for *-AMS implementations. Arpad showed that the waveforms were matched for different tap settings and pattern lengths. A MATLAB* version was also shown, with the same results. Adge Hawes commented on the convolution functions written in the code versus what was built into MATLAB*. C. Kumar commented that the M language is un-typed, making it popular among engineers.

In terms of execution times, MATLAB and C are comparable, with the VHDL-AMS code being much slower. The VHDL-AMS compiler didn't seem to help that code to run faster. Arpad concluded that ANSI C is the most inconvenient language, but is fast; VHDL AMS is somewhat better; MATLAB* is fast, friendly and efficient. Ian Dodd commented that memory managers handle malloc, alloc issues in C, meaning that few programmers need to deal directly with writing those functions. Todd Westerhoff added that the MATLAB* and VHDL-AMS code shown by Arpad is not IBIS-AMI-compliant, because model makers would still need to do the memory allocation to work with AMI tools. Mike Steinberger asked whether the free Perl vectorized language could be used to implement the same functions, without typing or direct memory allocation.

One participant inquired, regarding the Cisco presentation, why the two AMS simulators give such radically different responses. This question was deferred until the end of the meeting.

SERDES MODELING: DEMONSTRATING IBIS-AMI MODEL INTEROPERABILITY

Todd Westerhoff, Signal Integrity Software (SiSoft)

Todd showed both released toolkits from a structural viewpoint. The test case control file includes channel impulse response without equalization, plus model settings. The stimulus generator feeds data into the test simulator executable supplied with the kit. Impulse and waveform responses are provided into the receiver pads. Some coding is required for memory

optimization, and slight differences exist between the available toolkits. The second version of the toolkit shows slower performance due to disk writes transforming the waveform into a time and voltage format (this also doubled the file size). Benchmarks used 500k bits. "Astronormous" file sizes result as run time continues. File I/O is the performance limitation. Todd noted that, between AMS and AMI, AMS is the language while AMI is the interface between the model and the environment. When a program is bought, Todd added, he only cares if it runs, not how it is written. Additional examples were shown with post-processing. Luis Boluna noted that, like the BER plot shown in Todd's slides, MATLAB* has color mapping in its displays. Vuk Borich noted that the BER plots shown do not directly relate to AMI. Todd agreed that the illustration of BER was a tool-specific feature, but the model set can generate enough data that visualization differences are needed. Additionally, the plots illustrate the impact of time-varying behavior in the DFE circuit at the receiver as the adaptive algorithm finds the optimum result. Syed Huq suggested that "AMI model" was a less descriptive name than "AMI-compliant model." Todd agreed.

EXPERIENCES IN DEVELOPING AND CORRELATING EIGHT INTEROPERABLE ALGORITHMIC MODELS

Adge Hawes, IBM; Ken Willis, Cadence Design Systems

(Presented by Adge Hawes, IBM and C. Kumar, Cadence Design Systems)

Adge Hawes described the IBM internal tool, HSSCDR. This SerDes analysis suite is provided directly to customers and used internally to represent IBM hardware. The program is written in an internally-developed MATLAB-like C-based language, which is half-compiled, half-interpreted.

Adge showed IBIS-AMI-compliant model runtime comparisons against HSSCDR and *-AMS runs. He added that IBIS-AMI enabled distribution of IBM models without their partner external tool vendors having seen a single line of IBM code. He noted that free SerDes post-processing tools are widely available, but these are not as fast, compatible or capable as IBIS-AMI using their own code. Adge suggested a variety of development environments for code, including MATLAB and free variants Octave and Euler. Luis Boluna also suggested SCIlab. C compilers available include Free Visual C++ Express for Windows. Adge advised developers to beware the GPL viral effect, which can cause internal code to be legally forced into redistribution. He noted that some memory management is needed to ensure proper buffering and lining up of waveforms with clock edges. Luis asked whether jitter transients are relevant: could data, which may be jittered, be taken from an oscilloscope and used with these IBIS-AMI models? Adge responded that it could. Adge continued by noting some common mistakes made in ANSI C coding as well as differences between Windows* and Linux operating systems. He showed code examples on data structures and the AMI_Init and AMI_Close functions and example waveforms from an AMI model execution.

C. Kumar then presented on algorithmic model correlation. He showed the process of correlating simulation results between a proprietary tool using the "source" algorithmic model and a commercial tool using the IBIS-AMI model, with identical inputs. The basic strategy is to start simple (lossless channel with terminations, no filtering, pulse stimulus) and then add other variables (complex passive channel, bit stream, filtering, jitter injection). He detailed this correlation approach for a Tx circuit. Common pitfalls include Tx/Rx circuit model assumptions, magnitude scaling of impulse responses, S-parameters as relate to time domain simulations, stabilization time such as needed for clock recovery algorithms, consistent measurements between tools and supporting multiple platforms which may cause small numerical differences.

OPEN DISCUSSION AND CONCLUDING ITEMS

A participant inquired about results shown in the Cisco presentation illustrating variations in simulator output for the same model sets and expressed surprise that this could happen on a standard interface. Michael Mirmak pointed out that test load and data keywords in IBIS exist to assist model users in verifying simulator outputs against expected results supplied by the model maker. Mike Steinberger added that the AMI extensions to IBIS also help ensure that model processing is consistent between tools, as the algorithms are inside the model. Arpad Muranyi noted that the channel has an enormous impact on the system outputs, particularly in the examples shown by Cisco, and these are beyond the control of the IC model maker.

The participant responded that he was expecting a standard such as IBIS to define expected results. Michael noted that the IBIS standard defines a data exchange format for inputs, not necessarily outputs or even the interpretation of the data. He added that defining the interpretation in the specification would set limits on vendor flexibility that risk making the specification less acceptable to the industry marketplace. Todd Westerhoff observed that three existing "flavors" of IBIS currently exist: traditional table-based IBIS, multi-lingual IBIS as defined in IBIS 4.1 and 4.2 and IBIS-AMI. Each of these enables different levels of control over both data and data interpretation in simulation.

No other questions were raised.

Michael Mirmak closed the meeting by thanking the participants, presenters and co-sponsors and reminding those present of the dates for the next Summit and teleconference meetings. The meeting was adjourned at approximately 4:50 PM.

NEXT MEETING

The next IBIS Open Forum teleconference will be held February 22, 2008 from 8:00 AM to 10:00 AM US Pacific Time. The next IBIS Summit will take place at DATE on March 14, 2008. No teleconference has been arranged for the meeting.

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NOTES

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This meeting was conducted in accordance with the GEIA Legal Guides and GEIA Manual of Organization and Procedure.

The following e-mail addresses are used:

majordomo@eda-stds.org
In the body, for the IBIS Open Forum Reflector:
subscribe ibis <your e-mail address>

In the body, for the IBIS Users' Group Reflector:
subscribe ibis-users <your e-mail address>

Help and other commands:
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To join, change, or drop from either or both:
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IBIS Users' Group Reflector (ibis-users@eda-stds.org)
State your request.

ibis-info@eda-stds.org

To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the EIA-IBIS Open Forum as a full Member.

ibis@eda-stds.org

To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

ibis-users@eda-stds.org

To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda-stds.org

To report ibischk parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda-stds.org/ibis/bugs/ibischk/
http://www.eda-stds.org/ibis/bugs/ibischk/bugform.txt

icm-bug@eda-stds.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda-stds.org/ibis/icm_bugs/
http://www.eda-stds.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda-stds.org/ibis/bugs/s2ibis/bugs2i.txt
http://www.eda-stds.org/ibis/bugs/s2ibis2/bugs2i2.txt
http://www.eda-stds.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eigroup.org/ibis/ibis.htm

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda-stds.org/ibis/directory.html

All eda.org documents can be accessed using a mirror:

http://www.ibis-information.org

Note that the "/ibis" text should be removed from directory names when this URL mirror is used.

GEIA STANDARDS BALLOT VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

Organization	Interest Category	Standards Ballot Voting Status	December 21, 2007	January 11, 2008	February 1, 2008	February 7, 2008
Advanced Micro Devices	Producer	Inactive	√		√	
Agilent Technologies	User	Inactive				√
Ansoft	User	Inactive				√
Apple Computer	User	Inactive				
Applied Simulation Technology	User	Inactive				
ARM	Producer	Inactive				
Cadence Design Systems	User	Active		√	√	√
Cisco Systems	User	Active	√	√	√	√
Ericsson	Producer	Active	√	√	√	√
Freescale	Producer	Inactive				√
Green Streak Programs	General Interest	Inactive				
Hitachi ULSI Systems	Producer	Inactive				√
Huawei Technologies	User	Active	√		√	√
IBM	Producer	Active		√	√	√
Intel Corp.	Producer	Active	√	√	√	√
IO Methodology	User	Active	√	√	√	√
LSI	Producer	Active	√	√	√	√
Mentor Graphics	User	Active	√	√	√	√
Micron Technology	Producer	Active	√	√		√
Nokia Siemens Networks	Producer	Inactive	√			
Panasonic	Producer	Inactive				
Samtec	Producer	Inactive				√
Signal Integrity Software	User	Active	√	√	√	√
Sigrity	User	Inactive				√
STMicroelectronics	Producer	Inactive				
Synopsys	User	Inactive				√
Teraspeed Consulting	General Interest	Active	√	√	√	√
Texas Instruments	Producer	Inactive				√
Toshiba	Producer	Inactive				
Xilinx	Producer	Active			√	√
ZTE	User	Inactive				
Zuken GmbH	User	Inactive				

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

INTEREST CATEGORIES ASSOCIATED WITH GEIA BALLOT VOTING ARE:

- USERS - MEMBERS THAT UTILIZE ELECTRONIC EQUIPMENT TO PROVIDE SERVICES TO AN END USER.
- PRODUCERS - MEMBERS THAT SUPPLY ELECTRONIC EQUIPMENT.
- GENERAL INTEREST - MEMBERS ARE NEITHER PRODUCERS NOR USERS. THIS CATEGORY INCLUDES, BUT IS NOT LIMITED TO, GOVERNMENT, REGULATORY AGENCIES (STATE AND FEDERAL), RESEARCHERS, OTHER ORGANIZATIONS AND ASSOCIATIONS, AND/OR CONSUMERS.