Advances in 7.5Gb/s SerDes Modeling using IBISv4.2 (VHDL-AMS and Verilog-AMS)

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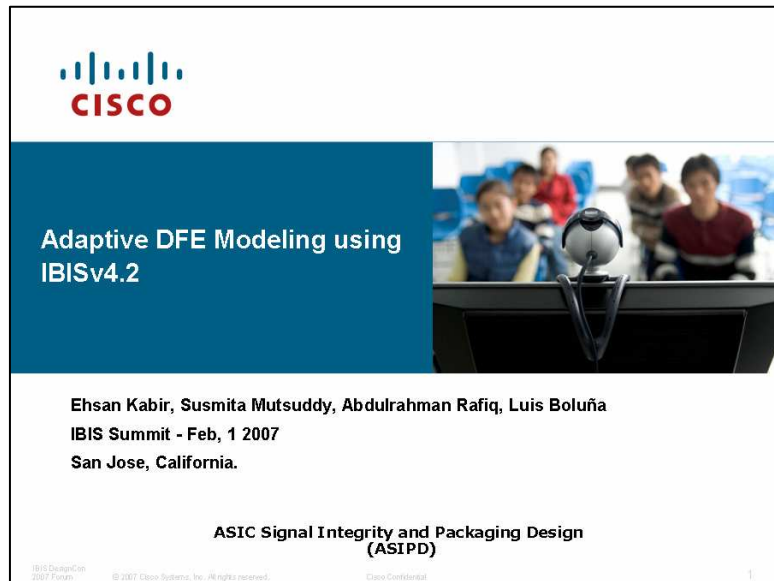
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[*] - *with Hanyang University, South Korea*

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    ASIC Signal Integrity and Packaging Design (ASIPD)

Where we left off: DesignCon 2006 paper

- Demonstrated a detailed DFE design in *AMS is feasible.

- Explained the challenge of interoperability and the promise of *AMS modeling to solve that and much more.

- The paper served as a catalyst to an ongoing effort in SerDes modeling across the industry.

The intent of this paper is to provide the remainder of the industry with an update on what has been accomplished and the status on ongoing efforts.
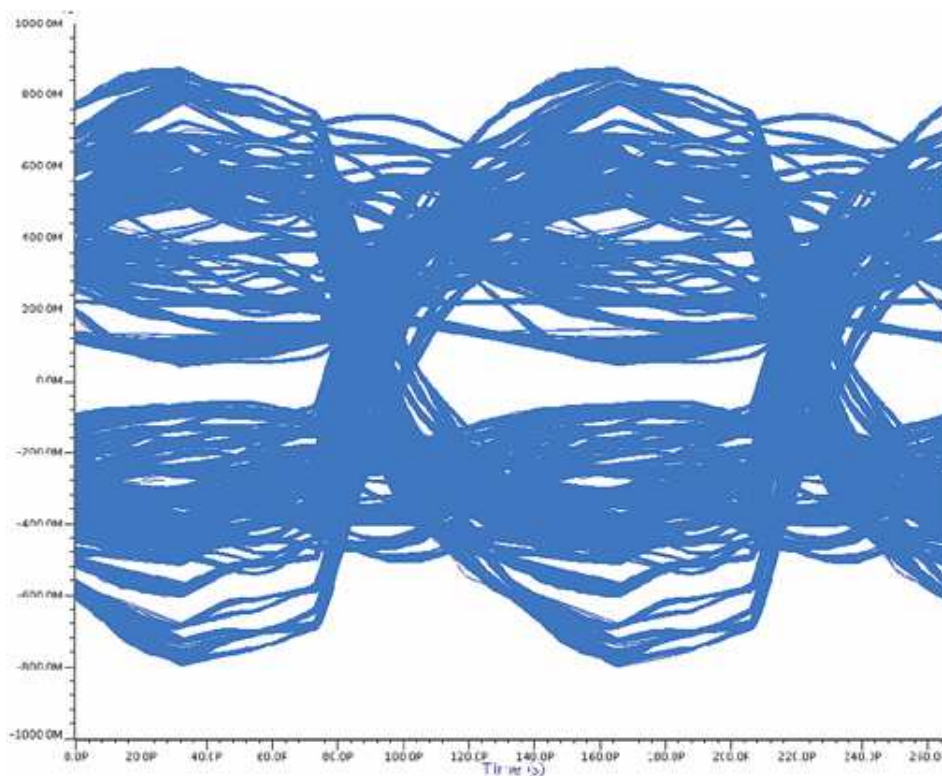
Agenda

- Demonstration of full SerDes channel simulation using detailed vendor models across 5 major ASIC vendors.

- Correlation of vendor models
    - To HSPICE
    - To Vendor Internal Matlab tool
    - To Silicon

- Demonstration of vendor model interoperability in a full SerDes Channel simulation(s).

- Demonstration of VHDL-AMS to Verilog-AMS interoperability in a SerDes full channel simulation.

- Model interoperability across several EDA tools

- Demonstration of post processing modules (to extrapolate BER) in fully coded AMS

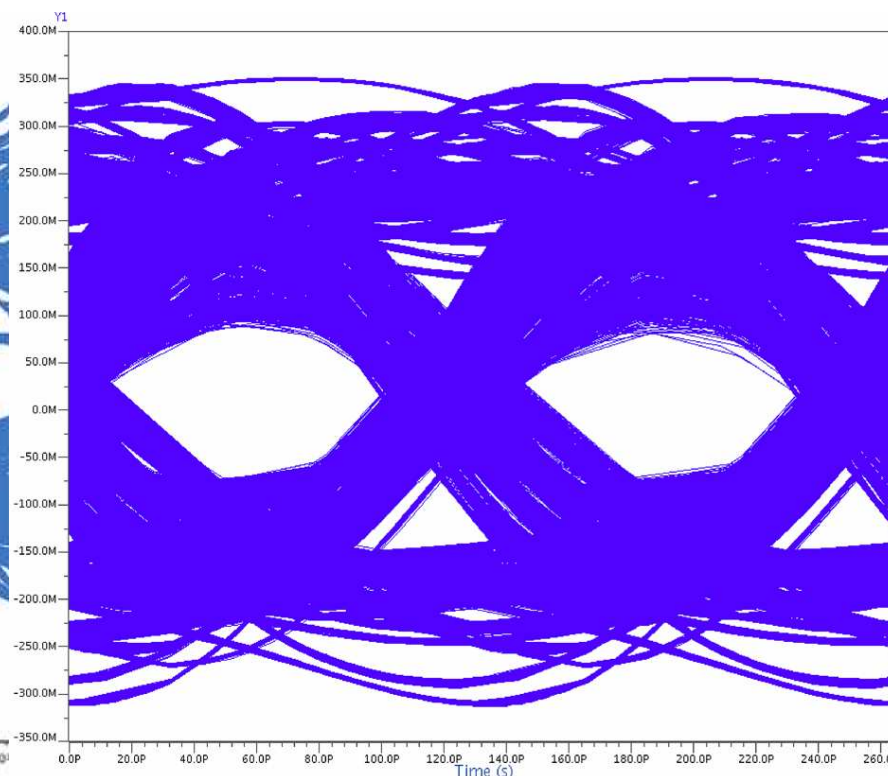**ASIC Signal Integrity and Packaging Design (ASIPD)**

Agenda

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Example of Vendor Models:
Full TX and RX EQ solution

- Analyzed channel for optimum pre-emphasis settings; -10% pre-cursor tap weight, -20% first post-cursor tap weight.
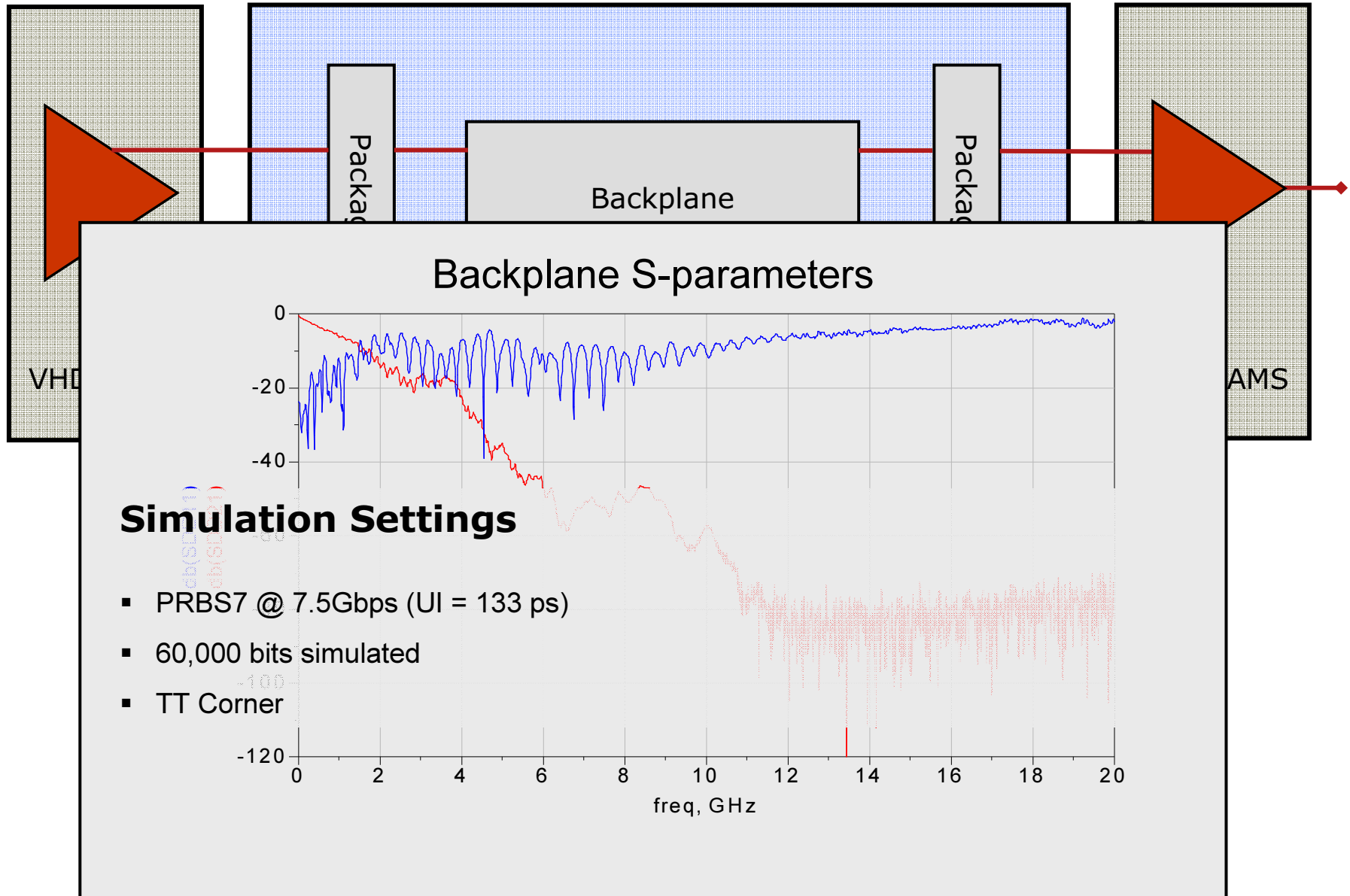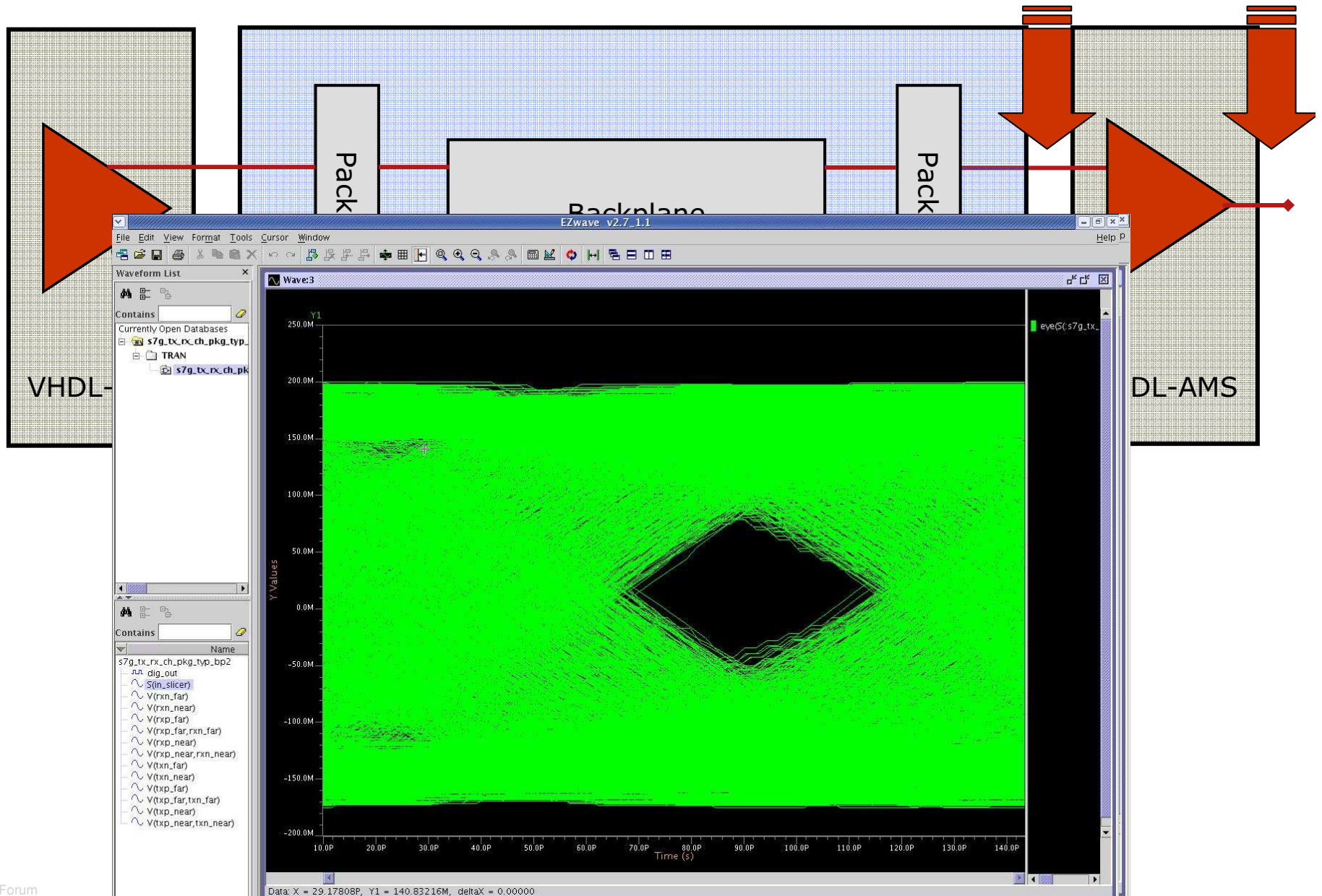

Differential signal at TX
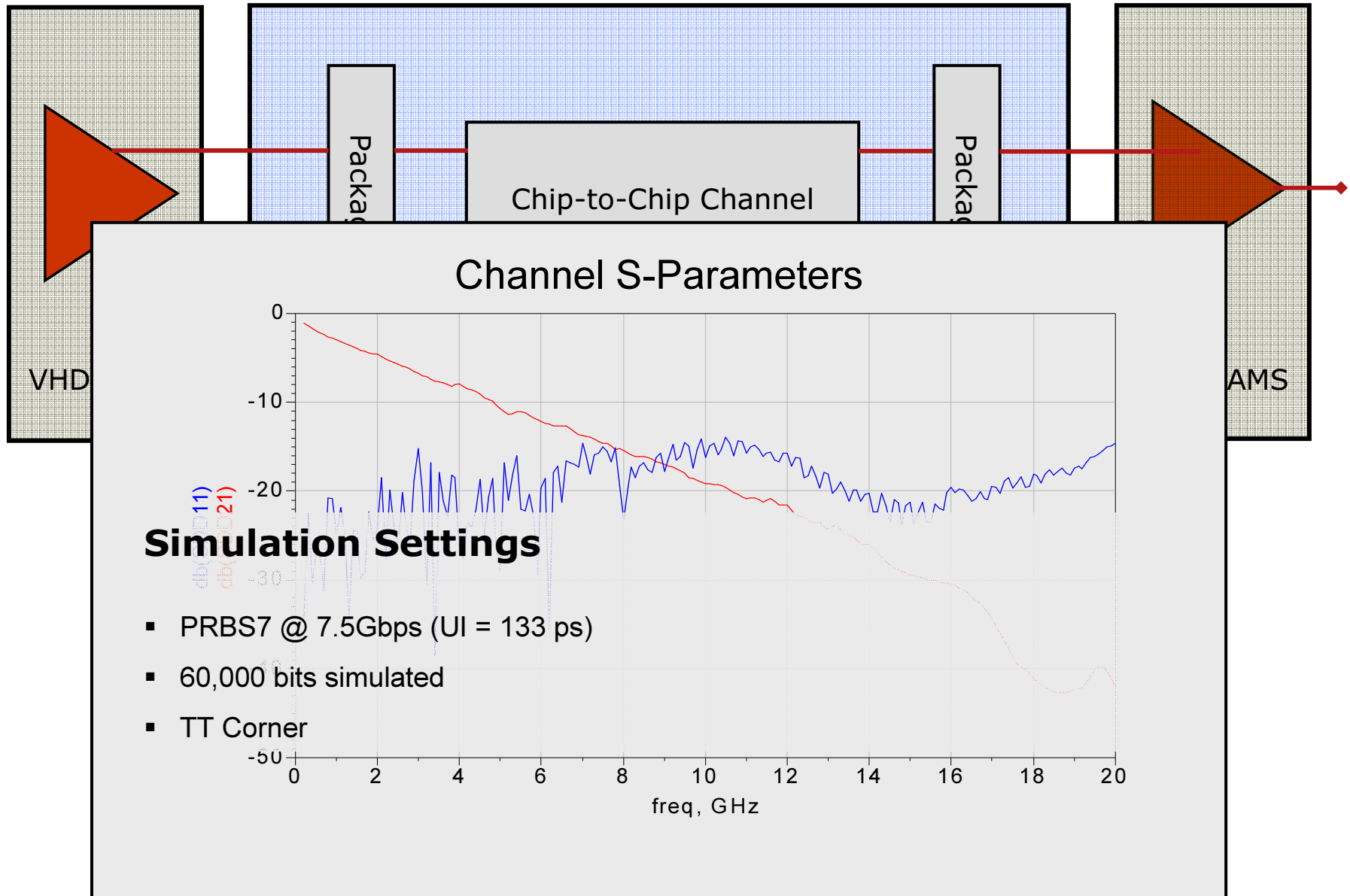
Differential signal at RX

ASIC Signal Integrity and Packaging Design (ASIPD)

Case 1 – 7.5Gbps through Backplane

Package

Backplane

Package

VHD

AMS

Backplane S-parameters

Simulation Settings

- PRBS7 @ 7.5Gbps (UI = 133 ps)
- 60,000 bits simulated
- TT Corner

freq, GHz

ASIC Signal Integrity and Packaging Design (ASIPD)

Case 1 – 7.5Gbps through Backplane

Case 2 – 7.5Gbps Chip-to-Chip

Package

Chip-to-Chip Channel

Package

VHD

AMS

Channel S-Parameters

(11)
(21)

0

-10

-20

-30

-50

0   2   4   6   8   10   12   14   16   18   20

freq, GHz

Simulation Settings

- PRBS7 @ 7.5Gbps (UI = 133 ps)

- 60,000 bits simulated

- TT Corner

ASIC Signal Integrity and Packaging Design (ASIPD)

Case 2 – 7.5Gbps Chip-to-Chip

Agenda

- Demonstration of full SerDes channel simulation using detailed vendor models.

- **Correlation of vendor models**
  - **To SPICE**
  - **To Vendor Internal Matlab tool**
  - **To Silicon**

- Demonstration of VHDL-AMS to Verilog-AMS interoperability in a SerDes full channel simulation.

- Model interoperability across several EDA tools

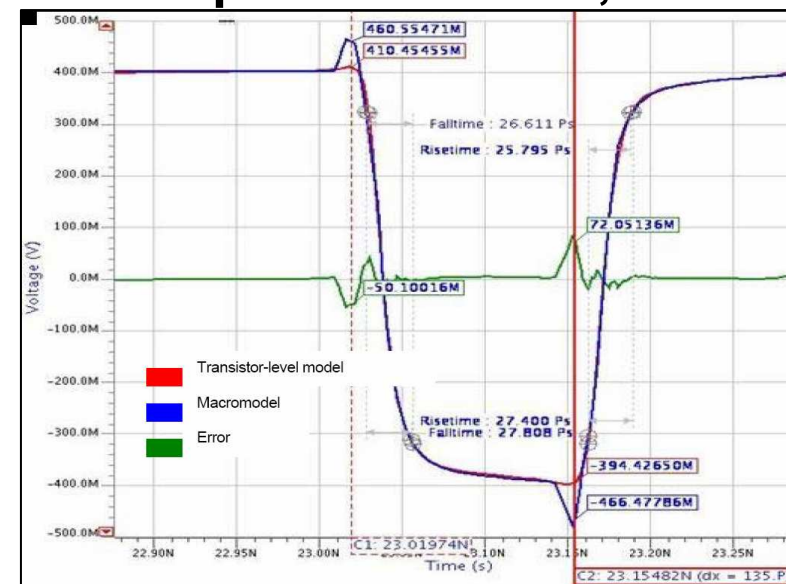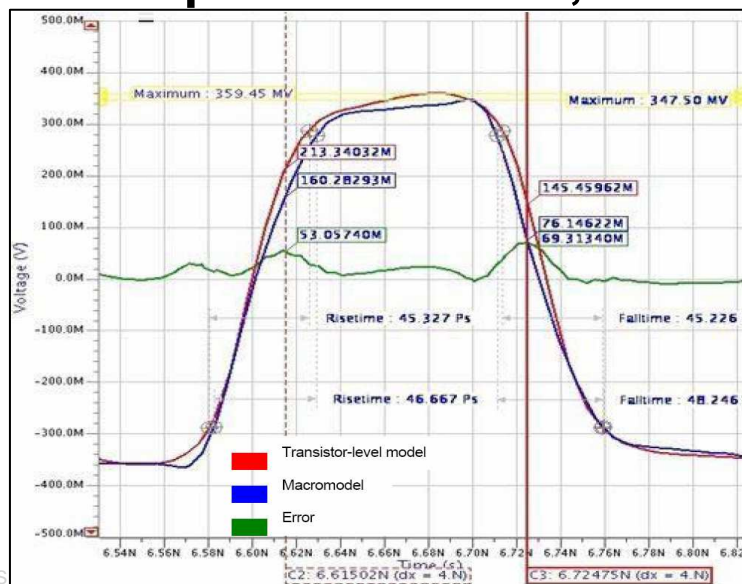- Demonstration of post processing modules (to extrapolate BER) in fully coded AMS

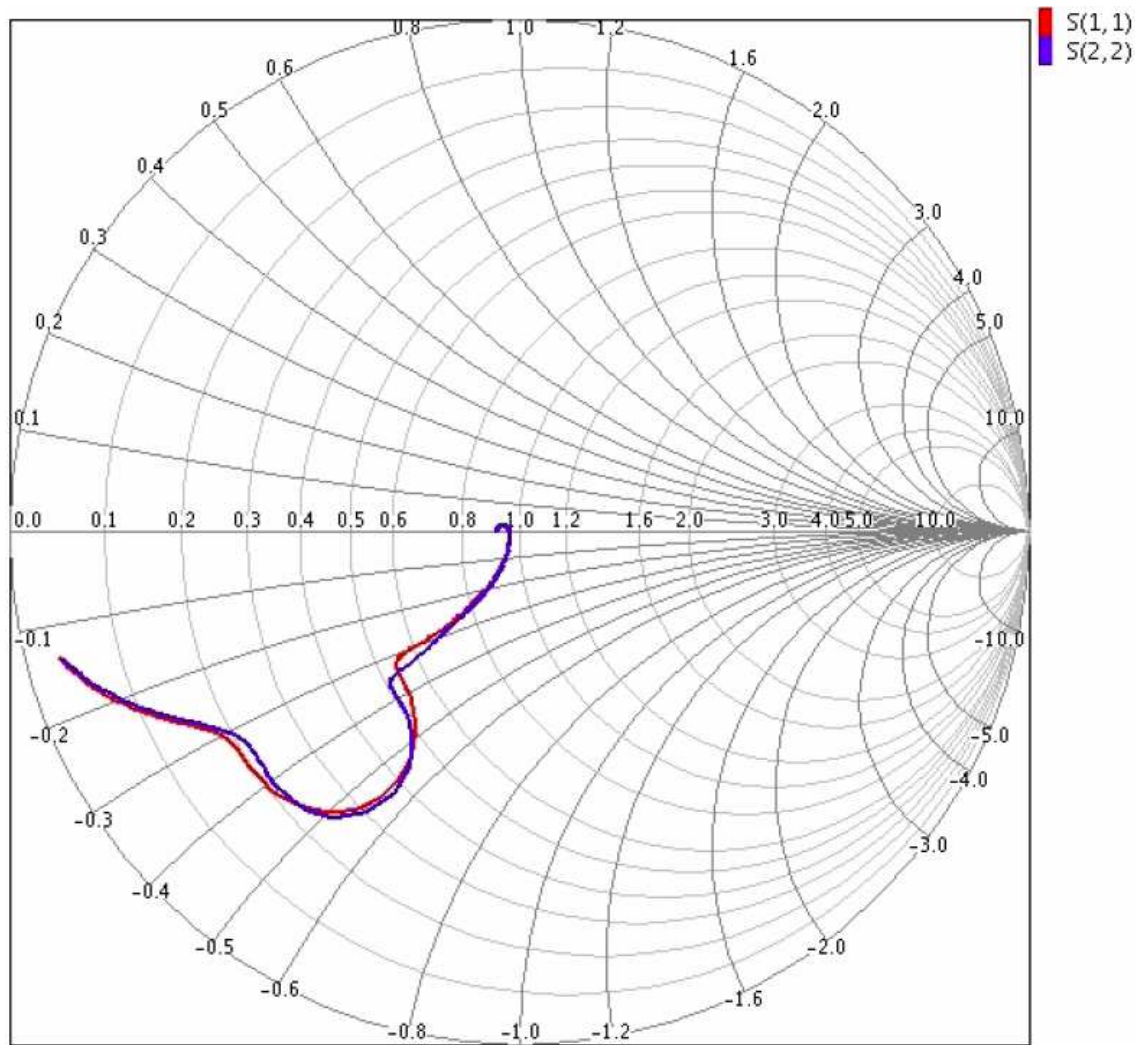# Vendor A TX AMS to SPICE Correlation: FAST/SLOW Process Corners
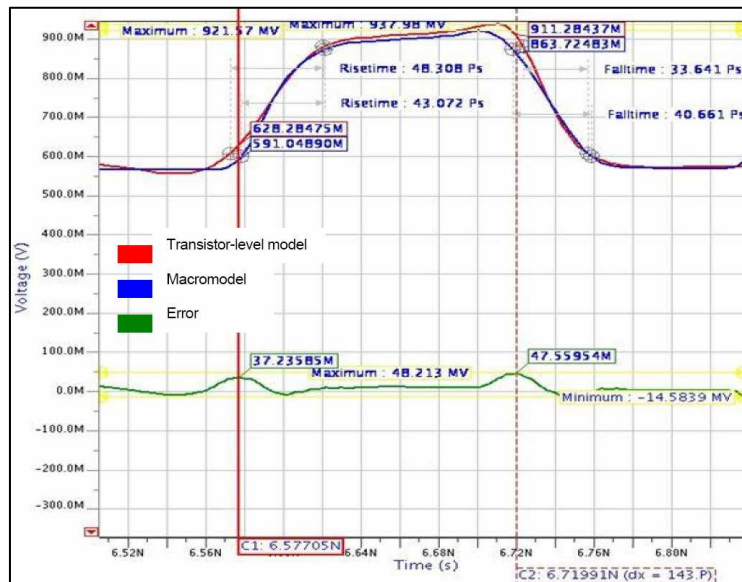
Slow process corner, 125C
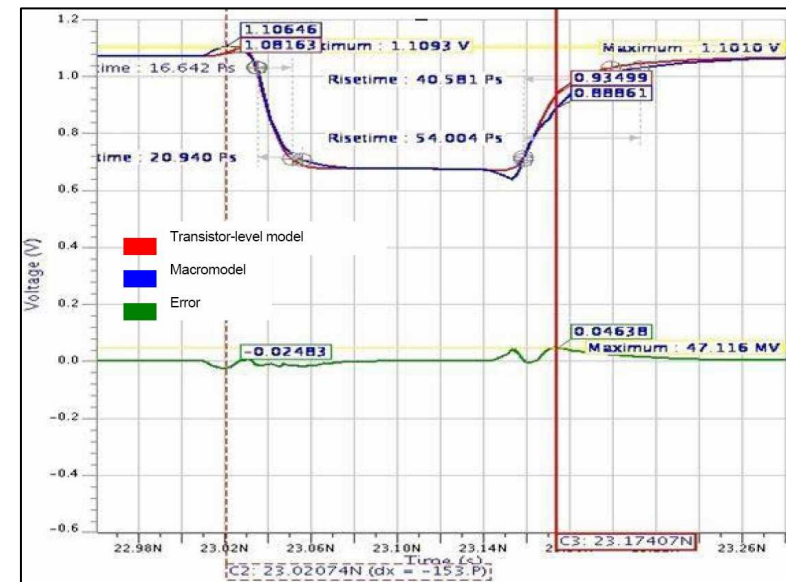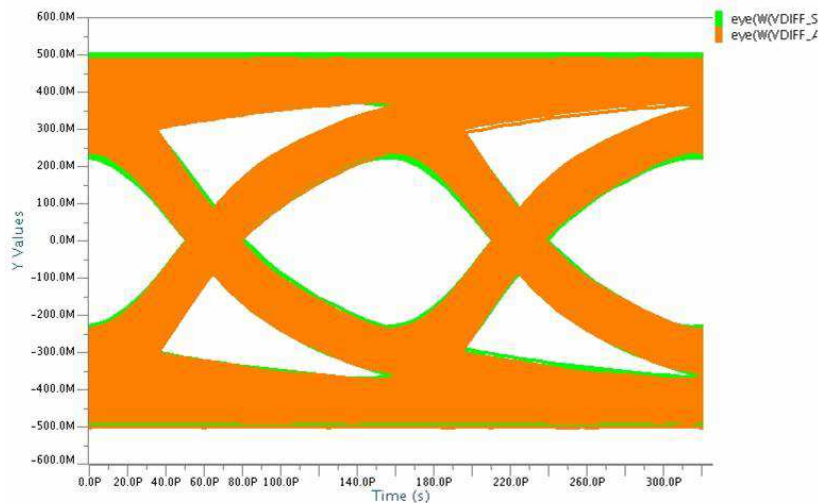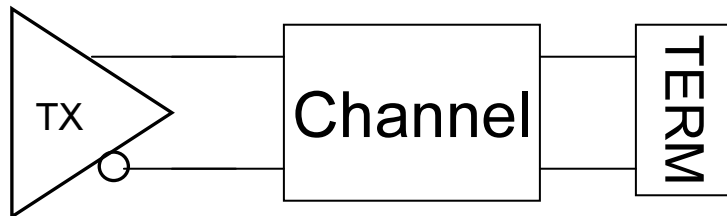

Fast process corner, 125C

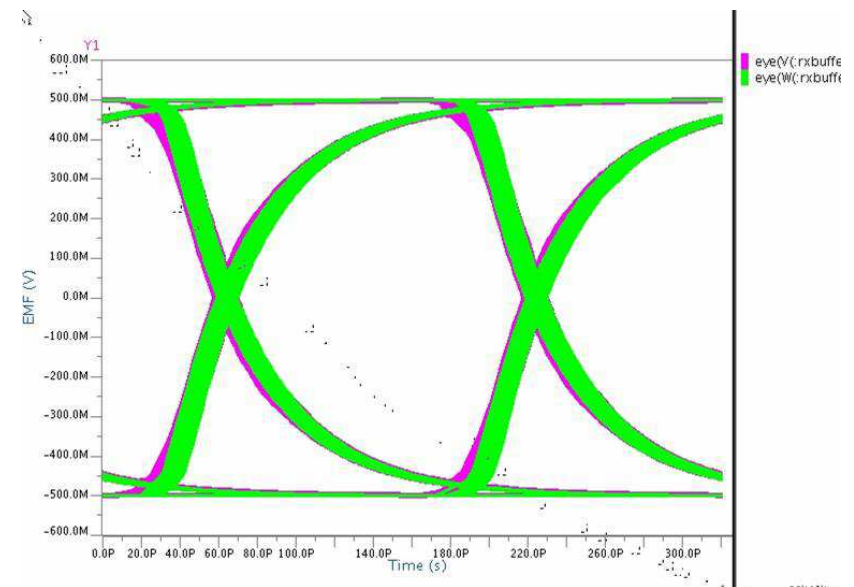# Vendor A RX AMS to SPICE Correlation

- AMS RX input impedance match perfectly with SPICE output.

- RED = S11(SPICE)

- BLUE = S11(AMS)

Vendor B VHDL-AMS to Spice Correlation

Differential eye diagram after

19 inch channel

Orange (AMS)/Green (SPICE)

Equalized Channel after

19 inch channel (After DFE)

Magenta (AMS)/Green (SPICE)

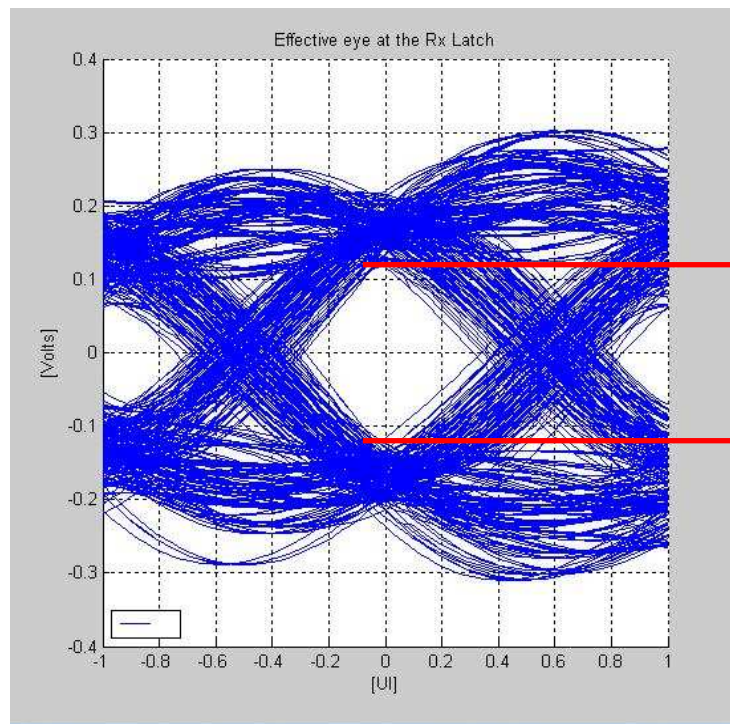# Vendor Verilog-AMS Model correlation to Vendor Internal Matlab tool

- Simulation setup: 8.5 Gb/s with PRBS7 pattern

    Cisco backplane channel

    Nominal corner
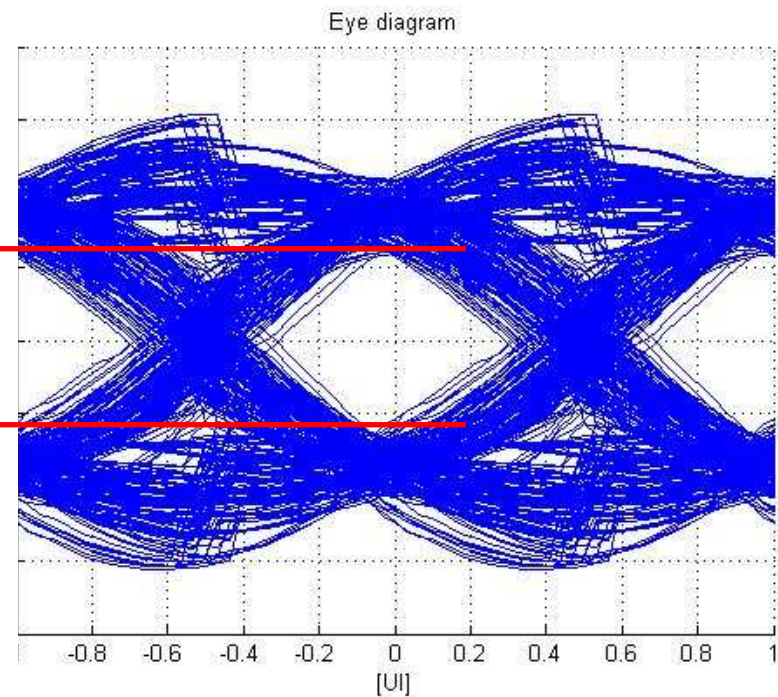
    200k Bits simulated with 200 ppm freq offset

Vendor Verilog-AMS Model correlation to Vendor Internal Matlab tool : Results
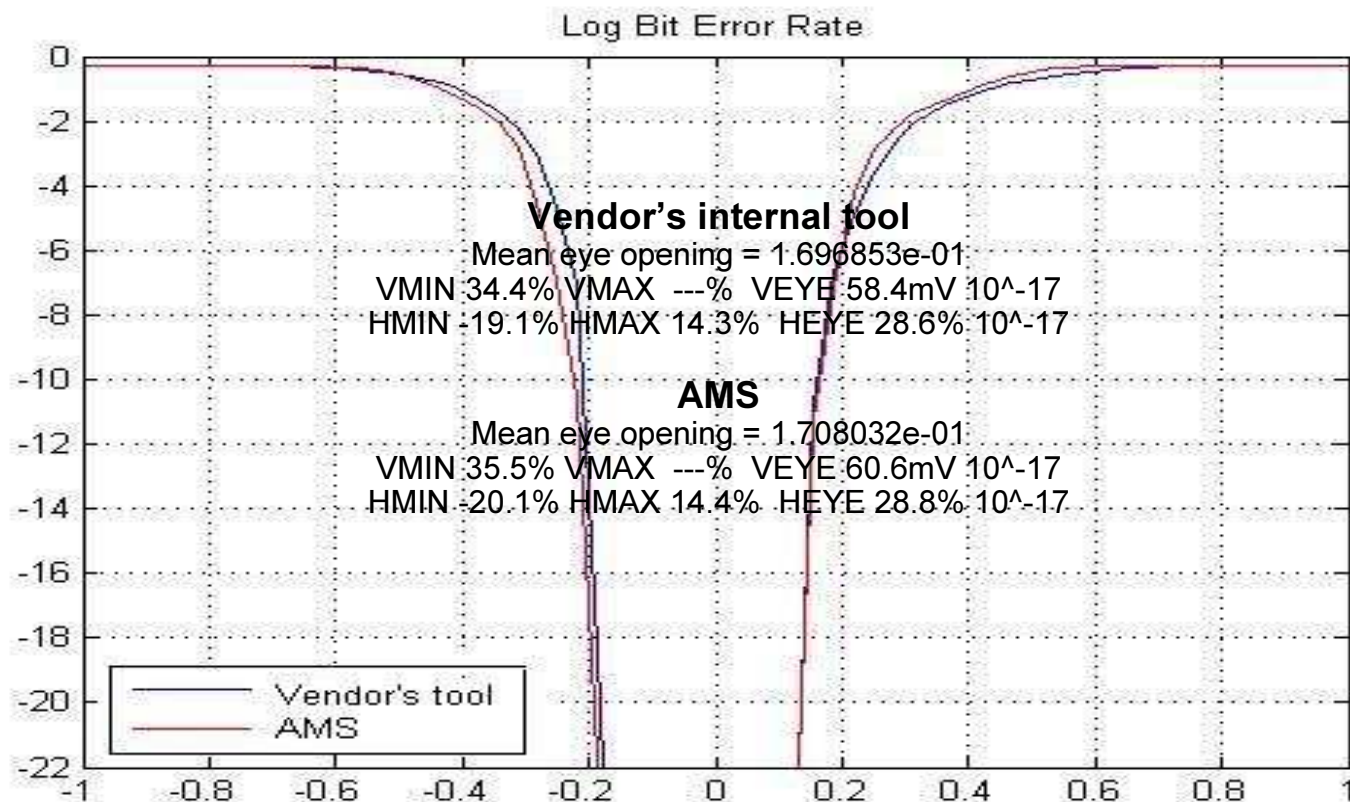
- Eye diagrams after the DFE

Eye diagram from Vendor's internal tool

Eye diagram from AMS simulation

ASIC Signal Integrity and Packaging Design (ASIPD)   16

Vendor Verilog-AMS Model correlation to Vendor Internal Matlab tool: Results

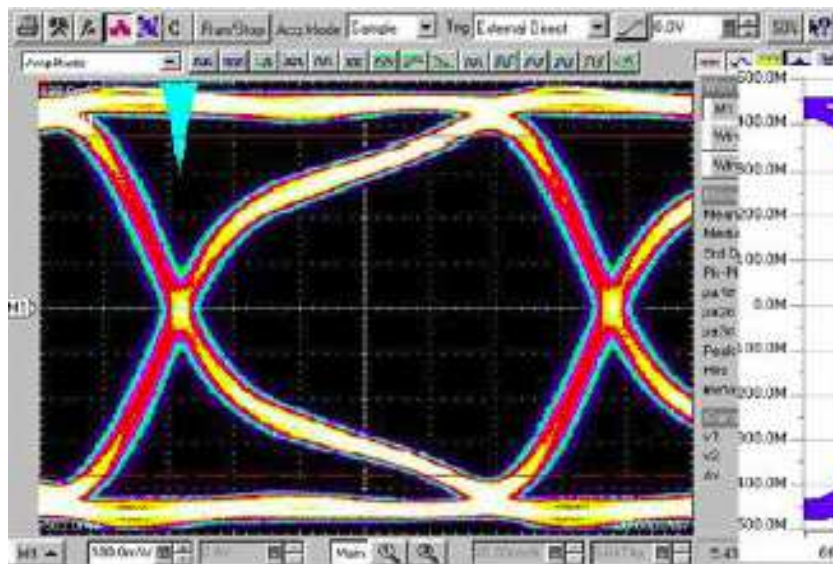
0.2 % difference HEYE at 10^-17

2.2 % difference VEYE at 10^-17
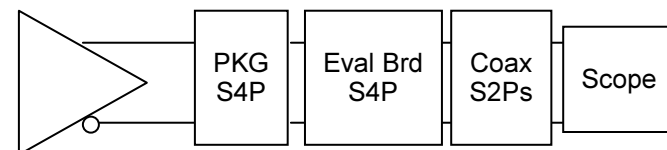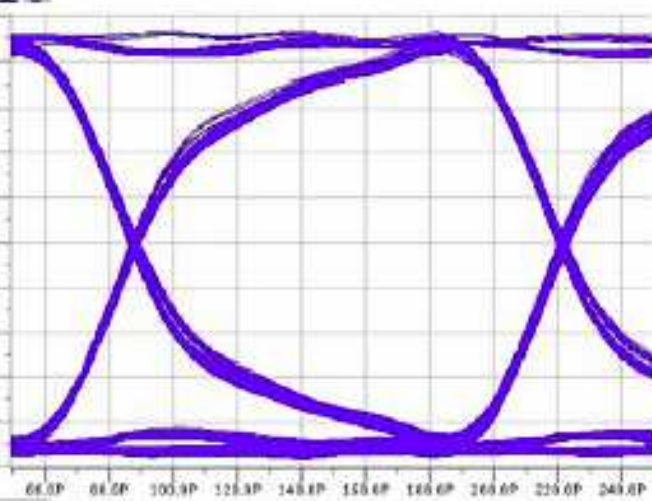
Vendor VHDL-AMS TX to Silicon Correlation

- PRBS31 data pattern from TX at7.5Gb/s

Lab Measurement   **AMS Output**

Sim Setup

Agenda

- Demonstration of two full SerDes channel simulations using detailed vendor models.

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  To HSPICE

  To Vendor Internal Matlab tool

  To Silicon

- **Demonstration of VHDL-AMS to Verilog-AMS interoperability in a SerDes full channel simulation.**

- Model interoperability across several EDA tools

- Demonstration of post processing modules (to extrapolate BER) in fully coded AMS
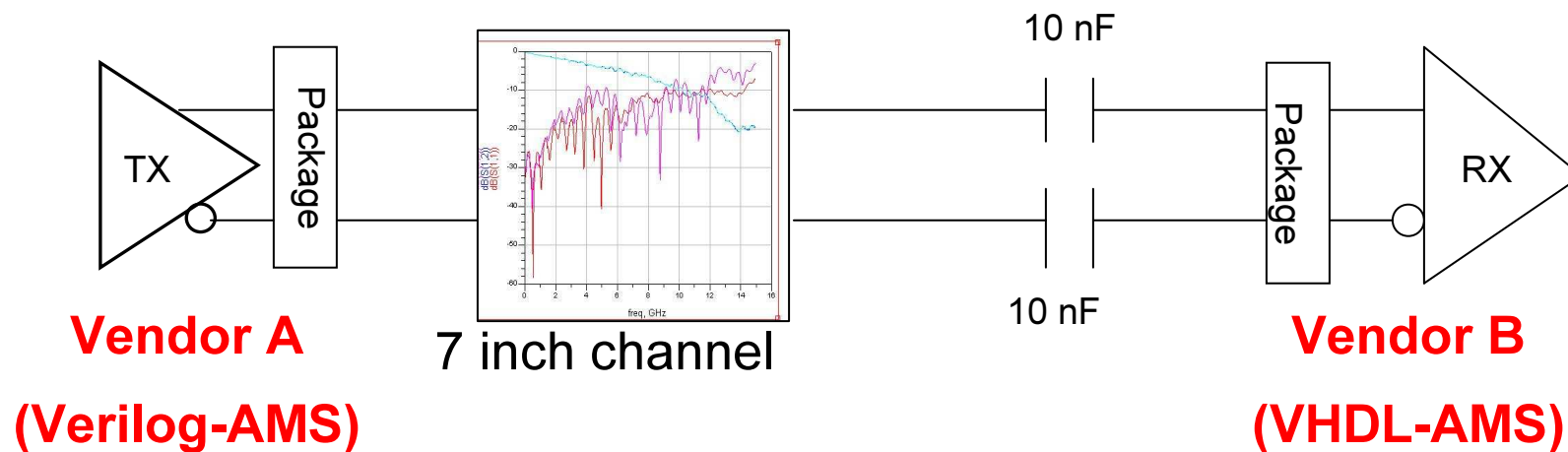
Verilog-AMS to VHDL-AMS interoperability

- Test conditions:
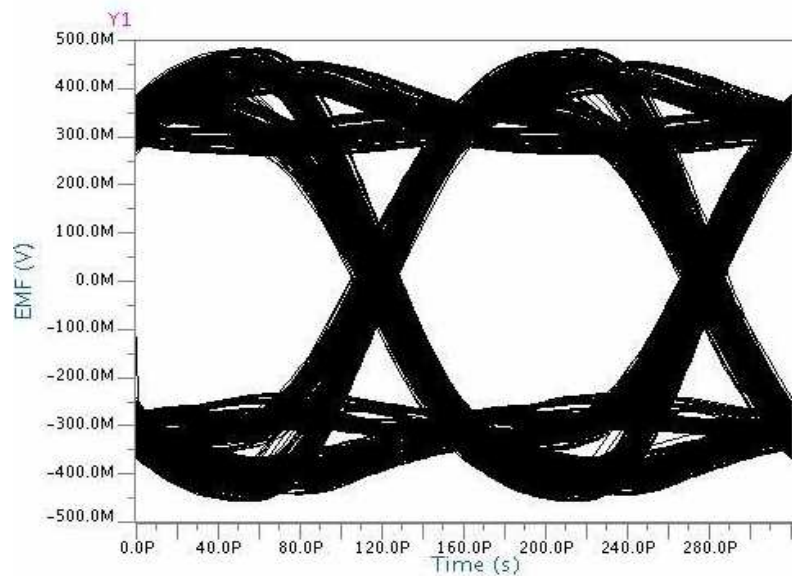 - Data Pattern: PRBS 7 running @ 6.25 Gb/s
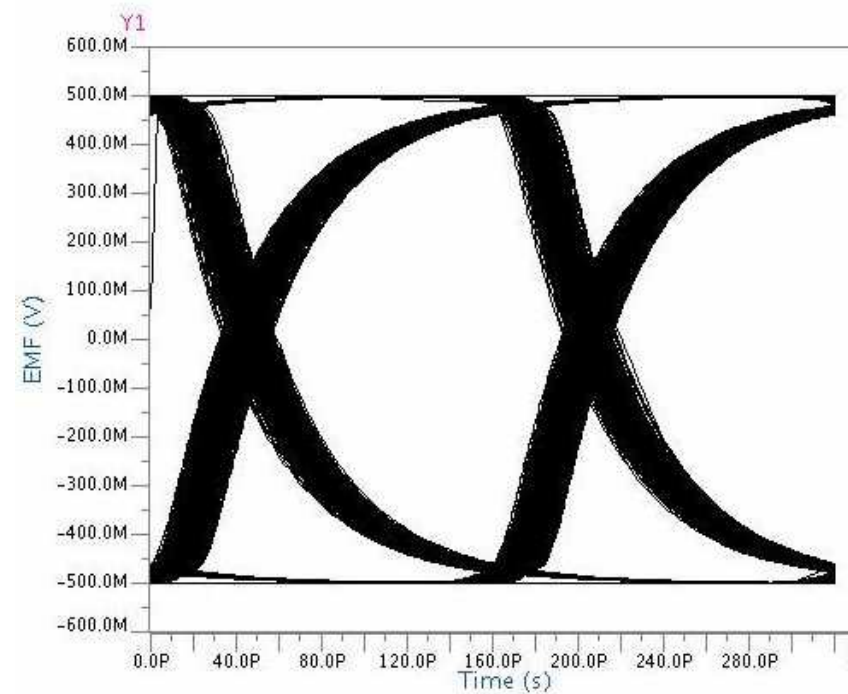 - Nominal condition
  - TX FFE on RX DFE on

Vendor A

(Verilog-AMS)

7 inch channel

10 nF

10 nF

Vendor B

(VHDL-AMS)

Verilog-AMS to VHDL-AMS interoperability
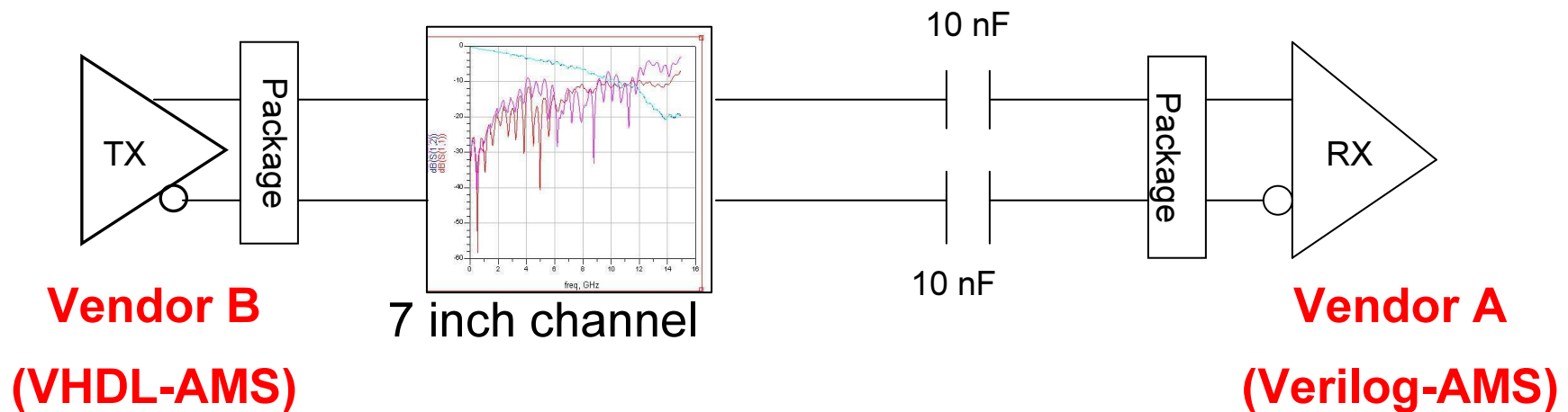
At the RX input

After the DFE

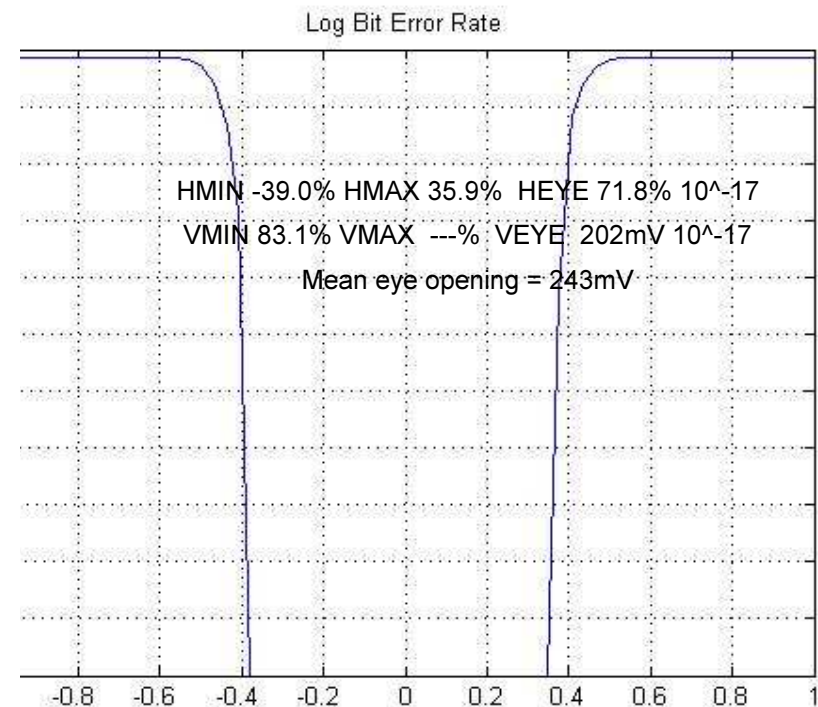# Reverse:
VHDL-AMS to Verilog-AMS interoperability

- Test conditions:

  Data Pattern: PRBS 7 running @ 6.25 Gb/s

  Nominal condition

  RX DFE on

Vendor B

(VHDL-AMS)

7 inch channel

10 nF

10 nF

Vendor A

(Verilog-AMS)

Reverse:
VHDL-AMS to Verilog-AMS interoperability

Eye diagram

Log Bit Error Rate

HMIN -39.0% HMAX 35.9% HEYE 71.8% 10^-17

VMIN 83.1% VMAX ---% VEYE 202mV 10^-17

Mean eye opening = 243mV
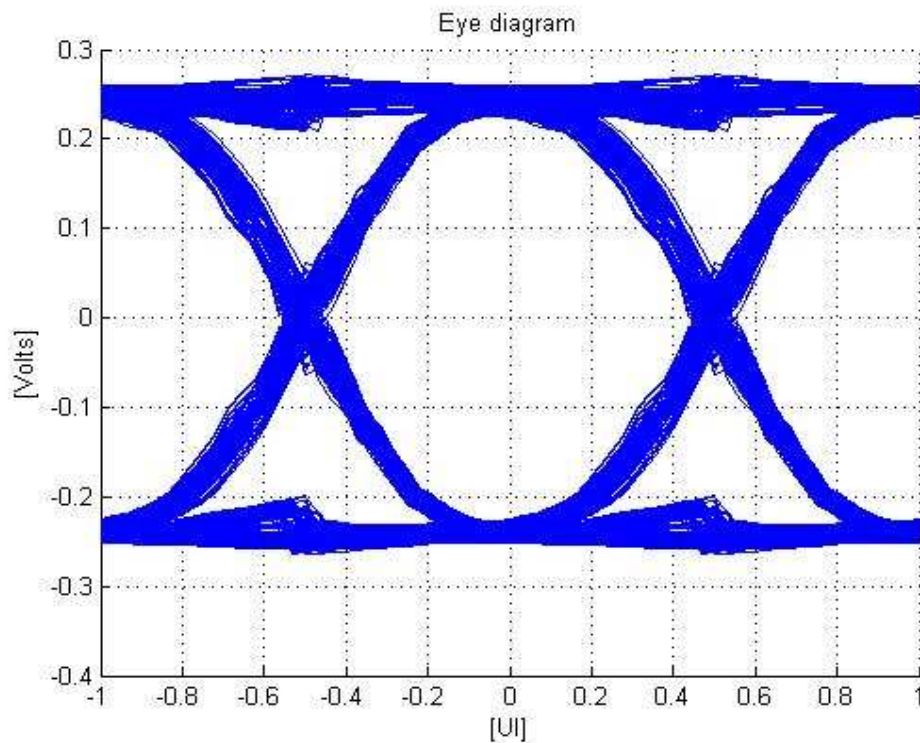
Results shown are after the DFE

# Cross-talk Simulation: Interoperability Case Study

- Link's data rate is 7.5 GHz;

- Verilog-AMS talking to Verilog-AMS (same vendor).

- NEXT is VHDL running at 6.5 GHz.

- FEXT is VHDL running at 7.5 GHz.

- No package Included.

- Numbers inside circles are showing mixed mode port numbers.
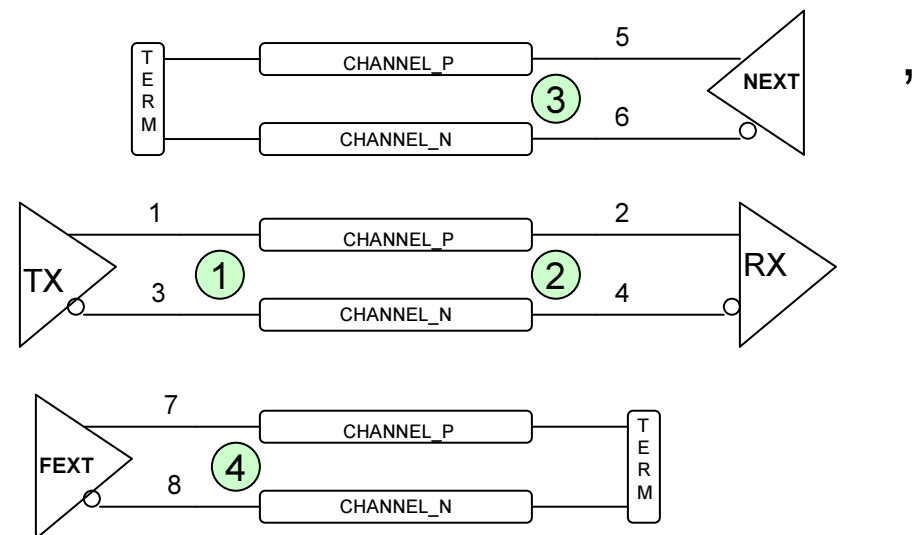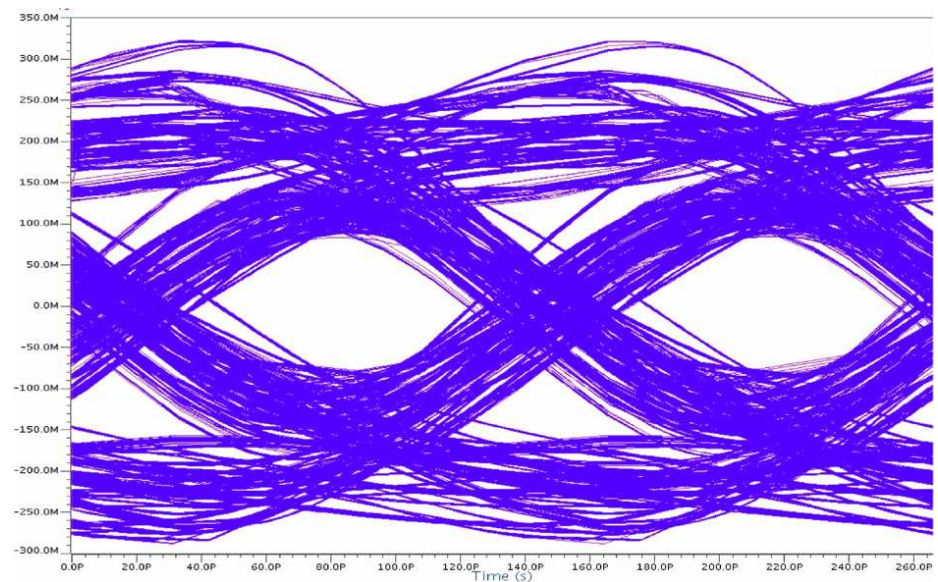

Cross-talk simulation setup

Interoperability Case Study … contd.

- Transient simulation length = 4.5 microseconds

- 7.5Gb/s PRBS 7 sent from transmitter of the link.

- 2 Identical sims: one with aggressors and one without aggressors.
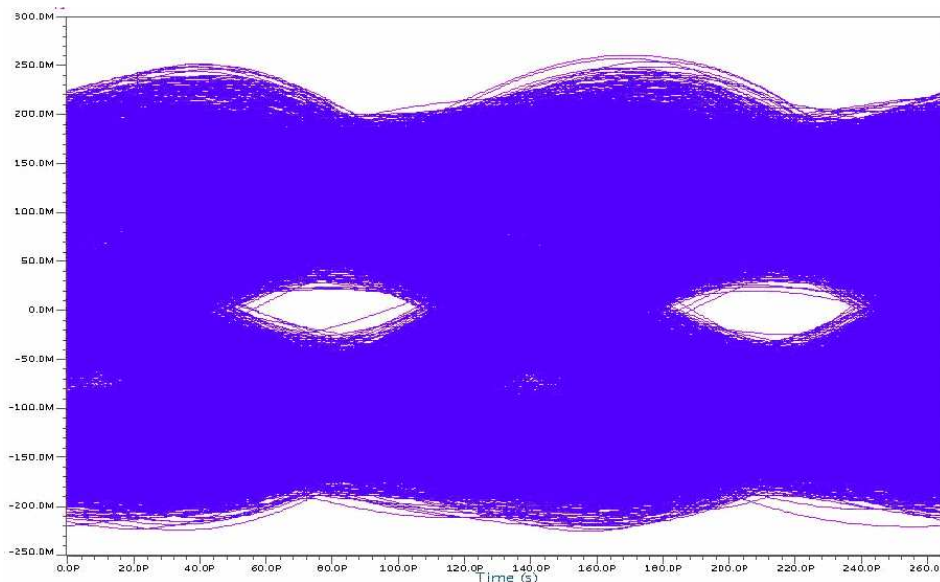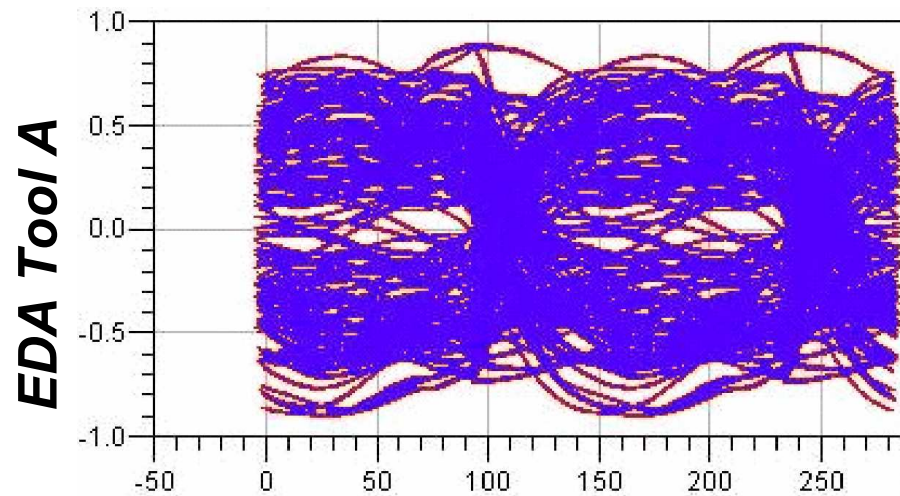

Differential signal at receiver
with Xtalk

Differential signal at receiver
without Xtalk

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- **Demonstration of VHDL-AMS to Verilog-AMS interoperability in a SerDes full channel simulation.**

- **Model interoperability across several EDA tools**

- Demonstration of post processing modules (to extrapolate BER) in fully coded AMS

Model interoperability across several EDA tools

EDA Tool A

Eye at TX for tool vendor A

Eye at RX for tool vendor A

EDA Tool B

Eye at TX for tool vendor B

Eye at RX for tool vendor B

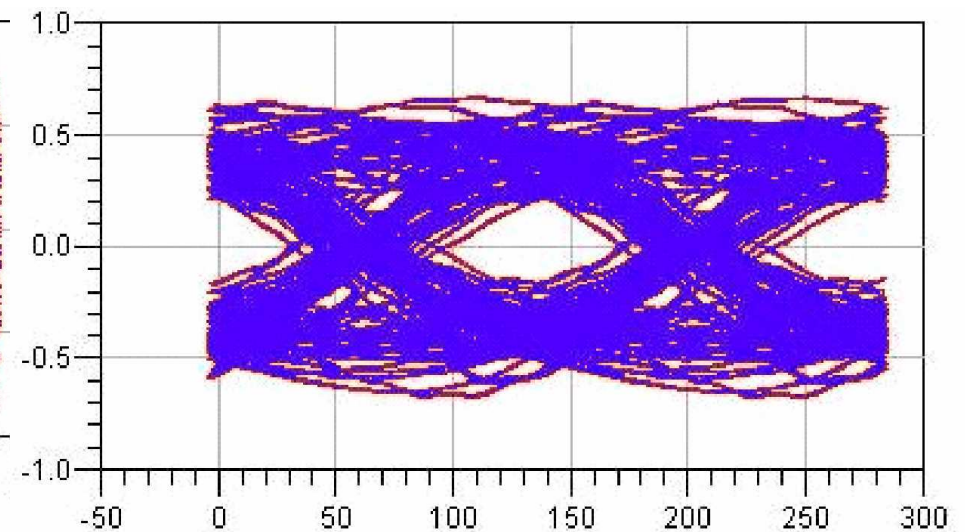**ASIC Signal Integrity and Packaging Design (ASIPD)**

Agenda

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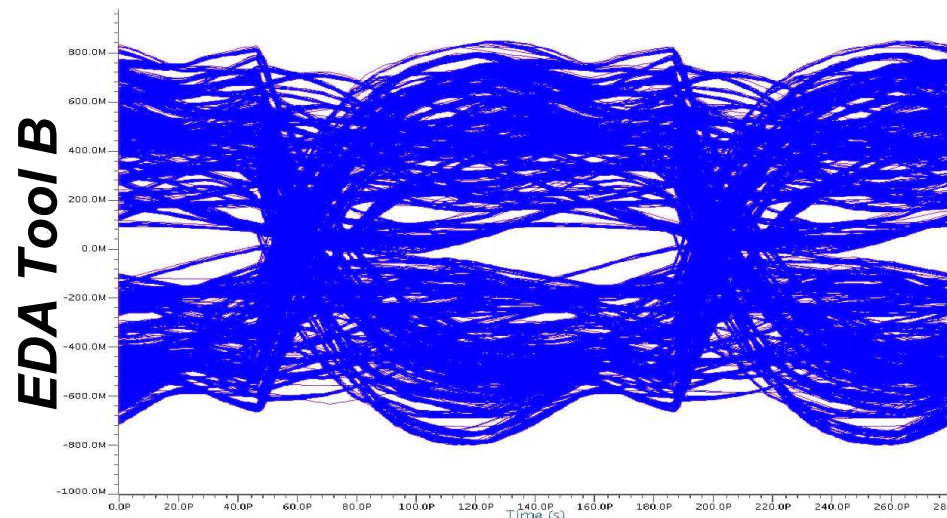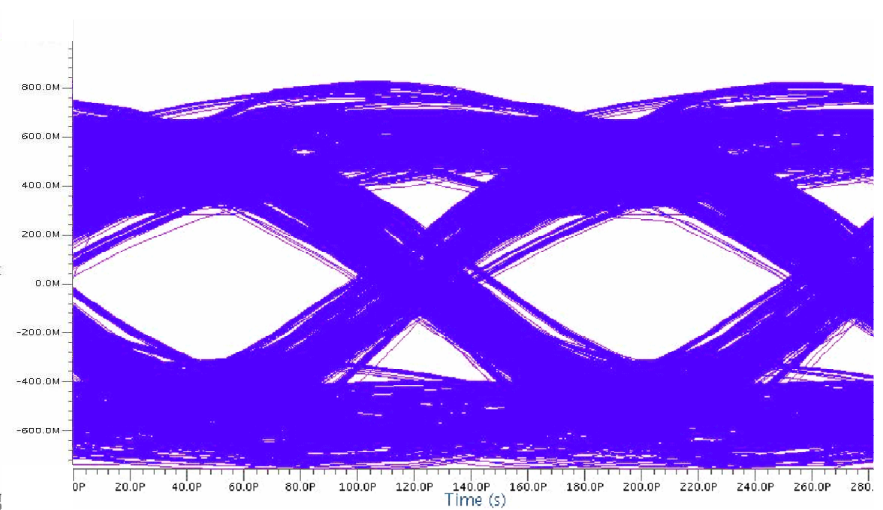- **Demonstration of post processing modules (to extrapolate BER) in fully coded AMS**

ASIC Signal Integrity and Packaging Design (ASIPD)

AMS post processing

- Demonstration of:
  - Extrapolate a time based simulation for BER metrology
  - Standardization of Signal Integrity based testing by use of post processing (independent of EDA tool)
  - Porting of Matlab based tools

- Took an existing Matlab based post processing function
  - Use as much of AMS language as possible for portability across EDA vendors
  - Creation of library of specialized Matlab functions into AMS

Special acknowledgement of Matlab code source: ST Microlectronics

Results based on AMS script

Jitter Probability Distribution Function

Bathtub Cruves, 30e6 samples
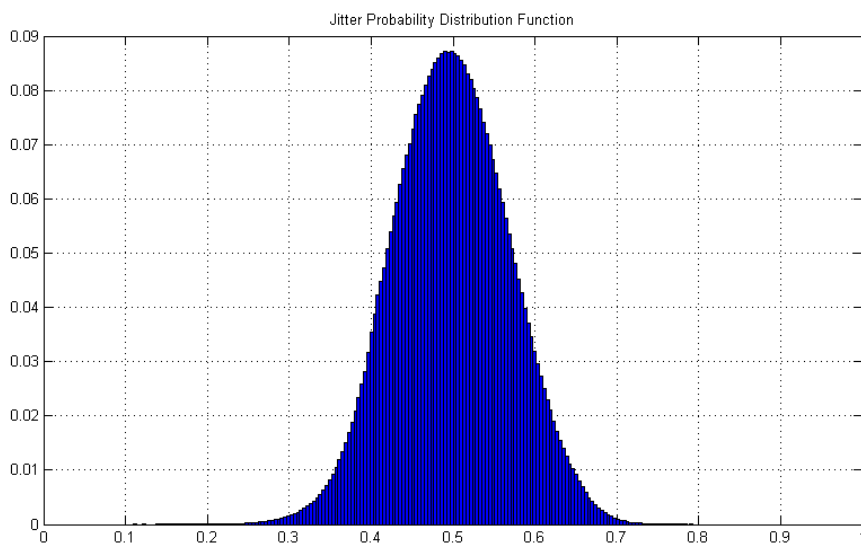
Histogram of zero crossings extracted from waveform
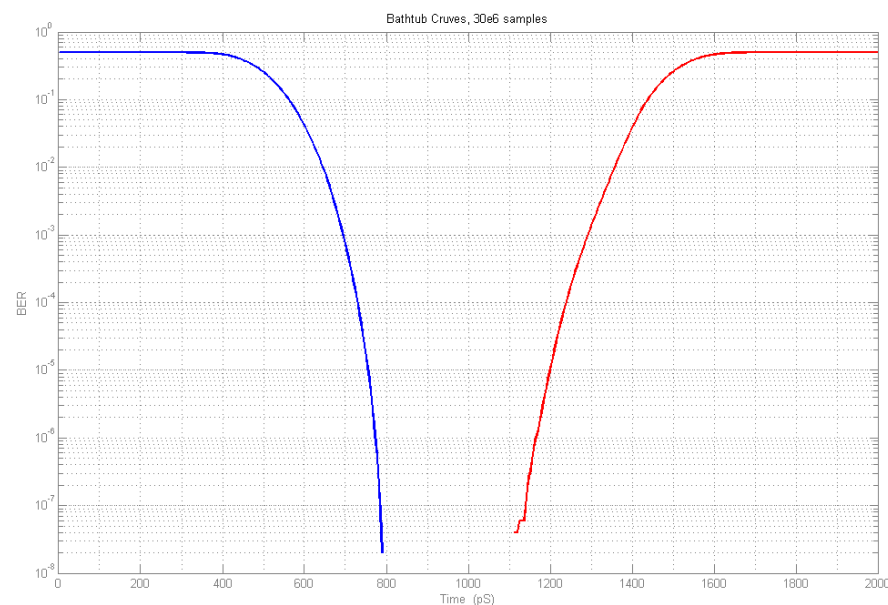
CDR based on normalized histogram dat

ASIC Signal Integrity and Packaging Design (ASIPD)   30

Learnings in translating from Matlab

- Multidimensional arrays became troublesome- but not an inherent AMS issue.

- Working around type changes in VHDL-AMS

- Certain math functions like sqrt are available- others like inverf had to be written (based on Fortran examples). Other matlab special functions such as hist were ported.

- It is possible to port over Matlab code to VHDL-AMS

- Graphical plotting is time consuming

Next Steps

- Need to avoid compiled models in favor of IP encryption. Significant work is under way with IEEE P1735

- More work needed from EDA vendors for tool features, utilities and multi-lingual support as per IBISv4.2

- Development of *AMS utilities in collaboration with Academia

- Work with our ASIC vendors for next generation *AMS models

- Simulation of higher data-rate SerDes and further modeling in *AMS

Solution providers of AMS