IBIS Advanced Technology Modeling Group (IBIS-ATM)* Status Report

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DesignCon IBIS Summit

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* Formerly IBIS-Macro

SiSoft™

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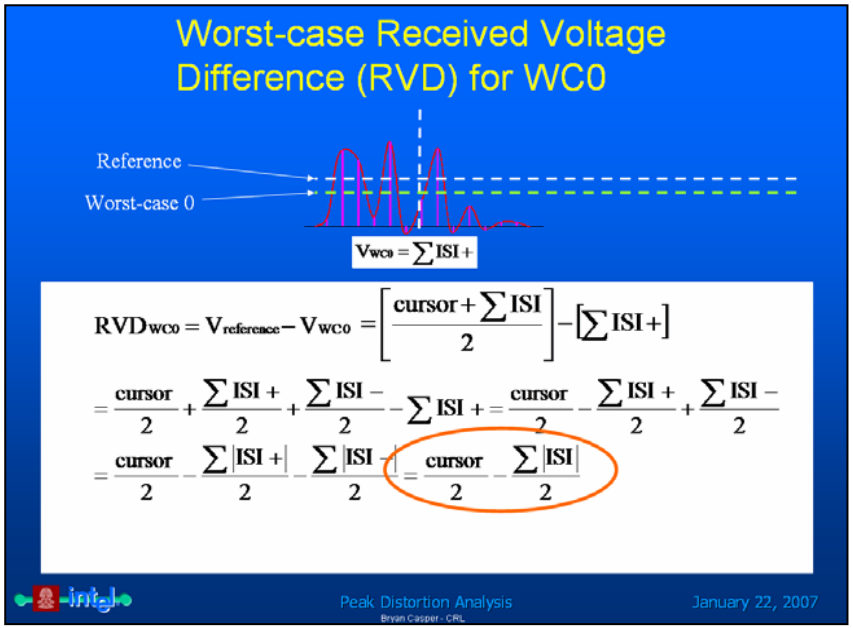
Agenda

- Updated Group Charter
- Peak Distortion Analysis
- HSpice investigations
- Cadence's Proposal / BIRD
- Circuit vs. Signal Simulation
- DLL / Executables / Encrypted Source, AMS / SystemC / Other Languages
- Terminology Presentations
- Current Status

Updated Group Charter

- Changed name to IBIS Advanced Technology Modeling Group (IBIS-ATM)
- Current goal:
  - Define a transmitter/receiver modeling standard for SERDES channel analysis that encompasses equalization and clock recovery
- The solution must:
  - Support multiple EDA vendors
  - Support multiple IC vendors
  - Protect semiconductor vendor IP
  - Support combined transmitter/receiver design
  - Support design optimization

Peak Distortion Analysis



- Analytical method for predicting maximum eye closure based on channel pulse response
- Implemented in VHDL-AMS and demonstrated by Arpad Muranyi of Intel

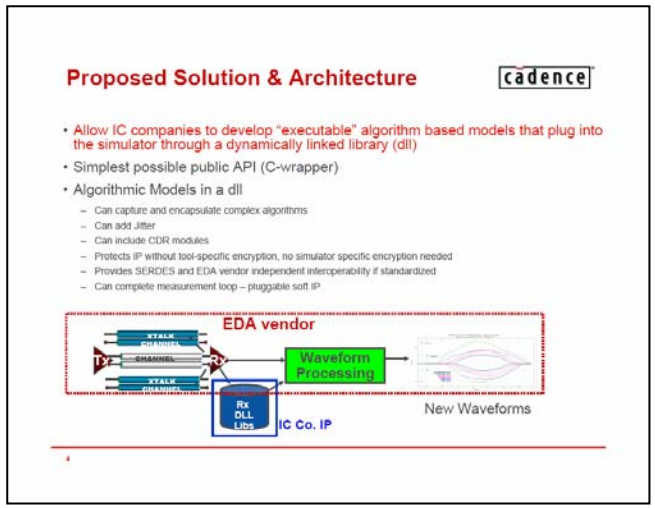
Reference presentation:

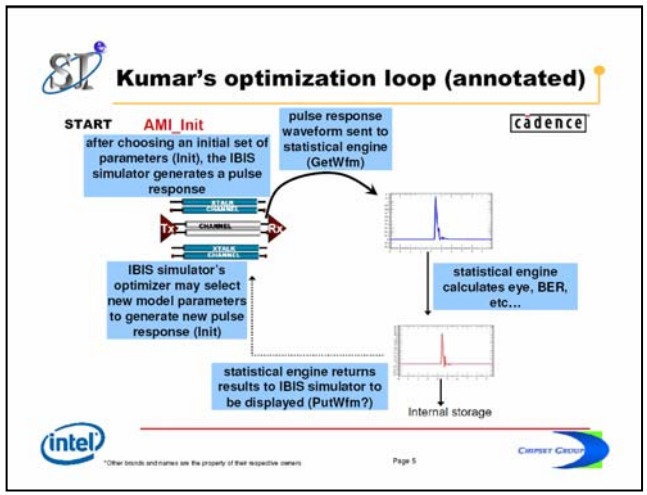
http://download.intel.com/education/highered/signal/ELCT865/Class2_15_16_Peak_Distortion_Analysis.ppt

HSpice Investigations

- Request from Cadence at Asian IBIS Summit to extend [External Model] Spice syntax to allow parameter passing
  - Berkeley Spice [currently supported] does not provide this
- Asked Synopsys if they would make HSpice syntax publicly available [de facto standard]
  - Synopsys declined, not wanting to restrict future extensions to HSpice's syntax
- Issue currently considered closed
  - Open invitation to group to propose specific syntax for parameter passing

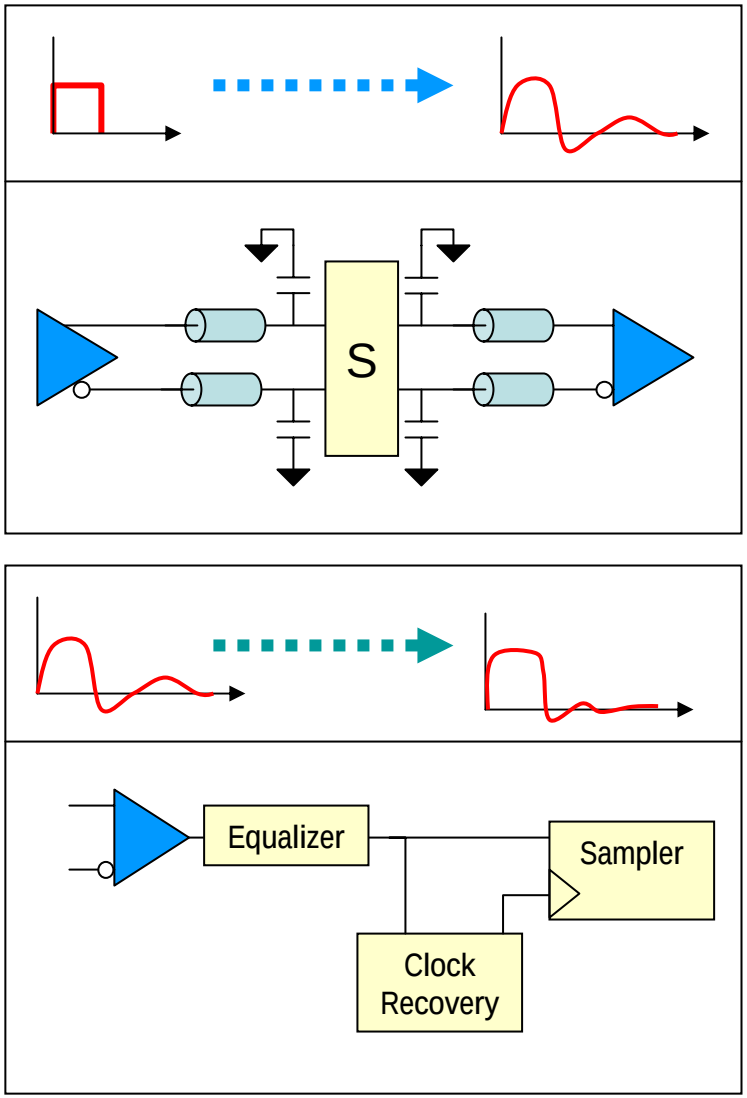
Cadence's AMI Proposal





- Multiple presentations at:
  - http://www.vhdl.org/pub/ibis/macromodel_wip/
- Ongoing discussions of Cadence's proposal and algorithms therein
- Related discussions on details of channel characterization and modeling
- Cadence presented proposal as draft IBIS BIRD

Circuit Simulation vs. Signal Processing

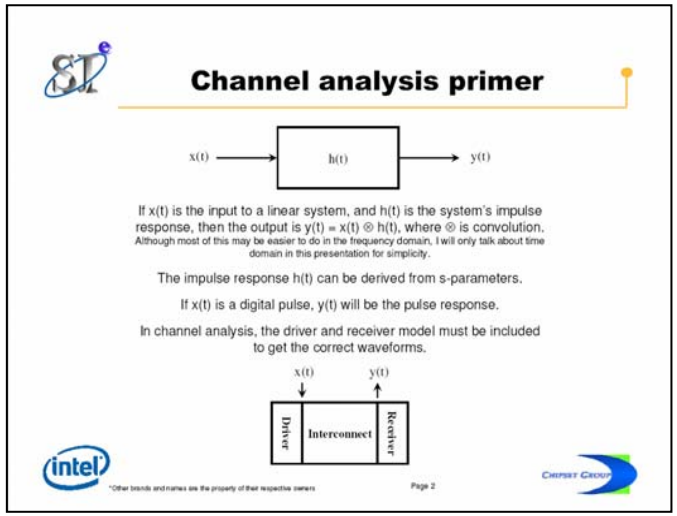


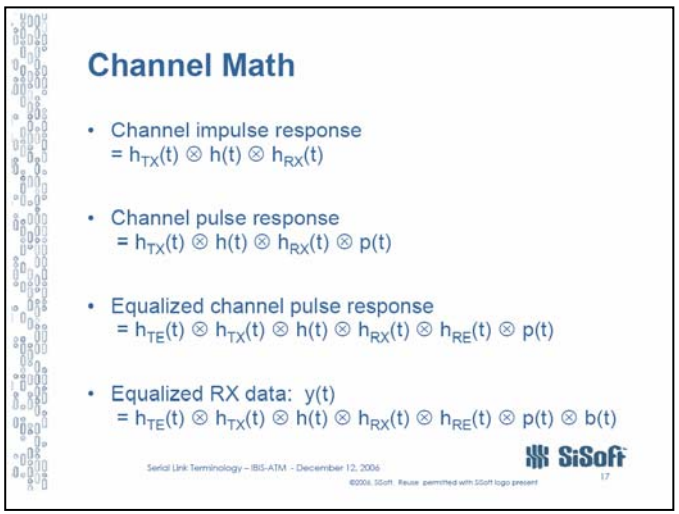
- Circuit Modeling/Simulation
  - Interconnect models
  - Network characterization
  - Impulse Response
  - Pulse Response
- Signal Processing Analysis
  - Transmitter equalization
  - Receiver equalization
  - Time-domain waveform generation (convolution)
  - Clock recovery

DLL / Executables / Encrypted Source, AMS / SystemC / Other Languages

- Secondary / deployment issue
- Extensively discussed model development and distribution:
  - Tradeoffs between different development languages
  - System language trends
  - Advantages / disadvantages of different distribution methods (.dll vs. executable vs. encrypted source)
  - Strengths and weaknesses of different IP-protection schemes

Terminology Presentations





- Intel
  - http://www.vhdl.org/pub/ibis/macromodel_wip/archive/20061024/arpadmuranyi/Channel%20analysis%20flow%20with%20IBIS/IBIS_API_flow.pdf
  - TinyURL version:
    - http://tinyurl.com/238mdw
- SiSoft
  - http://www.vhdl.org/pub/ibis/macromodel_wip/archive/20061212/toddwesterhoff/Serial%20Link%20Terminology/serial_link_terminology.pdf
  - TinyURL version:
    - http://tinyurl.com/yuhxn9

Current Status

- Still need better definition of target audience
  - Silicon/circuit designers?
  - Model developers?
  - System designers?
- Network characterization terminology still unclear
  - Impulse response vs. pulse response vs. transfer function vs. pole/zero representations
- Cadence's proposal under review
  - Ongoing discussions of detailed implications
  - SiSoft recommendations for enhancement
    - Mechanism to publish model parameters for EDA tool
    - Need analysis methodology-independent models
- Still exploring different analytical approaches

For More Information

- IBIS-ATM / IBIS-Macro Website
  - www.eda.org/pub/ibis/macromodel_wip/
- IBIS-Macro mail reflector
  - Mail to: ibis-macro-request@freelists.org
  - Subject: subscribe
- IBIS-Macro mail archives
  - www.freelists.org/archives/ibis-macro