Adaptive DFE Modeling using IBISv4.2

Ehsan Kabir, Susmita Mutsuddy, Abdulrahman Rafiq, Luis Boluña

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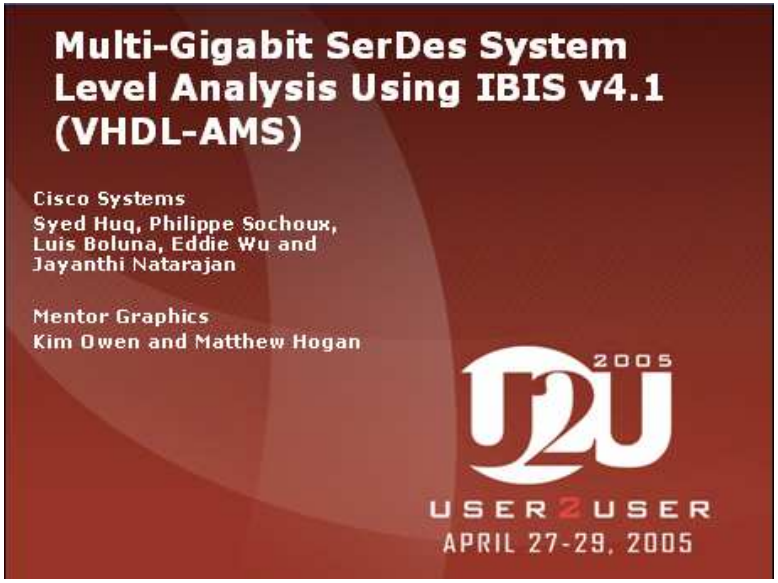
ASIC Signal Integrity and Packaging Design (ASIPD)

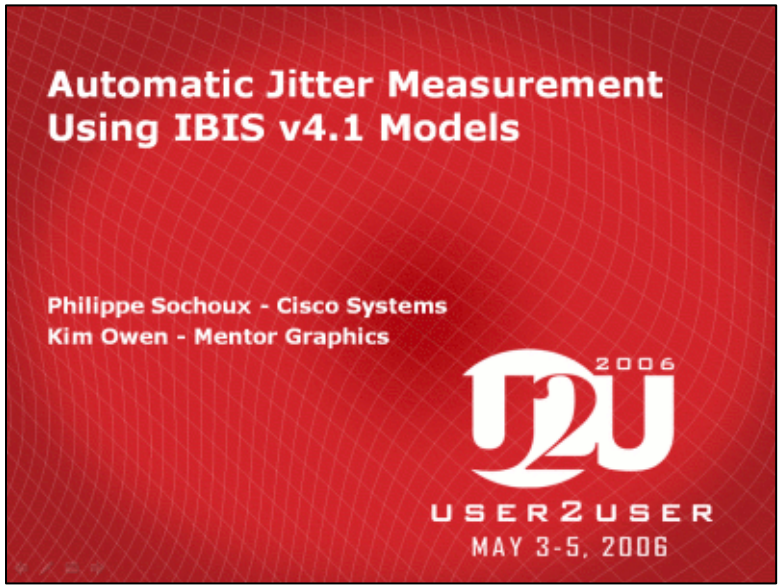
Today's Agenda

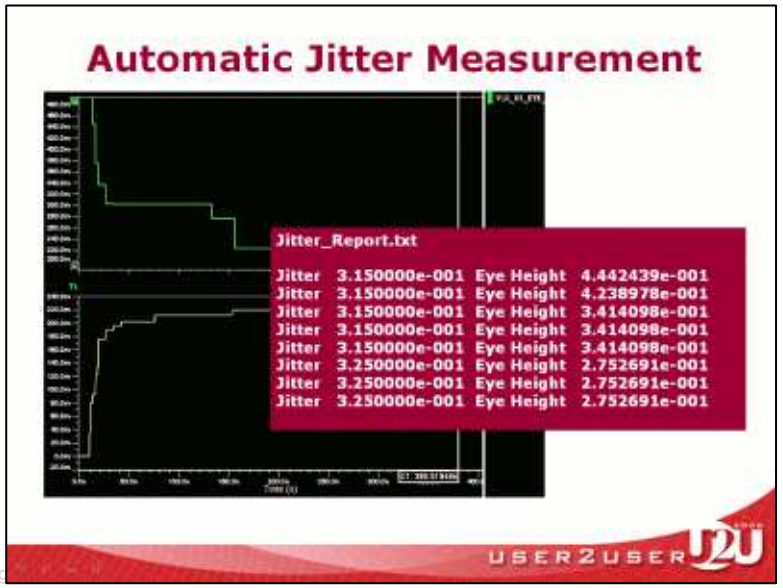
- Brief review of Past Work: where we left off...
- Brief Overview of the Challenge today in Modeling
- What is a DFE?
  - DFE diagram
  - LMS Algorithm
- VHDL Code:
  - The modeling process
  - AMS Code
  - Results
  - Learnings
- What's next
- Conclusions

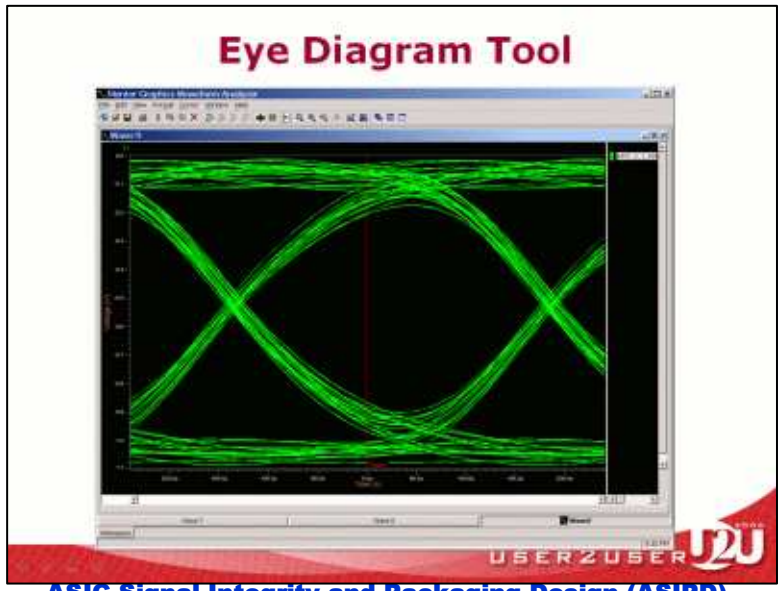
U2U 2005



U2U 2006







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Challenges

- SerDes Technology is seen in many applications today
  - XAUI, CEI, PCI-E, XFI, SATA, FC etc
- Limitations in Modeling features of SerDes using HSPICE
- Proprietary solutions in modeling is not acceptable due to interoperability issues
- DFE can be a complex feature to model and this paper will attempt to address this challenge using IBISv4.2

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What is a DFE ?

- A Decision Feedback Equalizer is a digital equalizer design to remove primarily Intersymbol Interference

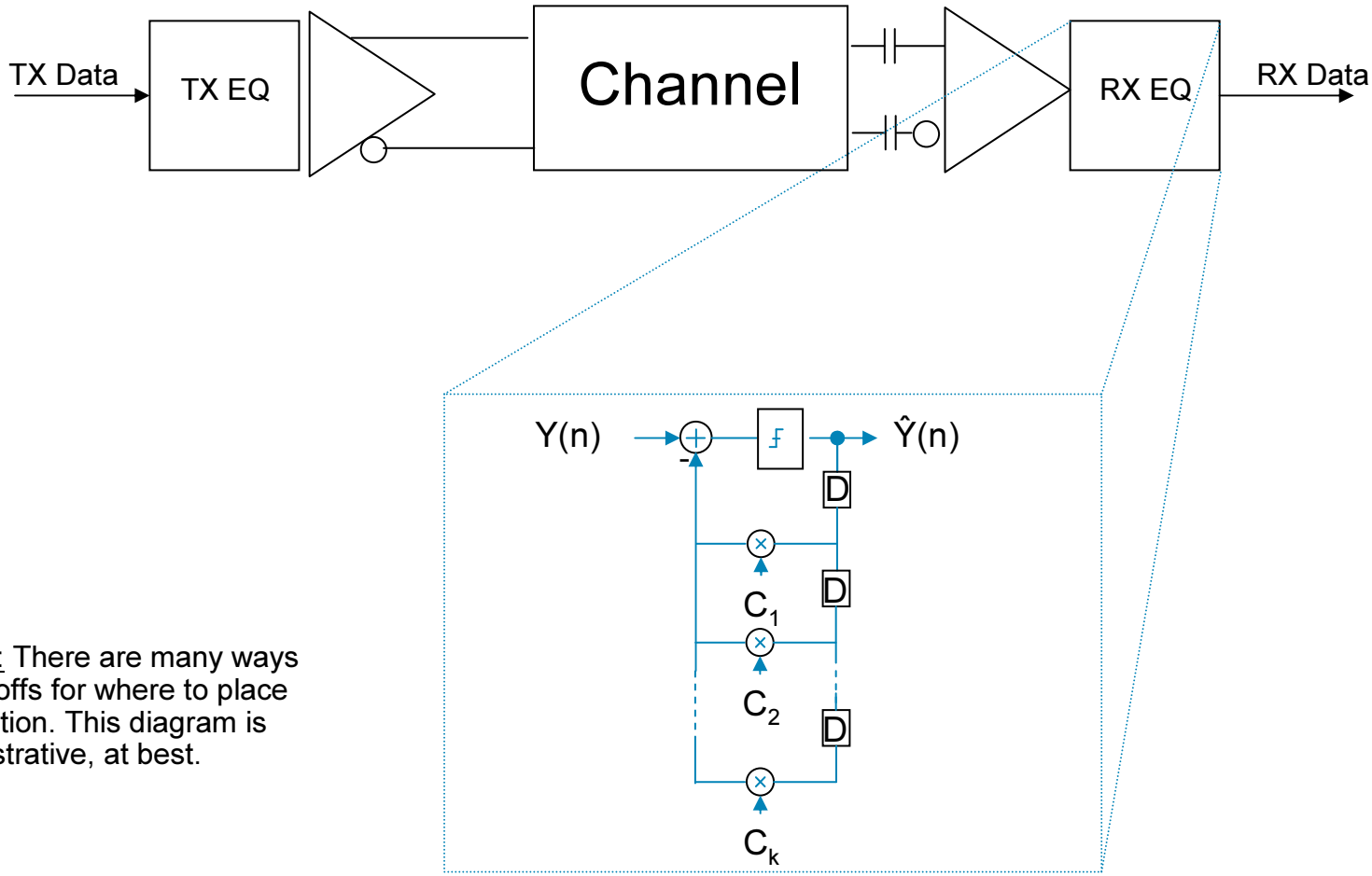
  –Unlike other filters the DFE does not invert the channel, it removes ISI

  –Does not amplify noise

  –Can accumulate errors

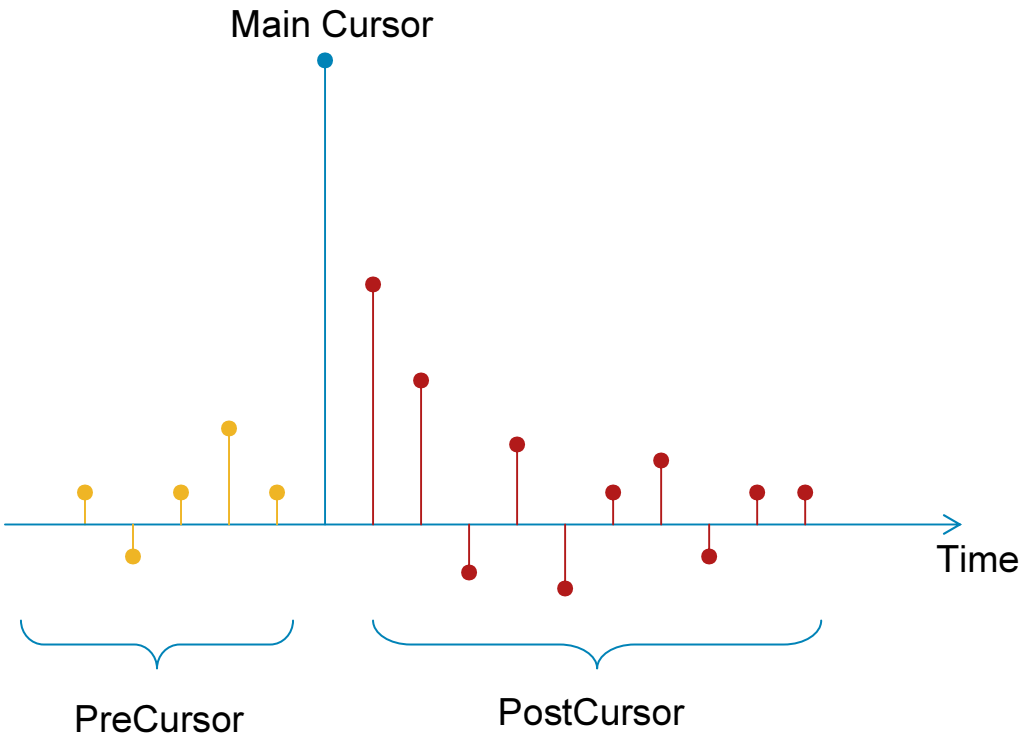
  –Feedforward EQ needed to reshape and remove precursor

What is a DFE? (2)



Disclaimer: There are many ways and tradeoffs for where to place equalization. This diagram is illustrative, at best.

What is a DFE? (3)
Response of a channel



Many creative and innovative ways to architect a DFE…

TABLE I
PREVIOUS MULTI-GB/S RECEIVERS WITH DFE

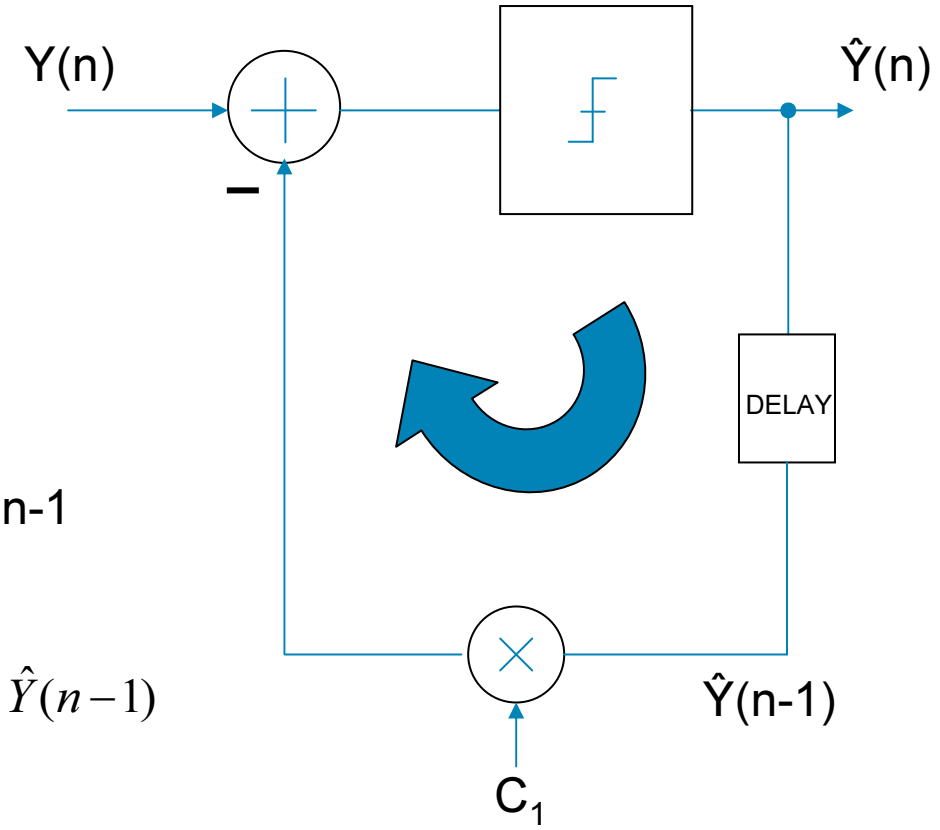
[Ref] Author (Year)	Baud rate	Receiver architecture	DFE type
[2] Zerbe (JSSC '03)	6.4-10Gb/s	2× interleaved, 2-PAM/4-PAM	5-tap DFE for >5th post-cursor ISI
[3] Balan (CICC '04)	6.4Gb/s	4× interleaved, 2-bit ADC	4-tap DFE, loop-unrolled
[4] Stojanovic (JSSC '05)	5-10Gb/s	Single-path, 2-PAM w/ DFE	1-tap DFE, loop-unrolled
[5] Krishnapura (ISSCC '05)	5Gb/s	Single-path	3-tap DFE
[6] Sorna (ISSCC '05)	6.4Gb/s	Single-path	5-tap DFE
[7] Krishna (ISSCC '05)	0.6-9.6Gb/s	2× interleaved	1-tap DFE, loop-unrolled
[8] Payne (ISSCC '05)	6.25Gb/s	2× interleaved	4-tap DFE

Table from Aida Varzaghani and Chih-Kong Ken Yang, April, 2006 JSSC

- Mixed Signal DFEs
- Analog DFEs
- All Digital DFEs

- Loop unrolling DFEs [Pahri '90, Kasturia '91, Stojanovic VLSI '04]
- Mixed Signal DFE [Brown ISSCC '97]
- RAM based DFE [Brown ISSCC '97]
- Mixed Signal DFE [Le, JSSC '02]
- Current Mode DFE [Wu, DesignCon '04]
- Look Ahead DFE [Kajley JSSC '97]
- Time Interleaved A/D DFE [Varzaghani JSSC '06]

1-tap DFE



Y(n) = input

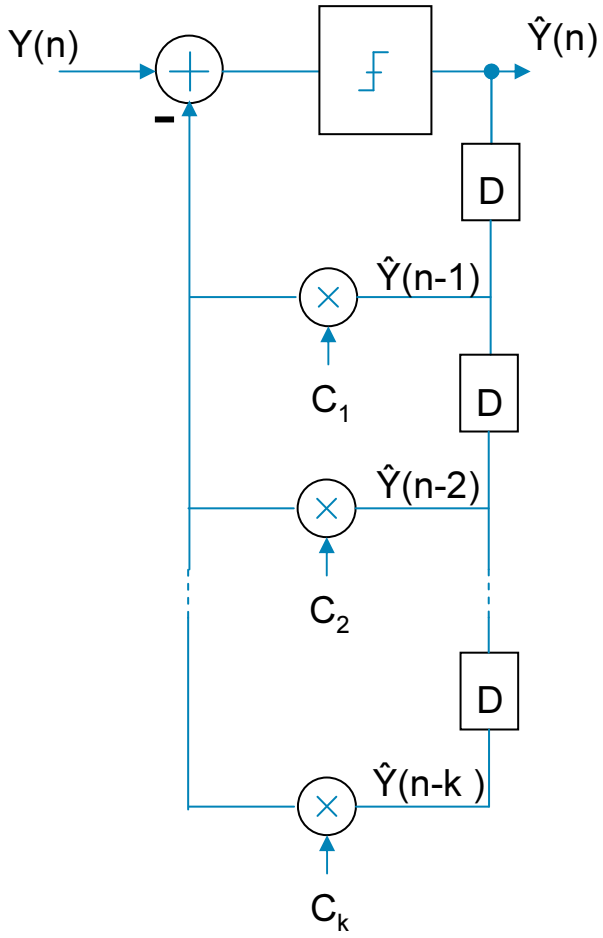
Ŷ(n) = digitized input at time n

Ŷ(n-1) = digitized input at time n-1

$$\hat{Y}(n)\Big|_{n=1}^{length\_of\_symbols} = Y(n) - C_1 * \hat{Y}(n-1)$$

The decision, multiplication and addition must all take place within one symbol time, as shown by arrow

Multiple tap DFE

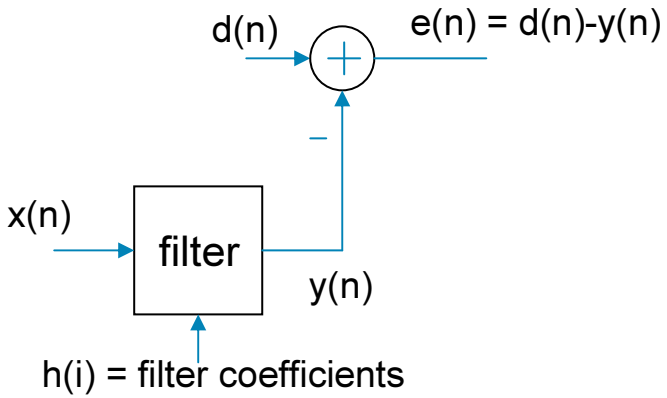


$$\hat{Y}(n)\Big|_{n=1}^{length\_of\_symbols} = Y(n) - C_k * \hat{Y}(n-k)$$

for k=1 to k taps

Algorithm – LMS

- LMS “Least Mean Square”
- Based on a gradient descent algorithm.



$$h_{n+1}(i) = h_n(i) + \frac{\mu}{2}\left\{-\left(\frac{\partial}{\partial h_n(i)}\left(|e|^2\right)\right)\right\} \qquad [\text{eqn } 1]$$

Rearranging terms for derivative portion,

$$\frac{\partial}{\partial h(i)}\left(|e|^2\right) = 2\frac{\partial}{\partial h(i)}(e)e = 2\frac{\partial}{\partial h(i)}(d-y)e = \frac{\partial}{\partial h(i)}\left(d - \sum_{i=0}^{N-1}(h(i)x(n-i))\right)e$$

$$\frac{\partial}{\partial h(i)}\left(|e|^2\right) = 2(-(x(n-i)))e \qquad [\text{eqn } 2]$$

plugged back into eqn 1,

$$h_{n+1}(i) = h_n(i) + \mu e x(n-i) \qquad [\text{eqn } 3]$$

coeff update

current coeff

previous symbol

error

Update step size

[Reference]

Other Adaptive Algorithms

Please note that there are other variations and algorithms found in academia/industry. Each has its merit and only two are mentioned here.

- Sign Algorithms
- Zero Forcing Algorithms
- etc., etc.

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Sharing our experience in creating the model

- Began with a 1 tap DFE in Matlab running at 6.25Gb/s, fixed coefficient.
- Converted this 1 tap 6.25Gb/s DFE model to VHDL-AMS
- Expanded this model to a multiple tap DFE model
- Added an LMS adaptive algorithm to Matlab model.
- Converted this multiple tap 6.25Gb/s DFE model to VHDL-AMS

VHDL-AMS code (1)

- Symbol spaced random data was sent via a channel and captured into a file. Note data is defined as centered around 0 with values of either +0.5 or -0.5.

- This waveform was read from a file and then placed into a single dimensional array, z.

- Essential code describing this:

```
-- load sample from "test.dat"
    file_open(load_file_channel, "test.dat", READ_MODE);          -- opening data file of channel output
      index := 1;
      while not endfile(load_file_channel) loop
            READLINE(load_file_channel, Y);
            read (Y, sample(index));
            index := index+1;
      end loop;

    for i in  1 to Nx loop
      z(i) := sample(i);
    end loop;
```

VHDL-AMS code (2)

Essential code for DFE and adaptation algorithm:

```
for i in (N+1) to Nx loop

  k := ((i-1) * N) - (N-1);
  for j in 1 to N loop
    z(i) := tap(k) * sign(z(i-j)) + z(i);
    k := k + 1;
  end loop;

  -- Co-efficients for next sample using Standard LMS algorithm.
  k := ((i-1) * N) - (N-1);
  for j in 1 to N loop
    tap(k+N) := tap(k) + mu * (0.5 * sign(z(i)) - z(i)) * sign(z(i-j));
    k := k + 1;
  end loop;

end loop;
```

N = number of taps
Nx = length of symbols

Z = symbols

mu = LMS step size

VHDL-AMS code (3)

- Essential code for writing results to a file:

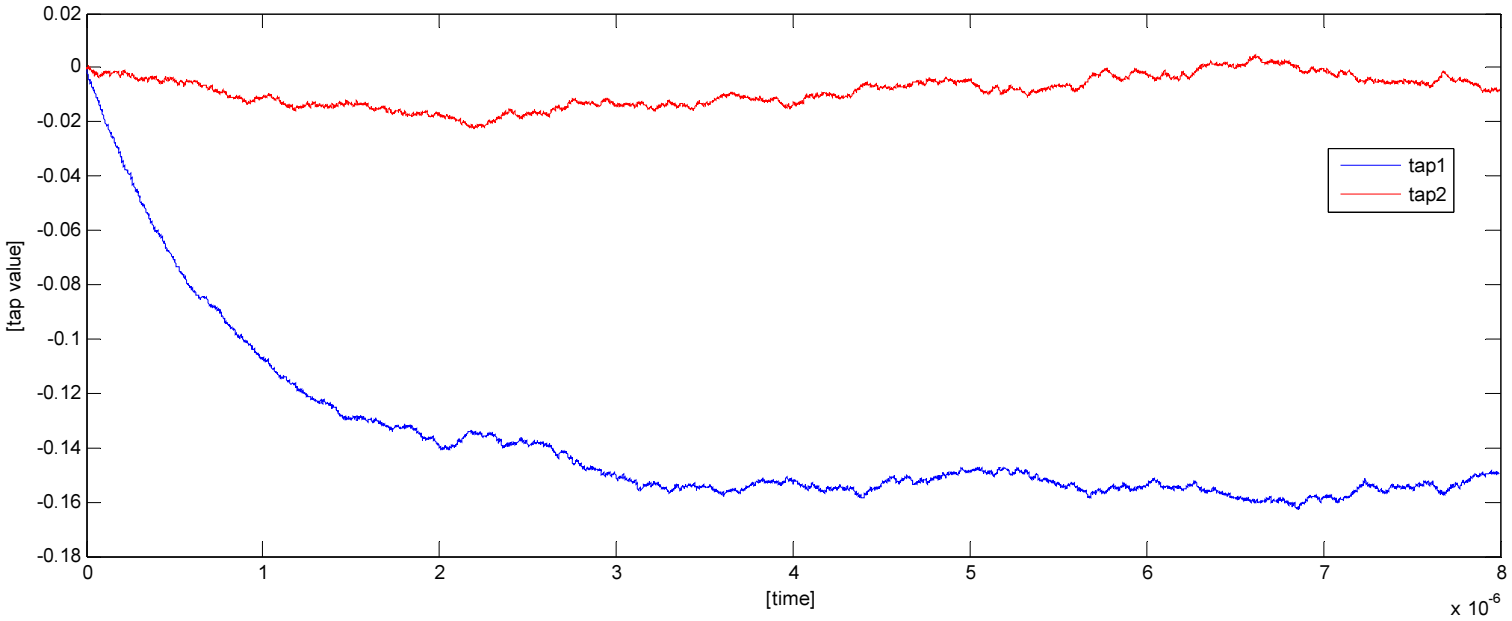
-- writing 1st,2nd,3rd,and 4th coefficients and DFE output to individual files.

```
    -- load first coeff1 to "tap1.dat"
    file_open(tap1_out, "tap1.dat", WRITE_MODE);
    index := 1;
    for index in 1 to Nx loop
       WRITELINE(tap1_out, S);
       write(S, coeff1(index));
    end loop;
```

< other taps written here as above>

```
    -- load z (DFE output)
    -- to "out.dat"
    file_open(count, "out.dat", WRITE_MODE);
         index := 1;
         for index in 1 to Nx loop
             WRITELINE(count, V);
             write(V, z(index));
         end loop;
```

AMS Results for a 6.25Gb/s Adaptive 2 tap DFE



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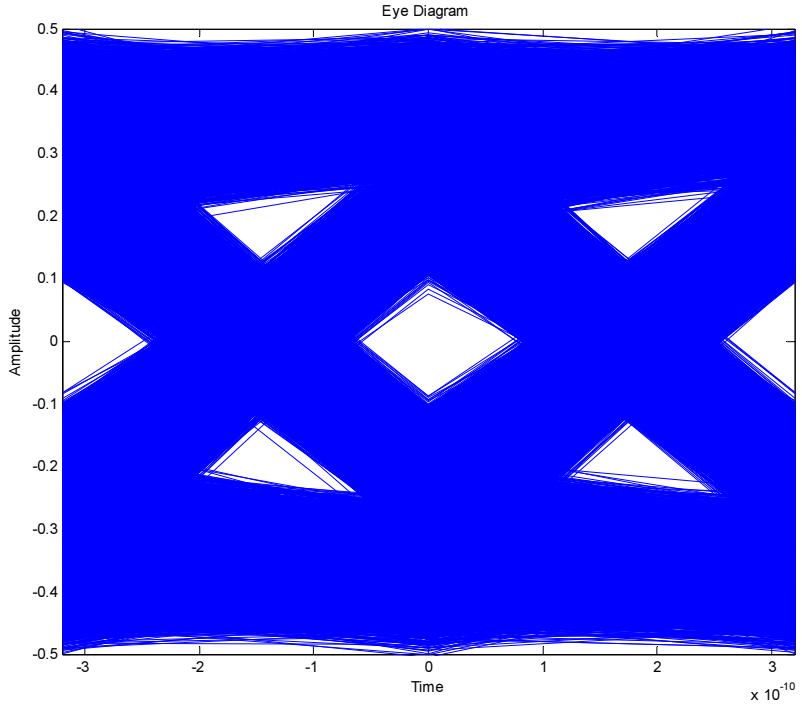
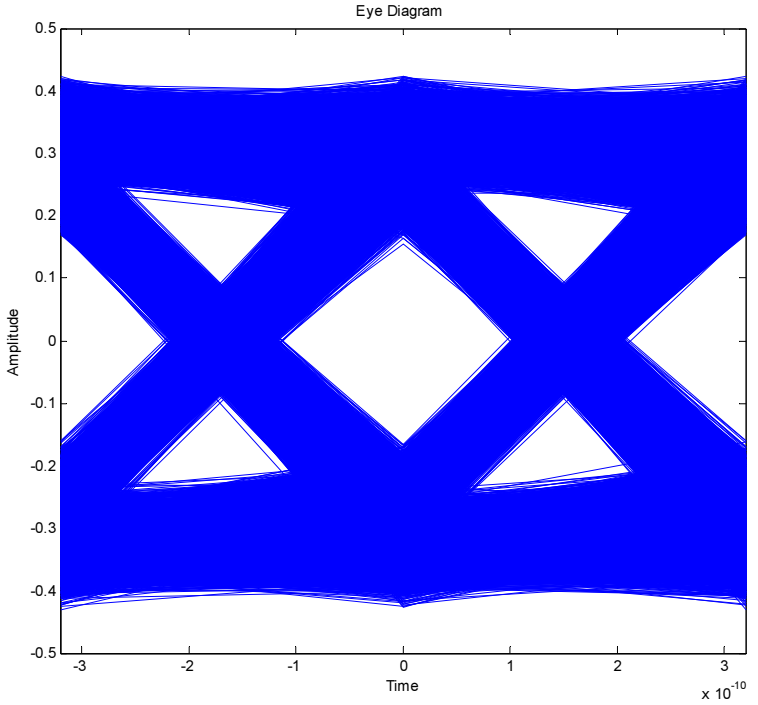
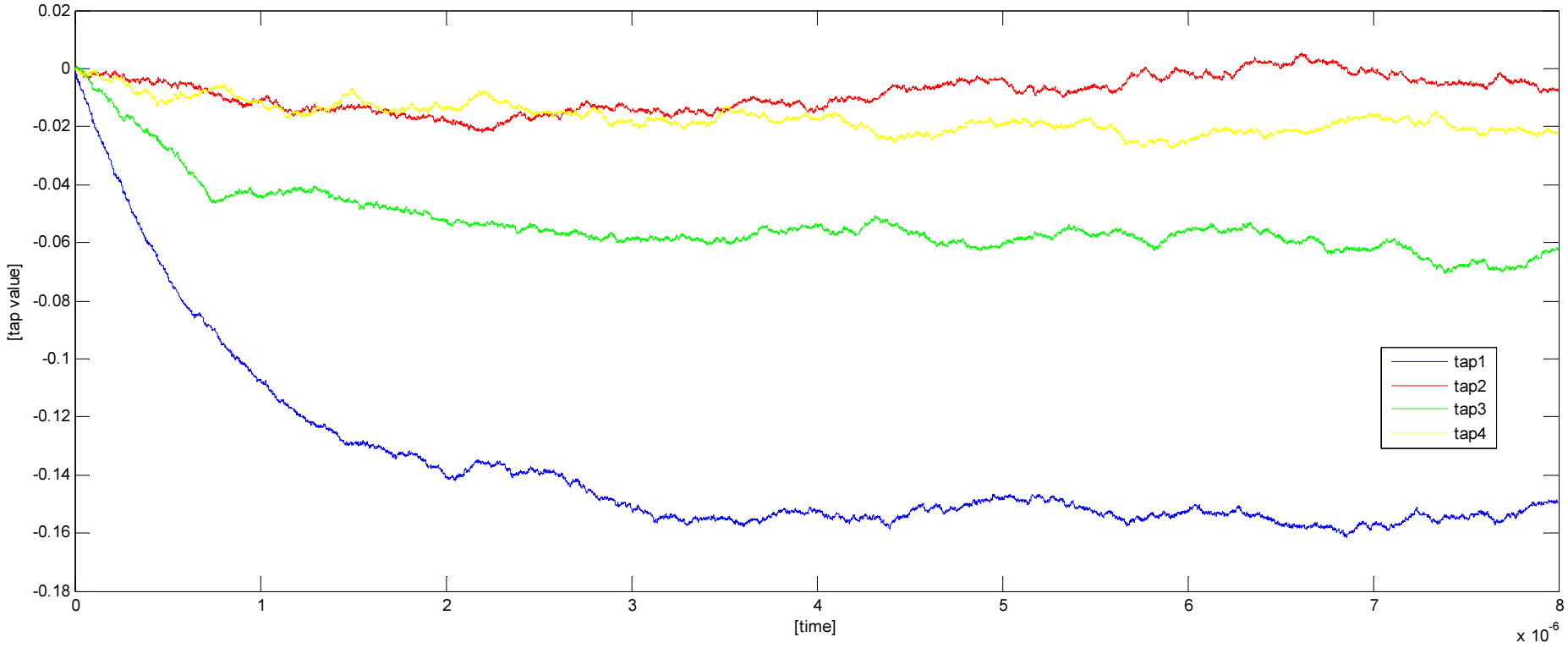
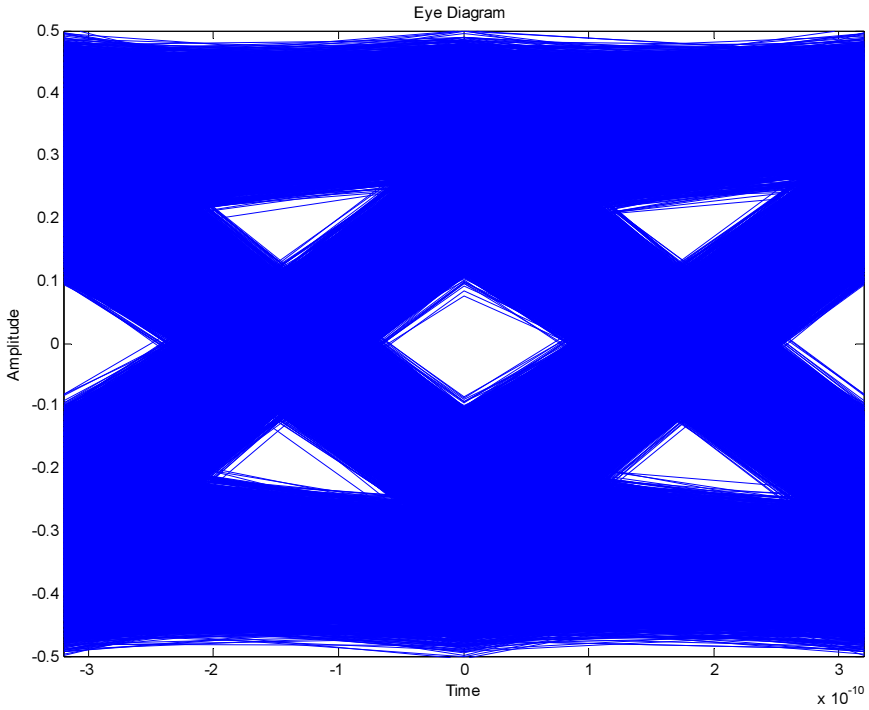


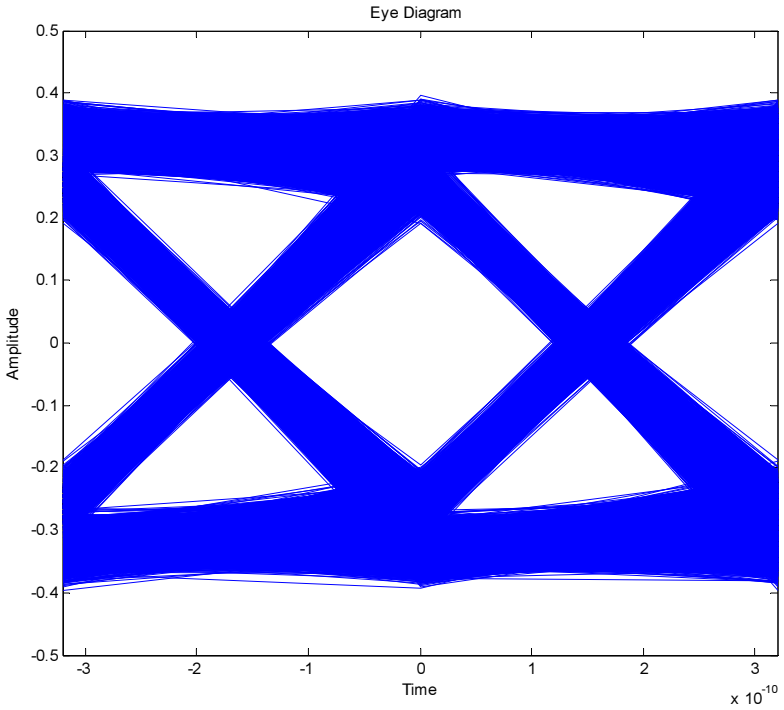


AMS Results for a 6.25Gb/s Adaptive 4 tap DFE



AMS Results for a 6.25Gb/s Adaptive 4 tap DFE





Please Note:

- The DFE model we present can be improved to include:
  - modeling of Feedback bandwidth
  - modeling of Adaptation bandwidth
  - Parasitics
  - Correlation to measurements
- Hence we are currently actively engaged with Vendors in modeling their circuitry in a more realistic manner in AMS.
- Nonetheless, we achieve our goal of demonstrating that AMS can model an Adaptive DFE.

Learnings and comments

- Reference libraries for the user can be a time saver.
- Debugging tools can be improved.
- Use of multidimensional arrays is restrictive and cumbersome.

Using AMS Models in IBIS v4.2…

- IBIS v4.2 supports multi-lingual language extensions through the use of SPICE, VHDL-AMS, Verilog-AMS to expand modeling support
- IBIS v4.2 Is extremely flexible and extendible
- IBIS v4.2 enable's users to model complex features of I/O's
- Latest IBIS version that supports Multi-lingual languages is IBIS v4.2

Calling AMS with IBIS v4.2 [External Circuit]

```
[Circuit Call] DFE2

Port_map vdd_ic  21
port_map vss_ic  22

[End Circuit Call]
|
|
[External Circuit] DFE2

Language  VHDL-AMS
|
|Corner   corner_name   file_name   subckt_name
|
Corner    Typ     DFE2.vhd   ADFE_typ2

Corner    Min     DFE2.vhd  ADFE_min2

Corner    Max    DFE2.vhd  ADFE_max2

Ports  vdd_ic  vss_ic
|
[End External Circuit]
```

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Next Steps

- Cross-functional team has been expanded to now cover SerDes Modeling, Simulation and Measurement.
- Ongoing work with 4 preferred ASIC vendors for AMS model generation. This will cover IBISv4.2 models for over a dozen current ASIC designs

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Conclusion: Summary

- IBISv4.2 with multi-lingual extension is capable of modeling complex structures of a SerDes such as a DFE
- Correlation with Matlab and VHDL-AMS achieved in modeling a DFE

Conclusion: My Message to You…

- 2005 U2U paper demonstrates IBISv4.2 VHDL AMS implementation of 3.125Gb/s TX and channel (extendable to other data rates).
- 2006 U2U paper demonstrates IBISv4.2 VHDL AMS implementation of metrics by which we can implement testability and observability portions of the channel.
- Present work here demonstrates IBISv4.2 implementation of an adaptive multitap DFE (extendable to other data rates).

- These are small significant steps. Work is progressing.

- IBISv4.2 with multi-lingual extensions is a viable format today to model various features of SerDes technology

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