HDL and IBIS 4.1 Models in a Functional DDR Memory Interface Analysis

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Project Definition

- Analyze a complete DDR memory interface in one simulation
- Simulation should consider:
  - Overshoot/Undershoot violations
  - Setup and hold timing violations
  - Include pattern dependant crosstalk between address, command, control, and data signals
  - Slew dependant timing calculations

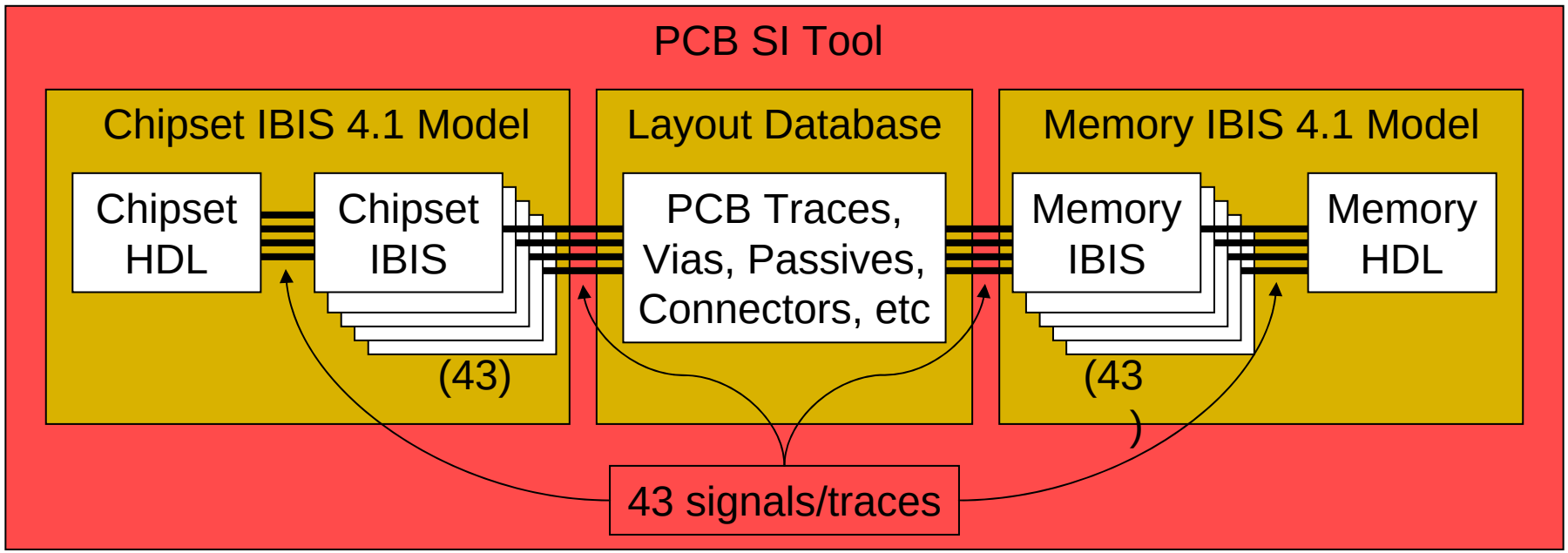
Project Approach

- Combine HDL functional models and IBIS I/O models
- HDL code takes care of timing checks
- IBIS model contains basic electrical checks
- How does it all work?

IBIS 4.1!

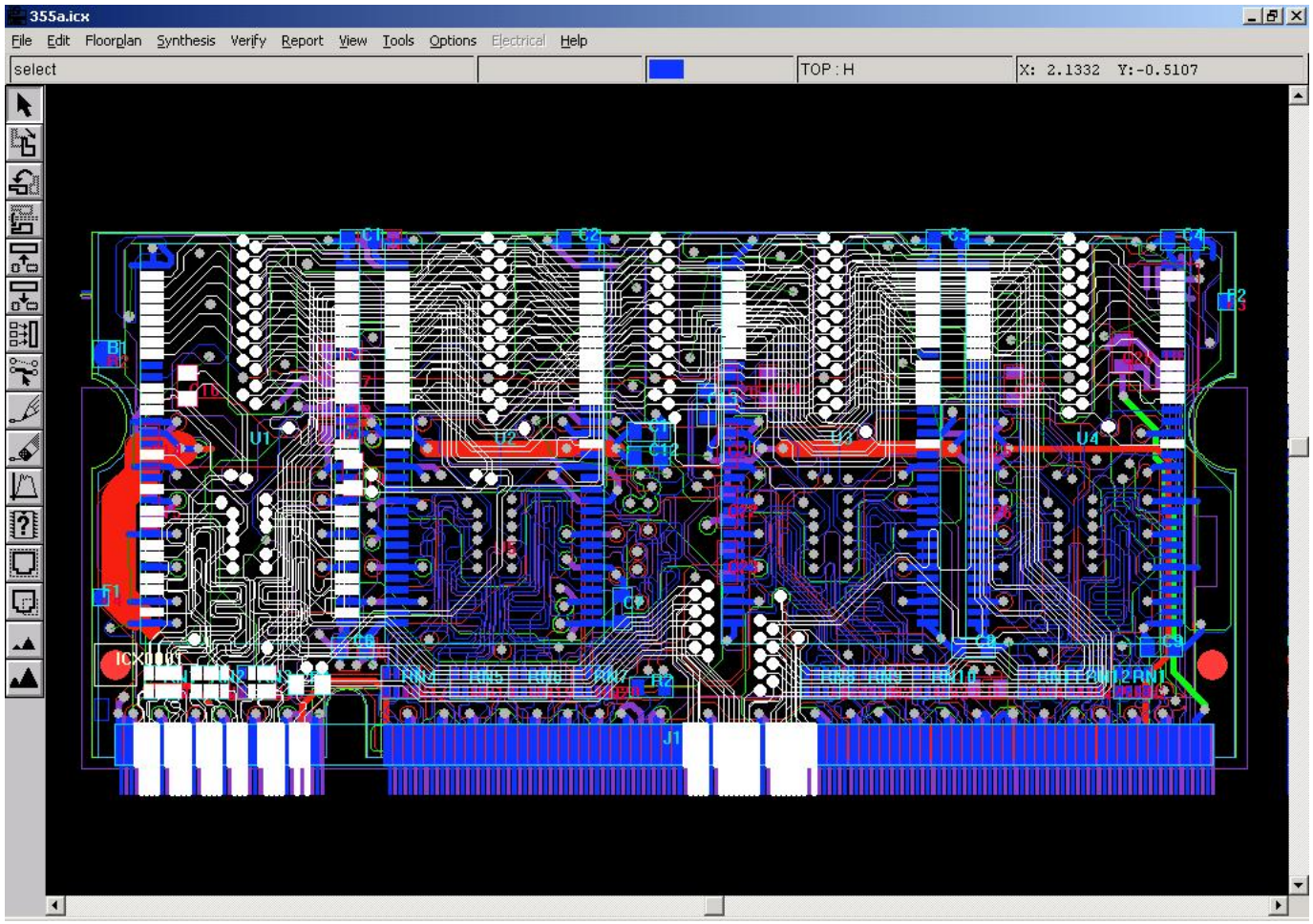
Simulation Diagram

- Connection of HDL functional models and IBIS I/O models to the physical board layout



Analysis Details

- Memory module (simulated traces highlighted in white)

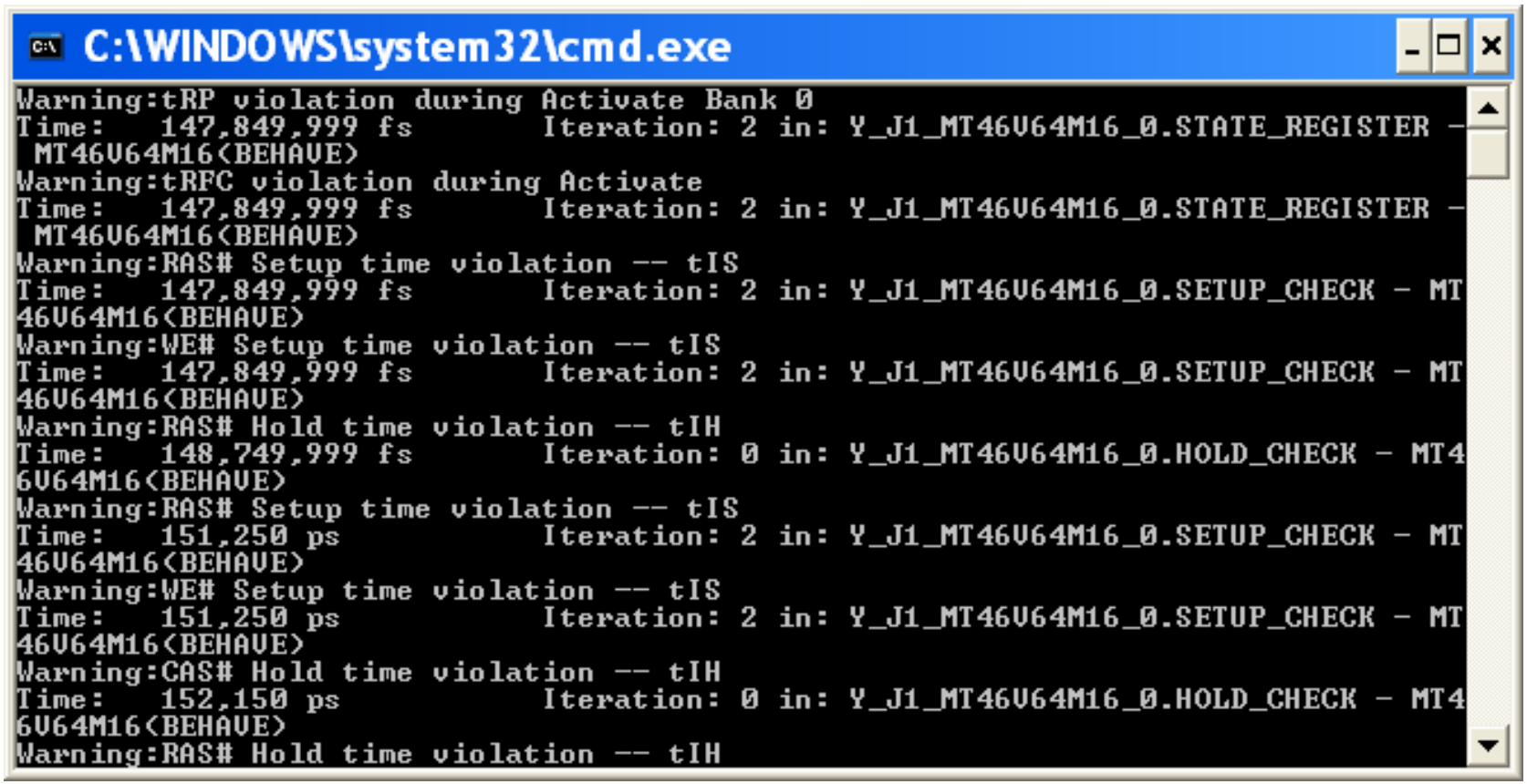


Analysis Details

- Digital code from the chipset testbench generates the system stimulus
- Random address and data pattern generators ensure realistic stimulus patterns for the Write cycle
- Memory responds to chipset commands, thus automating Read cycle data patterns
- Single simulation completes a Read and Write Cycle – multiple cycles can be run to simulate realistic bus utilization

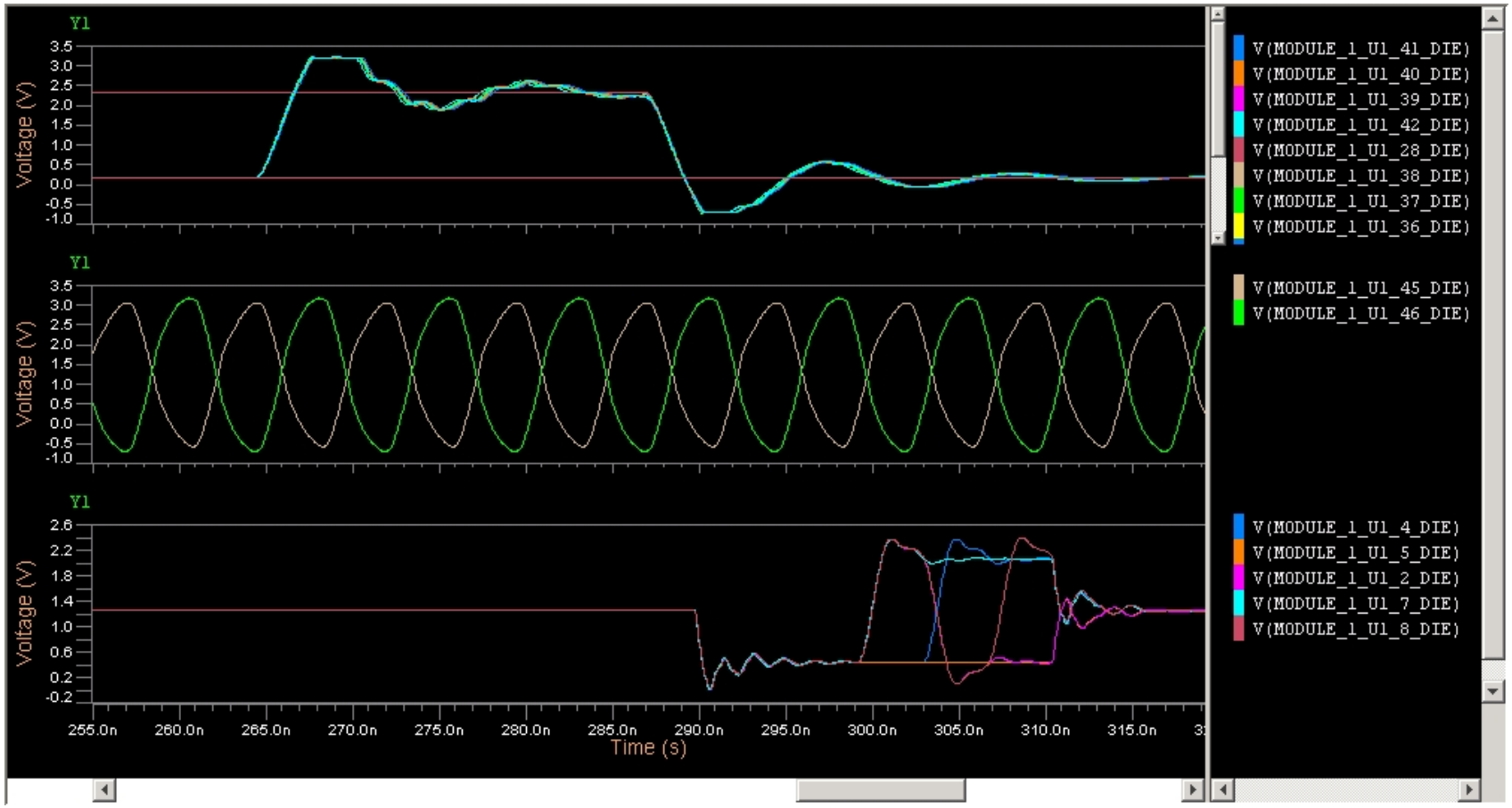
Functional SI Verification Results

- HDL models contain timing checks
- Timing violations caused by PCB effects are flagged



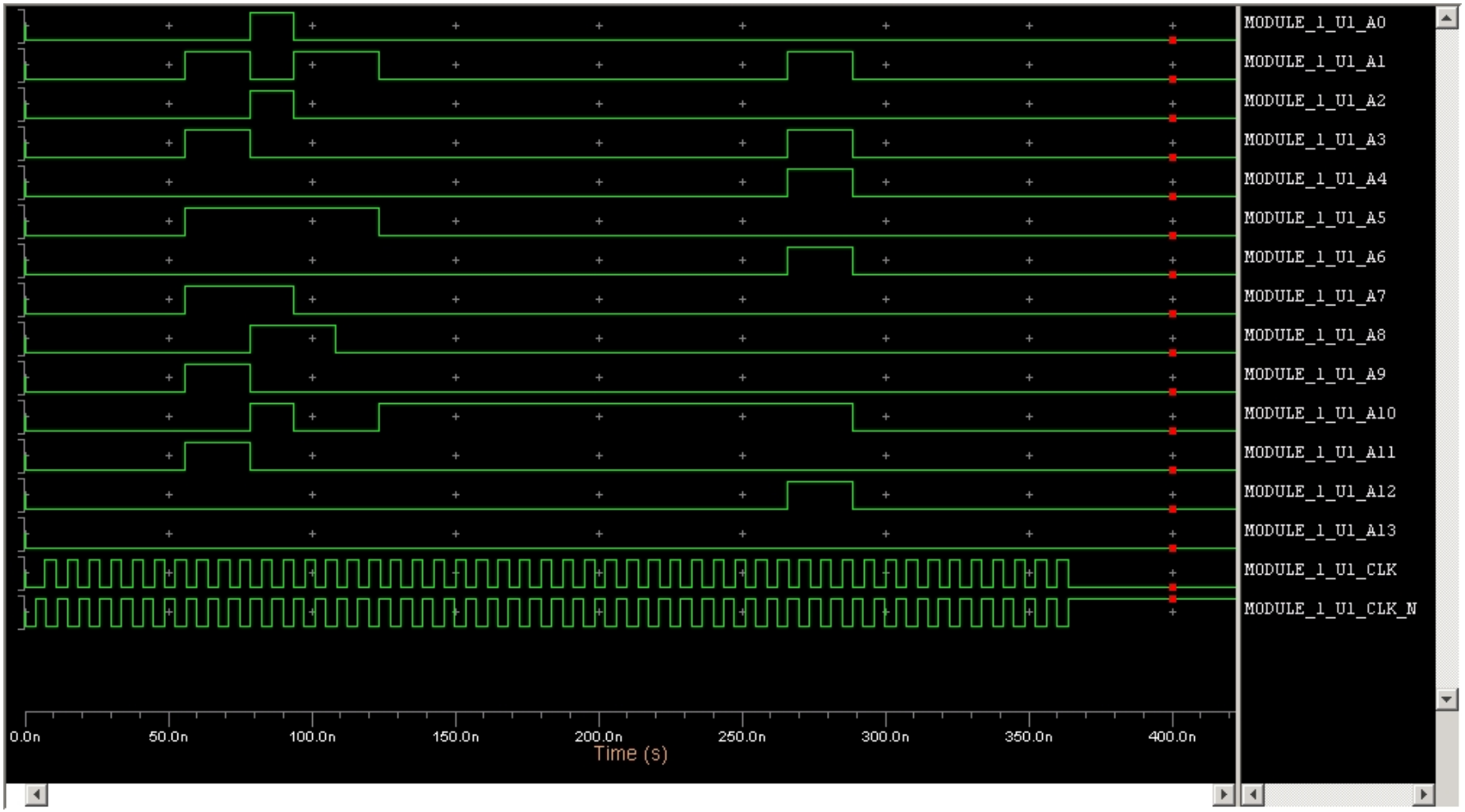
Functional SI Verification Results

- Analog Address, Clock, and Data signals at memory during a burst write from the chipset
- Simulation easily changed to generate pseudo-random or fixed address and data patterns



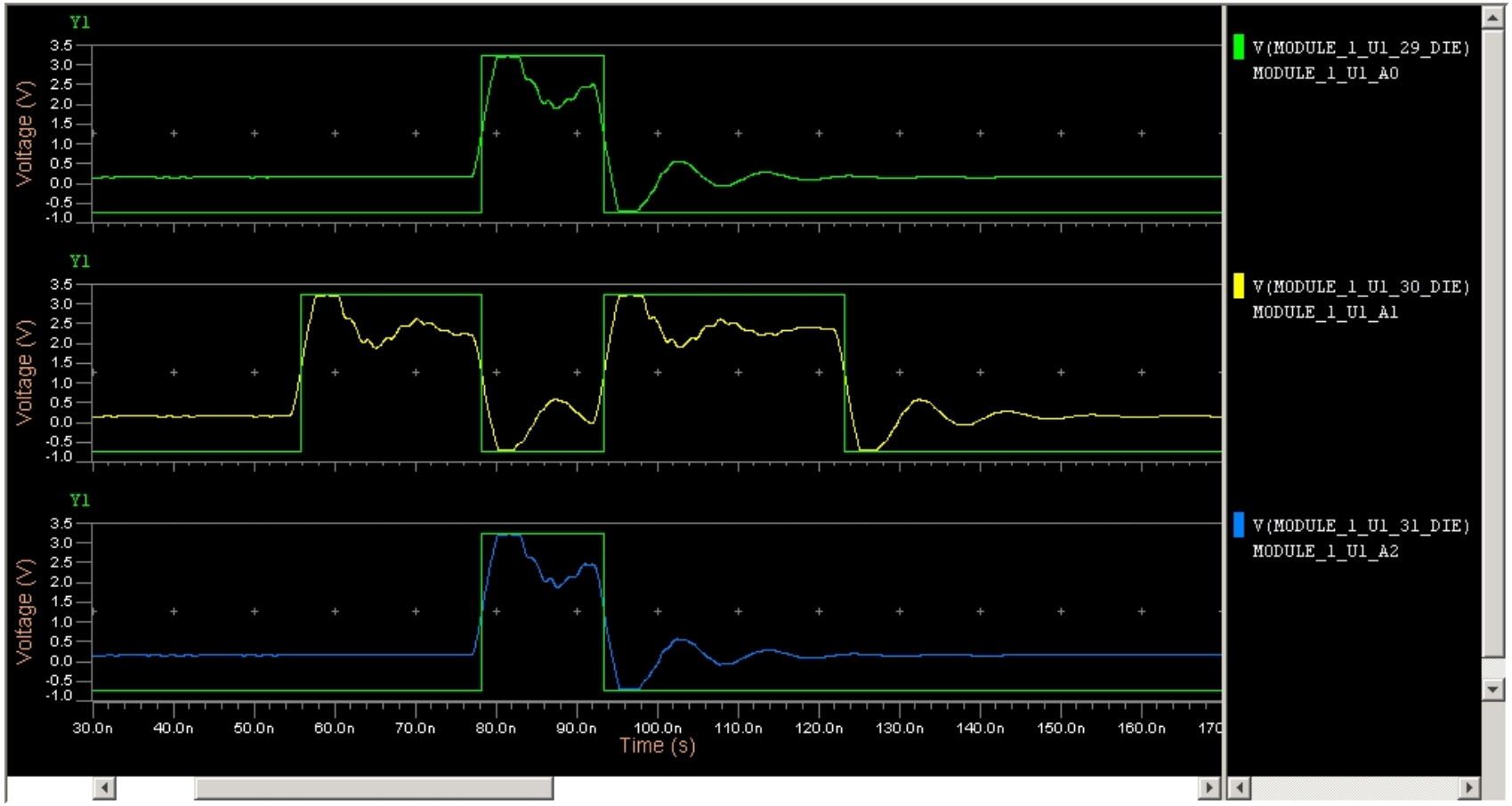
Functional SI Verification Results

- Digital Address and Clock signals at the memory die during a burst write from the chipset



Functional SI Verification Results

- Combined analog and digital Address signals at the memory die during a burst write from the chipset
- Provides a useful visualization of the logical analog equivalent



Future Enhancements

- Exercise all 64 DQ signals in the system (instead of 8)
- Use AMS to analyze slew dependant timing – outputting results on separate signal
- Model DDR2 system including ODT effects
- Include S-parameter models to replace PCB physical information for enhanced crosstalk analysis
- IBIS enhancements:
  - Instantiating a [Model] in a [Circuit Call] statement
  - Corner-specific Parameters passing

Project Contributors

- Gary Pratt, Mentor Graphics
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