Differential System Design and Power Delivery

Vishram S. Pandit and Michael Mirmak

Intel Corp.

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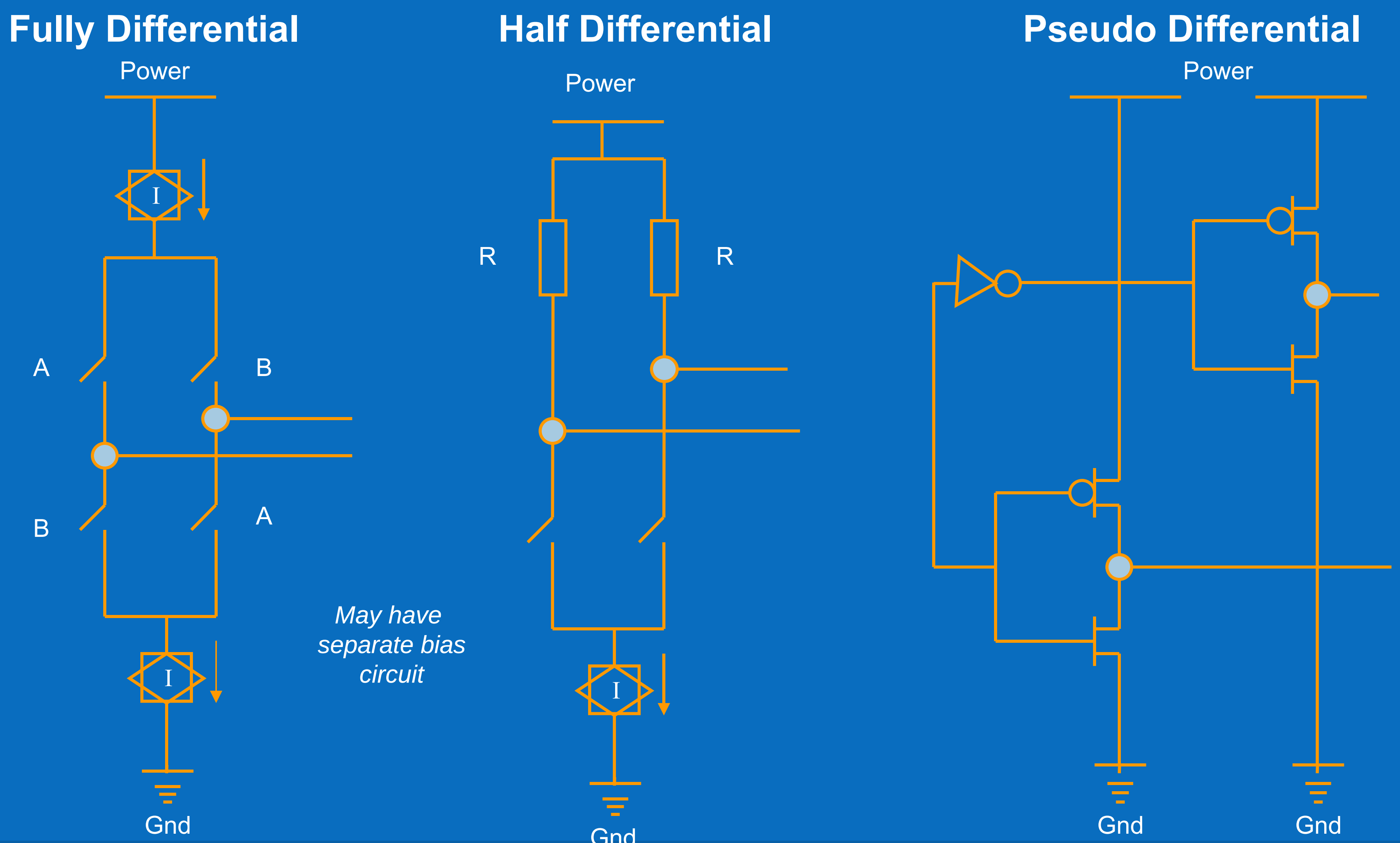
Motivation

- Common assumptions for differential system design...
  - Currents in differential lines are equal and opposite
    ➔ Summation of currents in sig and sig# (differential lines) is zero
  - Current in power equals current in ground at the driver
- These are <u>not</u> valid for all differential systems
- Understanding current behavior is key to proper differential power delivery design
- IBIS* community needs to address this behavior for system simulations

Outline

- Driver and termination types used in differential current analysis
  - "Differential" driver types
    - Fully, Half and Pseudo
  - Termination schemes and current profiles
    - Power, Ground, Between Lines, PI
- Detailed analysis of the popular half differential driver design
  - Currents in
    - Power and ground at driver
    - Differential lines
- Power Delivery (PD) design examples
  - Normal operation vs. driver power on/off
  - IBIS model usage

Typical Differential Driver Types (1)



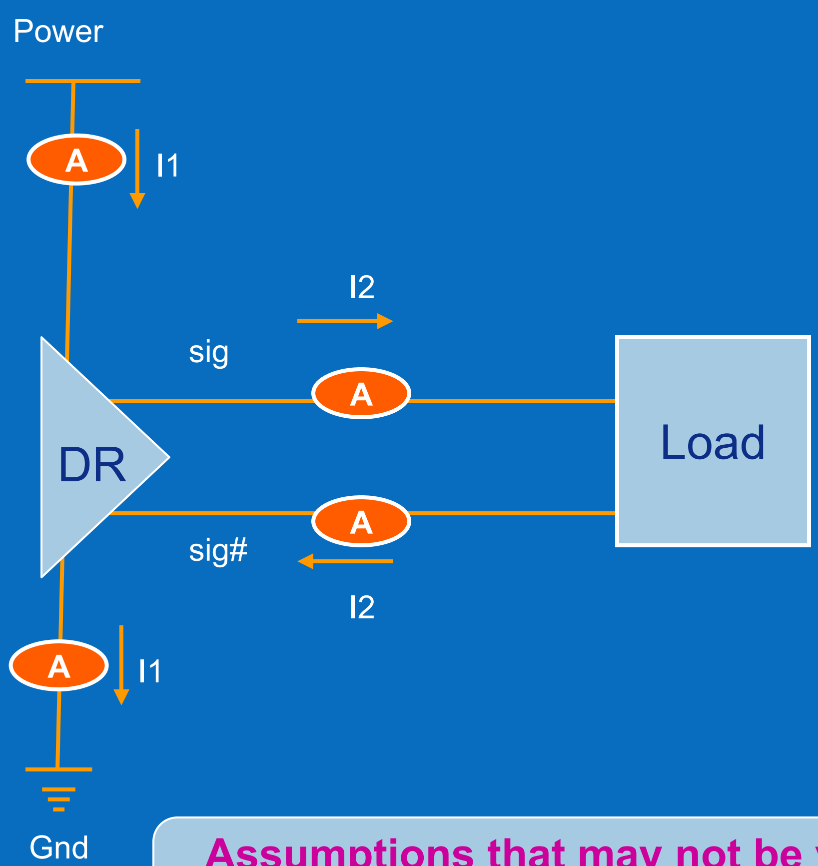
May have separate bias circuit

(1) IBIS Modeling Cookbook for IBIS Ver. 4

Differential Interface Characteristics

	Fully Differential	Half Differential	Pseudo Differential
Driver Terminations	Between sig and sig# (if not at receiver)	Different combinations (e.g., sig and sig# to power, gnd)	Not terminated
Receiver Terminations	Between sig and sig# (If not at driver)	Different combinations (e.g., sig and sig# to power, gnd)	Different combinations (e.g., sig and sig# to power, gnd)
Driver Bias	May be separate bias circuit	Provided through termination	Usually not necessary
Industry Interfaces	LVDS	USB2.0, PCI Express*, SATA, etc.	USB1.1

Typical Expectations for Differential Systems



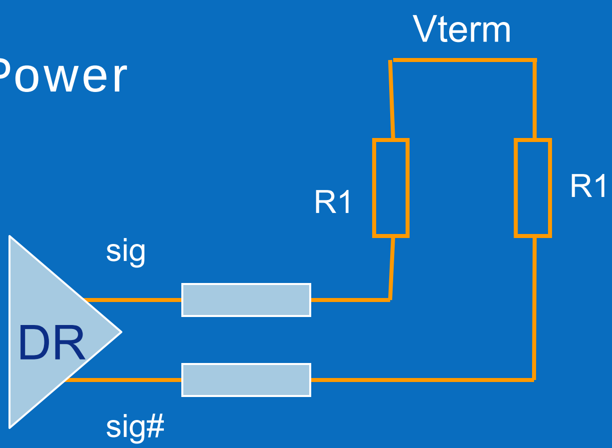
At driver…

- Current in power = current in ground
- Currents in sig + sig# = 0
  - Equal and opposite currents in sig and sig#
- Voltages in sig and sig# = Mirror image with respect to a common reference

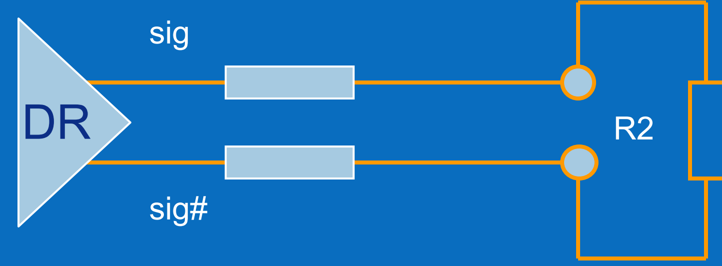
Assumptions that may not be valid for all differential systems:
- **At driver, current in power = current in ground**
- **Summation of currents in sig and sig# = 0**

Termination Schemes for Half Differential

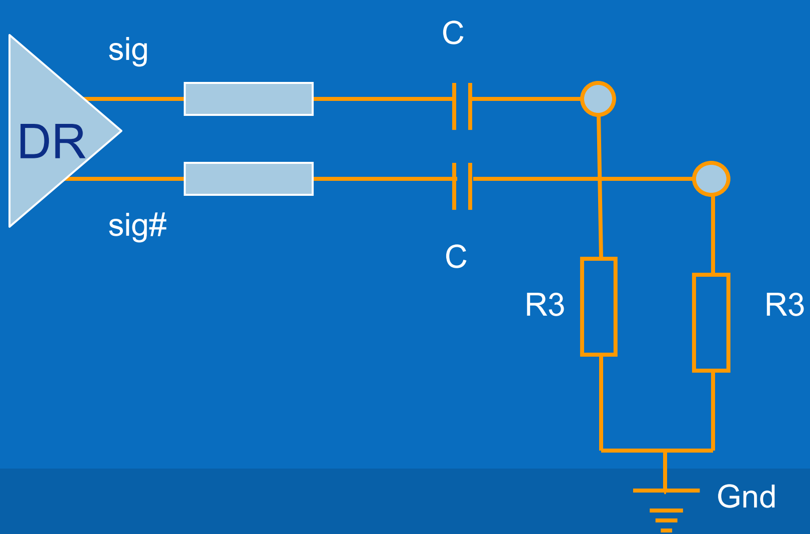
1) Power



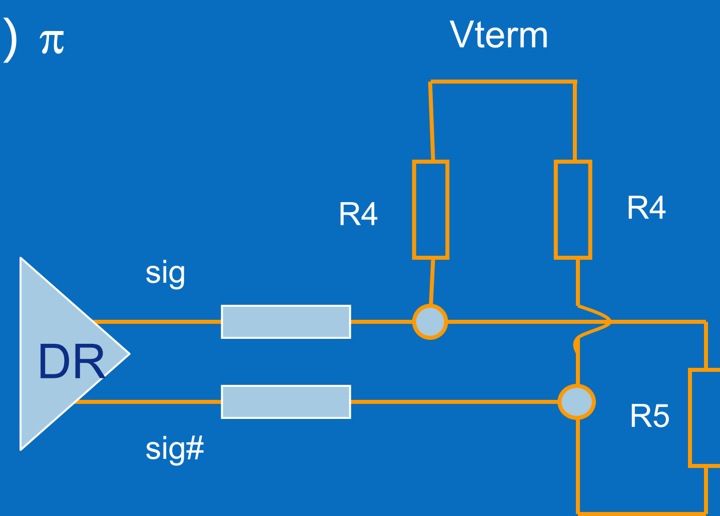
2) Line to line



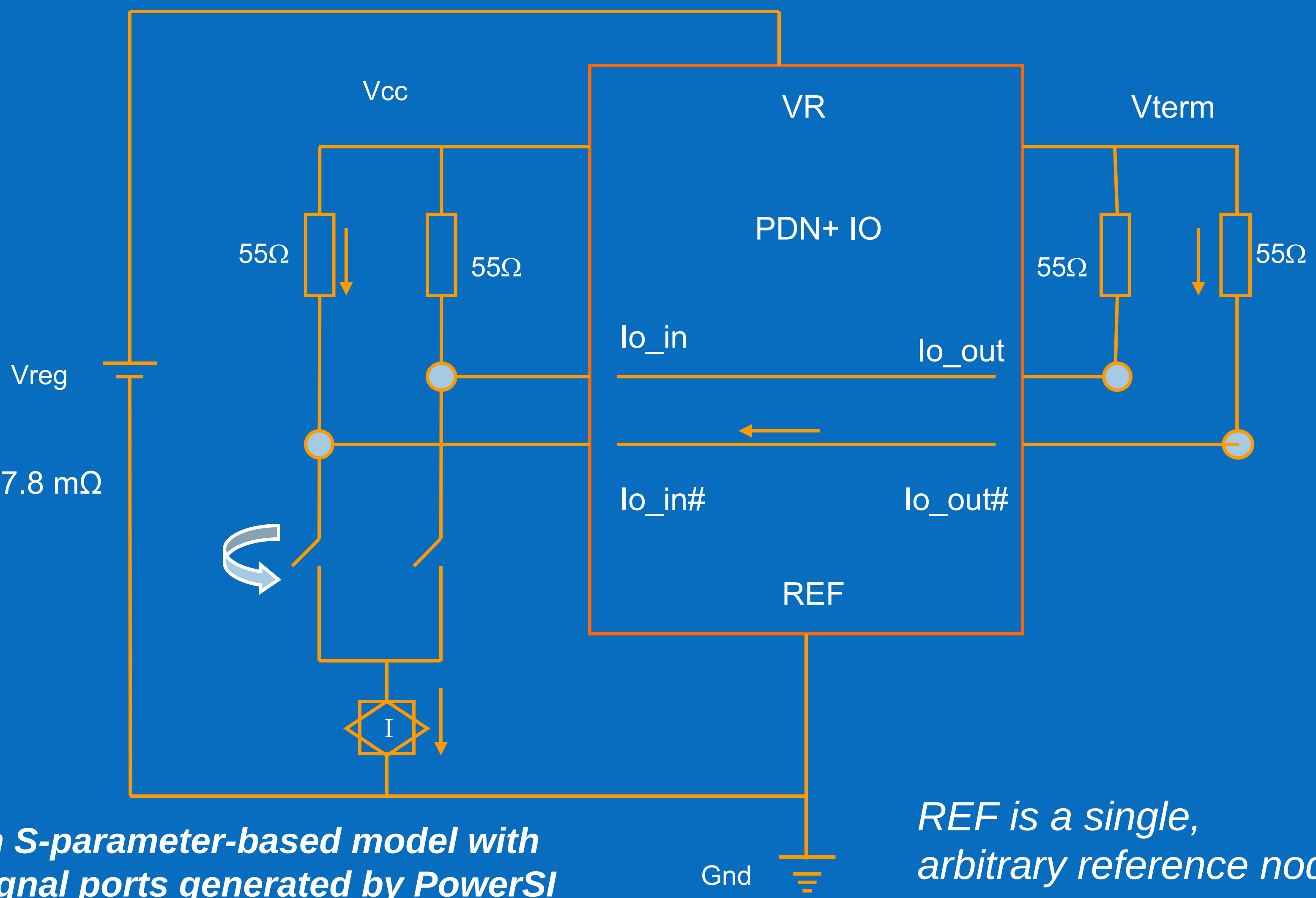
3) Ground



4) π



Termination #1: Power

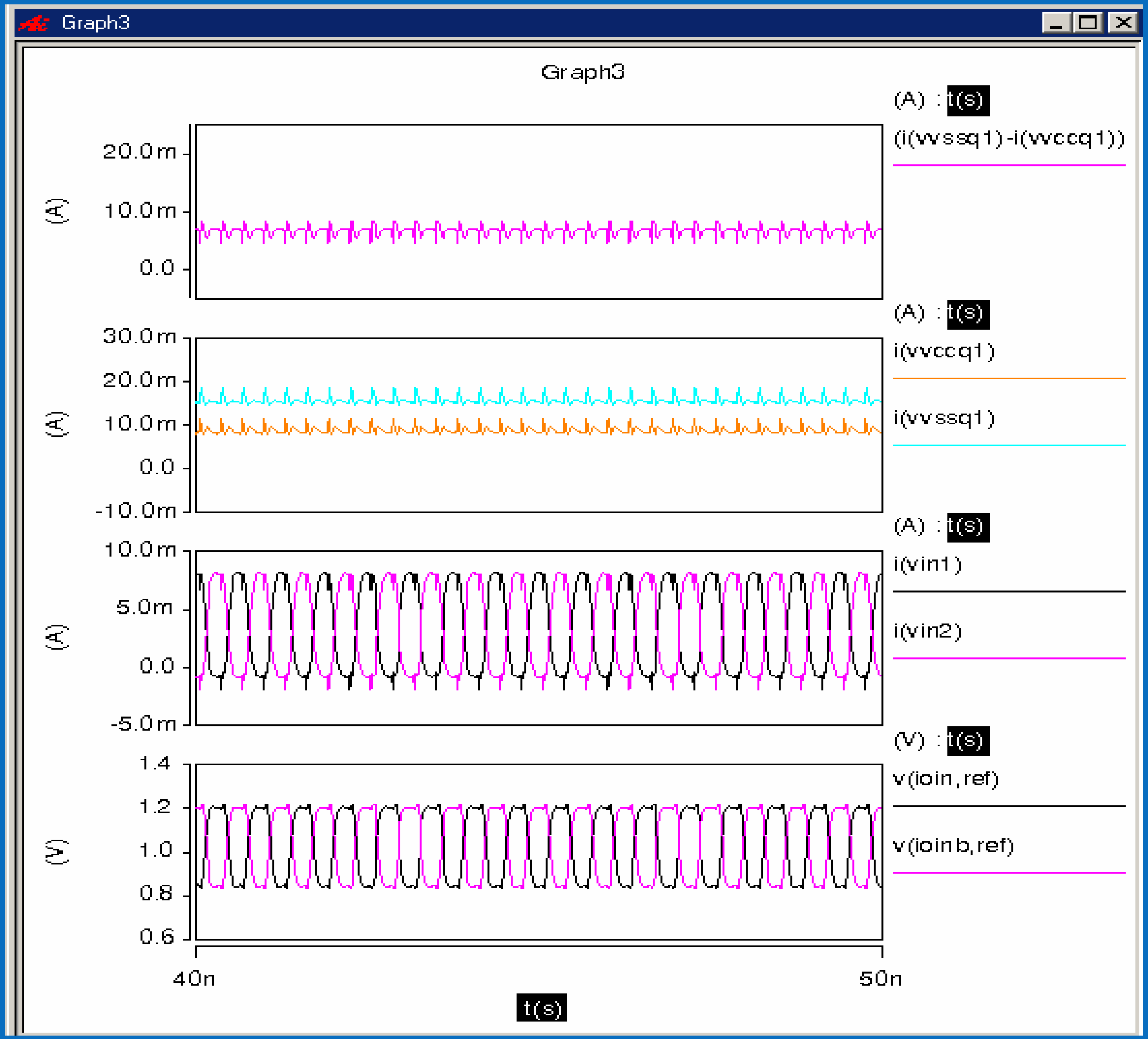


Vreg model:
1.25 V, 5 nH, 7.8 mΩ

Box is an S-parameter-based model with power, signal ports generated by PowerSI

REF is a single, arbitrary reference node

Normal Operating Condition



Difference Current:
Large DC, Small AC

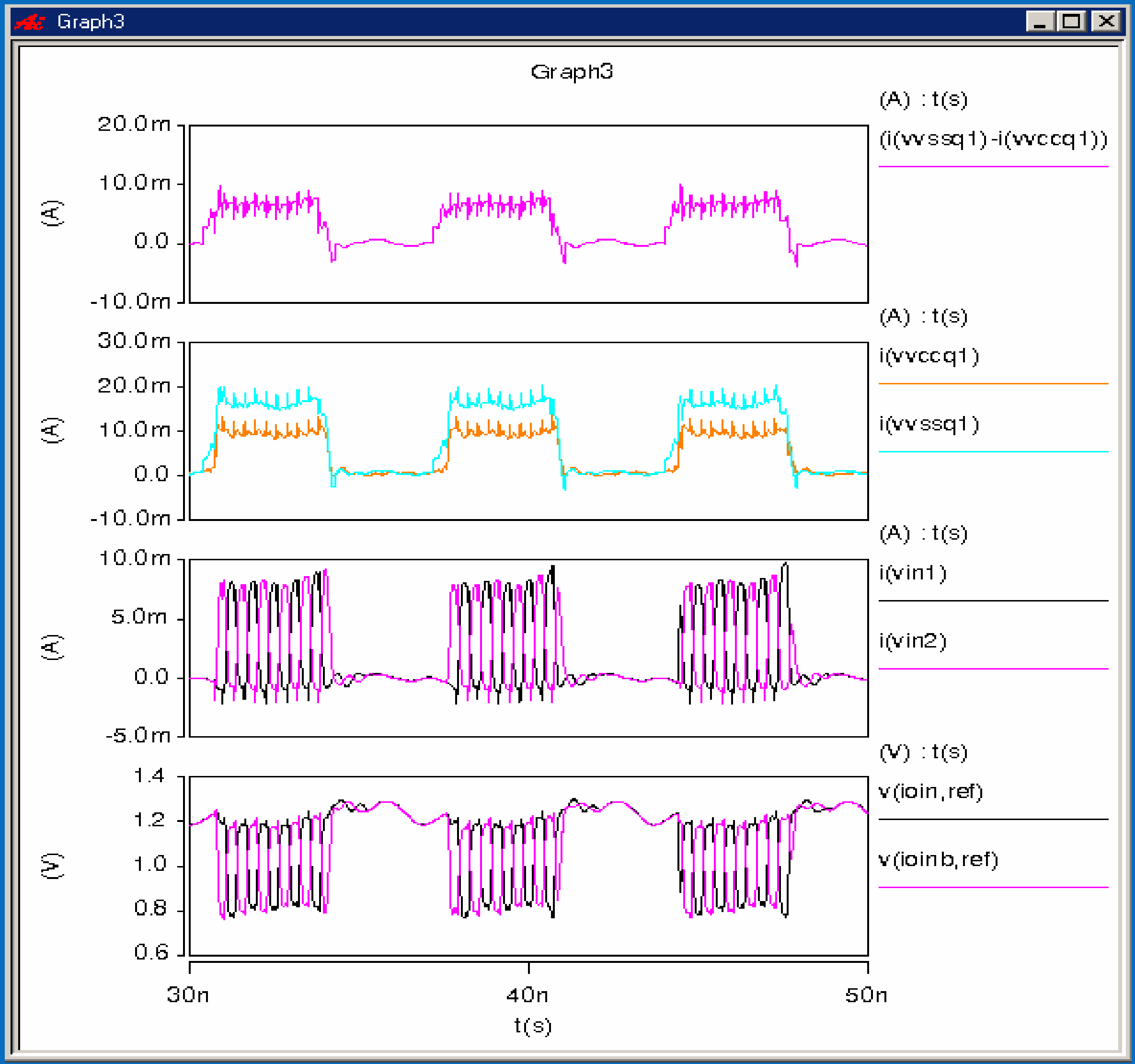
Current (vssq)
≠
Current (vccq)

Currents in Tlines:
Summation ≠ 0 (1)

Voltages in Tlines

(1) Majority of return current is through ground, a net DC return current

Driver Power On / off



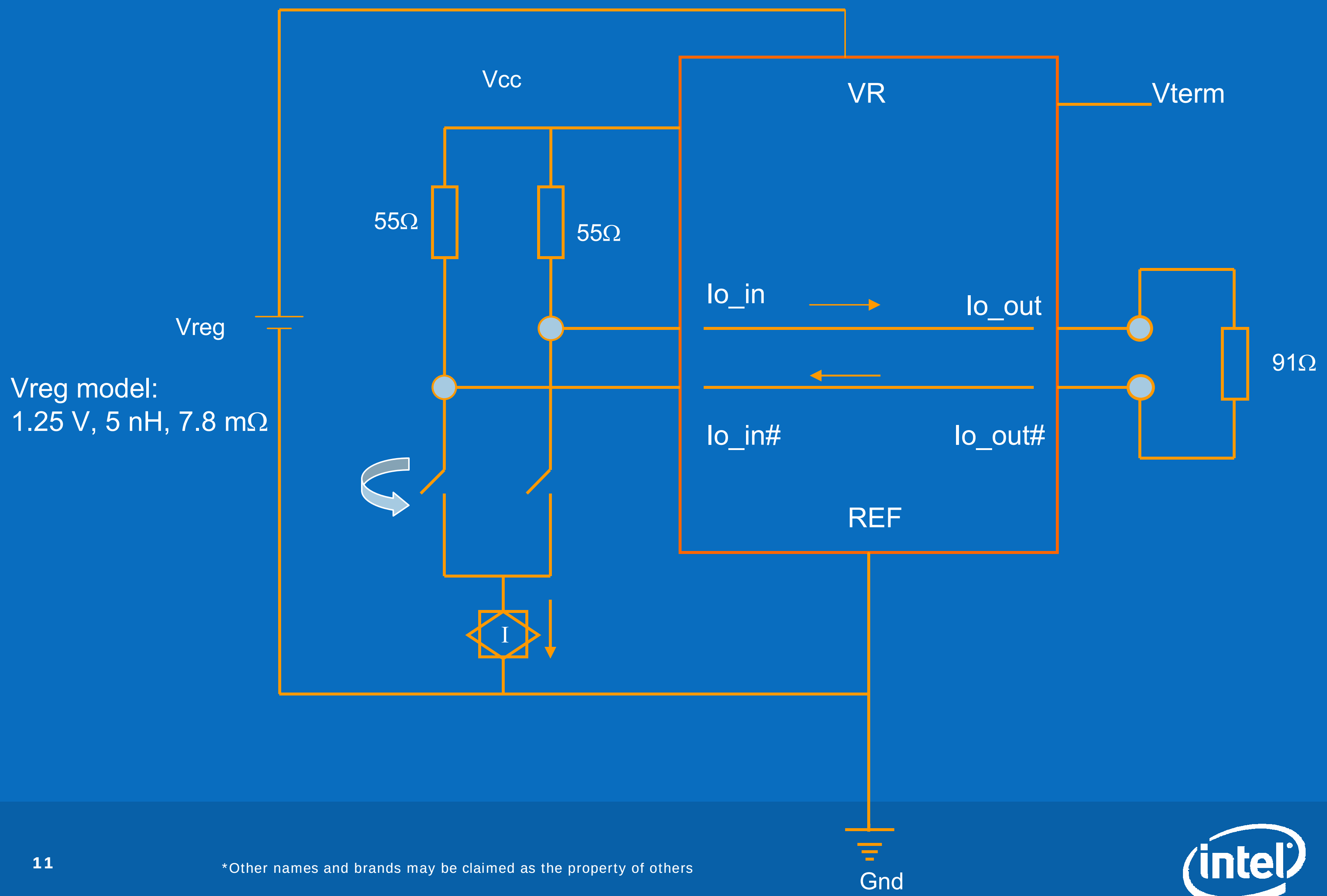
Difference Current :
Large DC & AC

Current (vssq)
≠
Current (vccq)

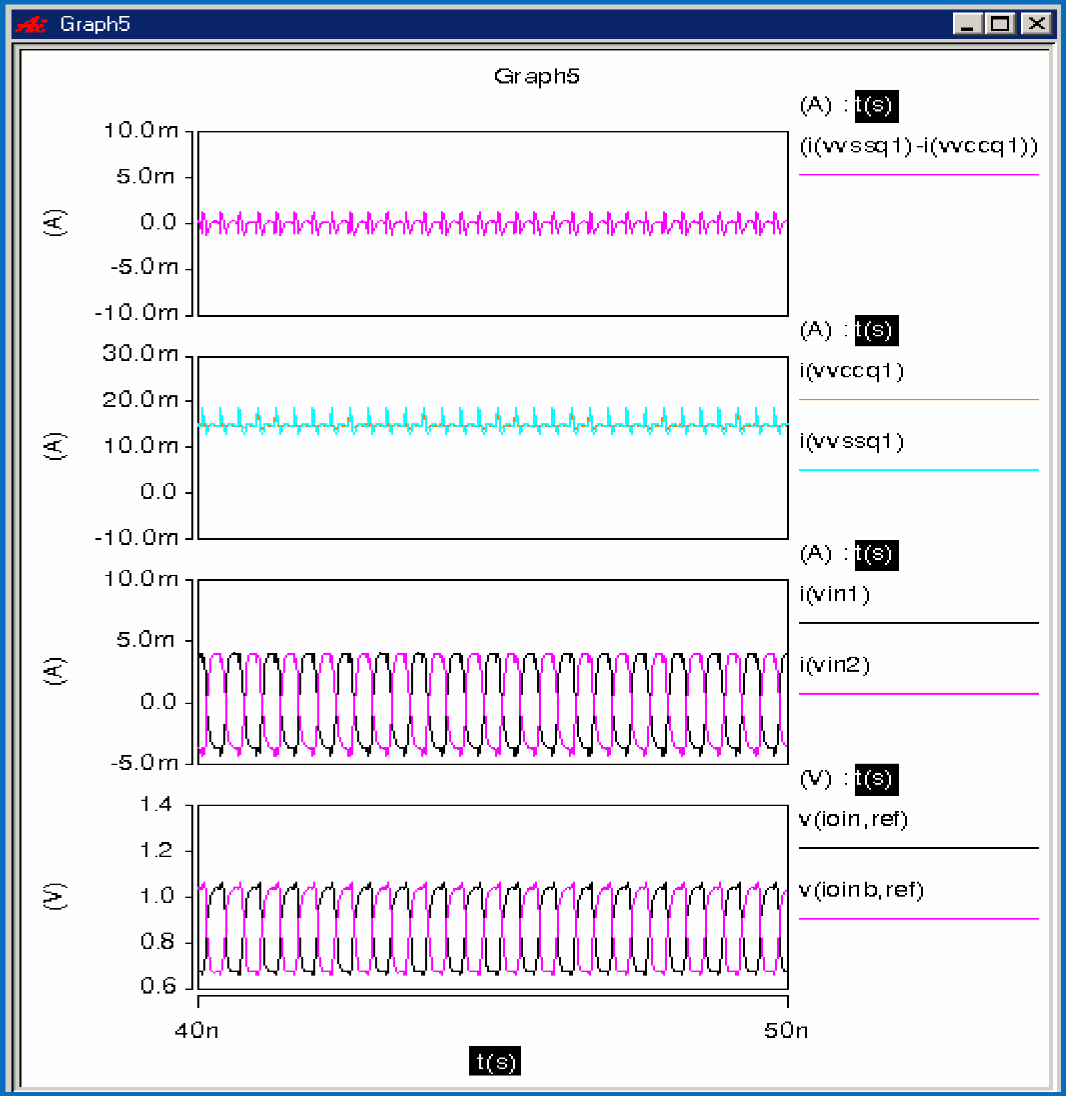
Currents in Tlines:
Summation ≠ 0

Voltages in Tlines

Termination #2: Line to Line



Normal Operating Conditions



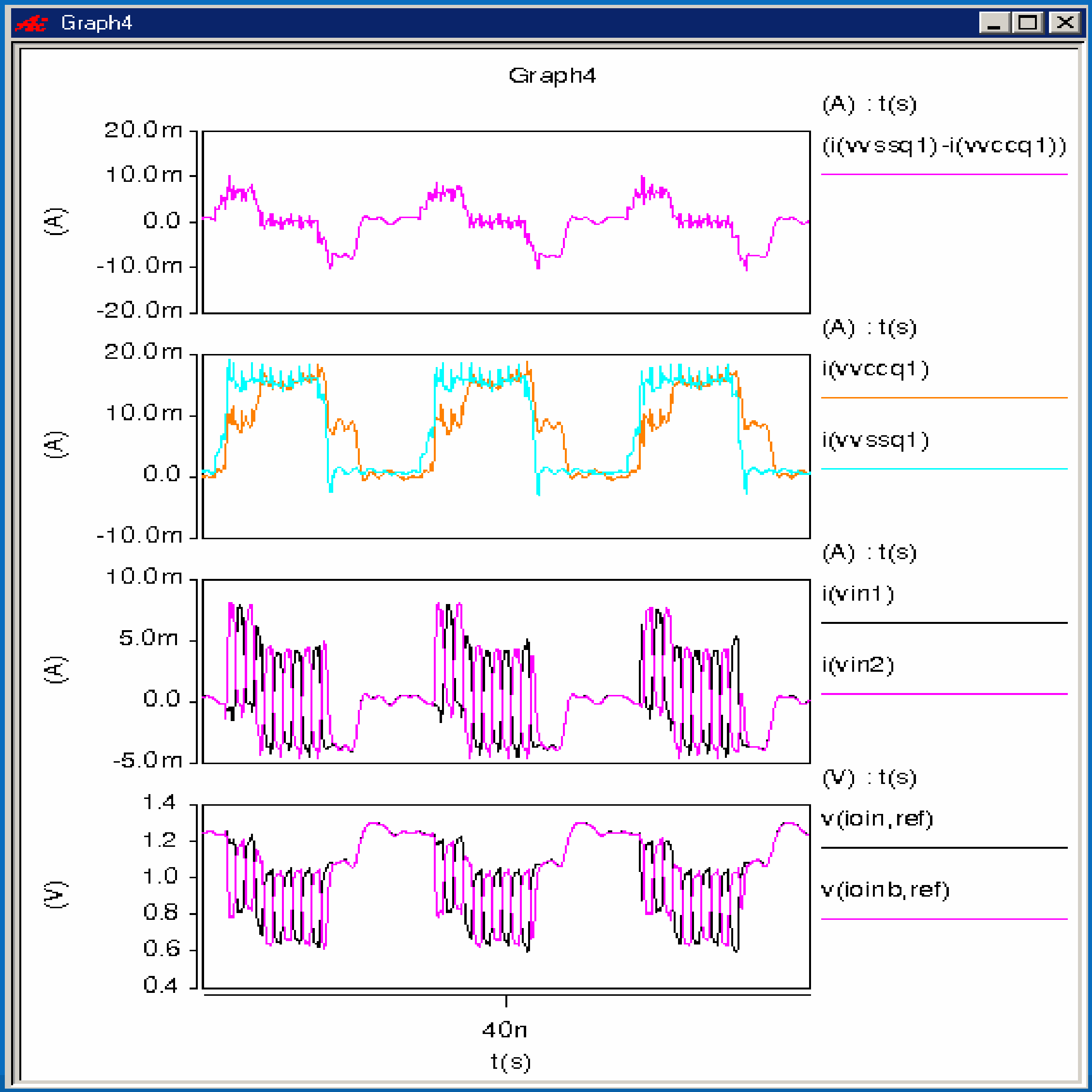
Difference Current:
Small DC & AC

Current (vssq)
=
Current (vccq)

Currents in Tlines:
Equal and opposite;
Summation ≈ 0

Voltages in Tlines

Driver Power On / off



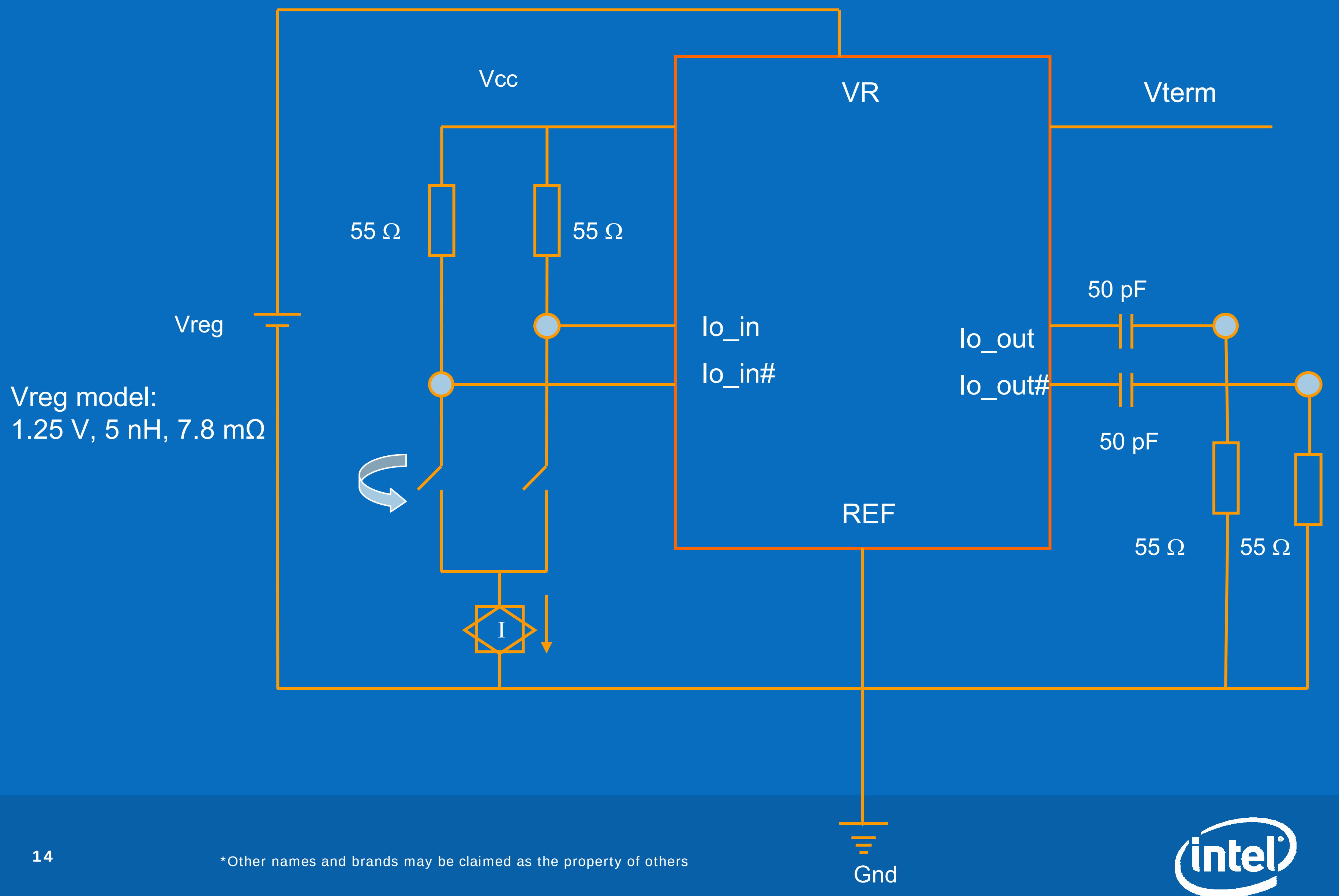
Difference Current:
Large DC & AC

Current (vssq)
≠
Current (vccq)

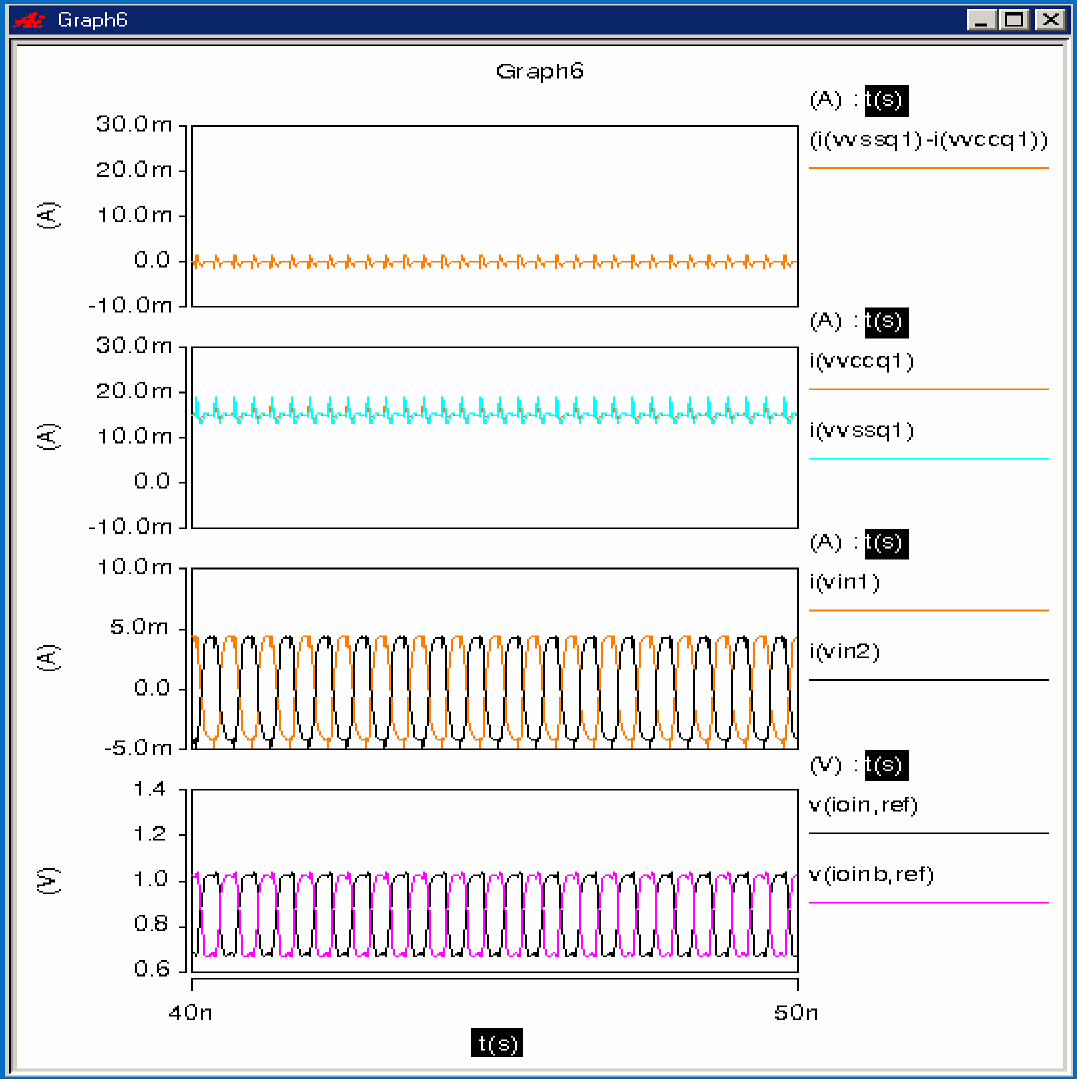
Currents in Tlines:
Summation eventually ≈ 0

Voltages in Tlines with
change in common
reference

Termination #3: Ground



Normal Operating Conditions



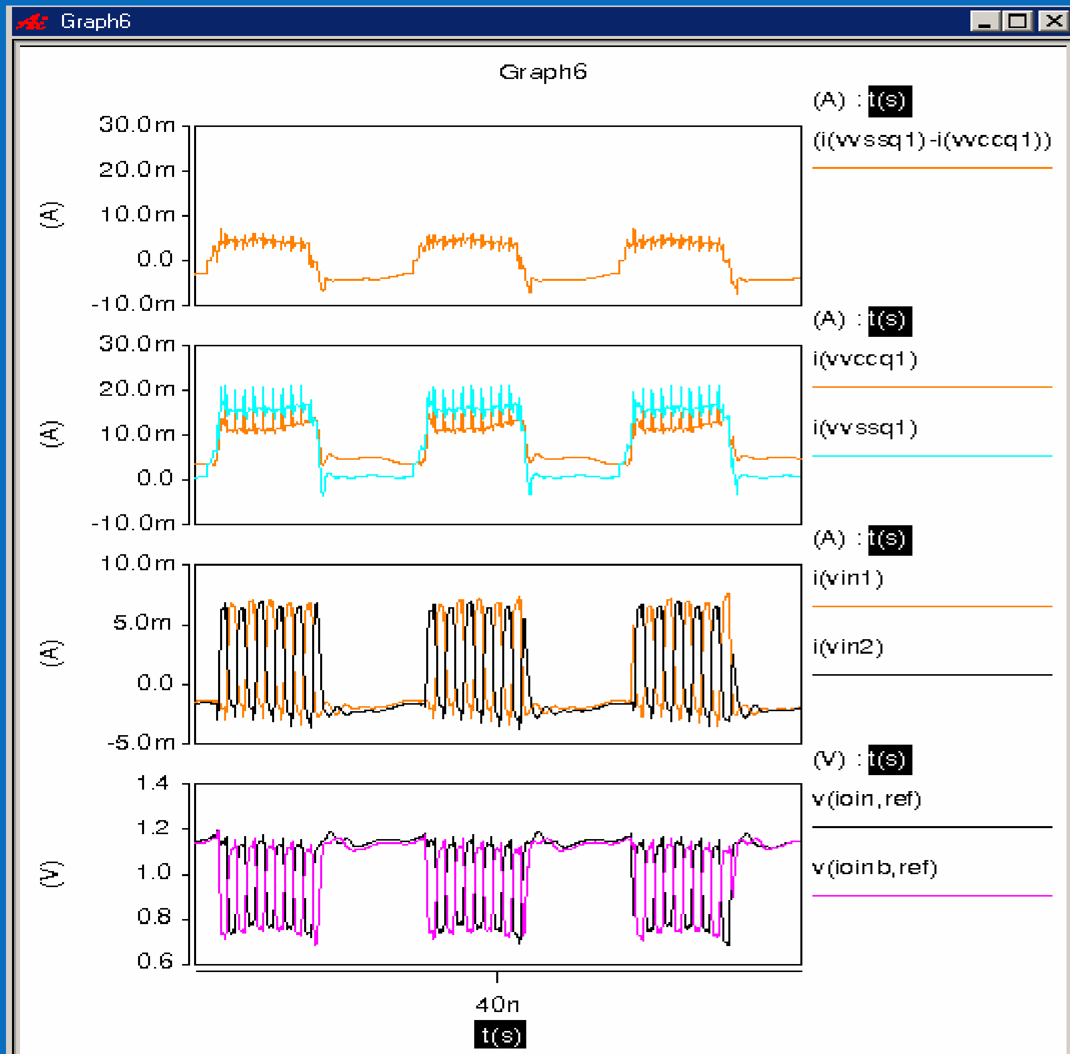
Difference Current:
Small DC & AC

Current (vssq)
=
Current (vccq)

Currents in Tlines:
Equal and opposite;
Summation ≈ 0

Voltages in Tlines

Driver Power On / off



Difference Current: Large DC & AC

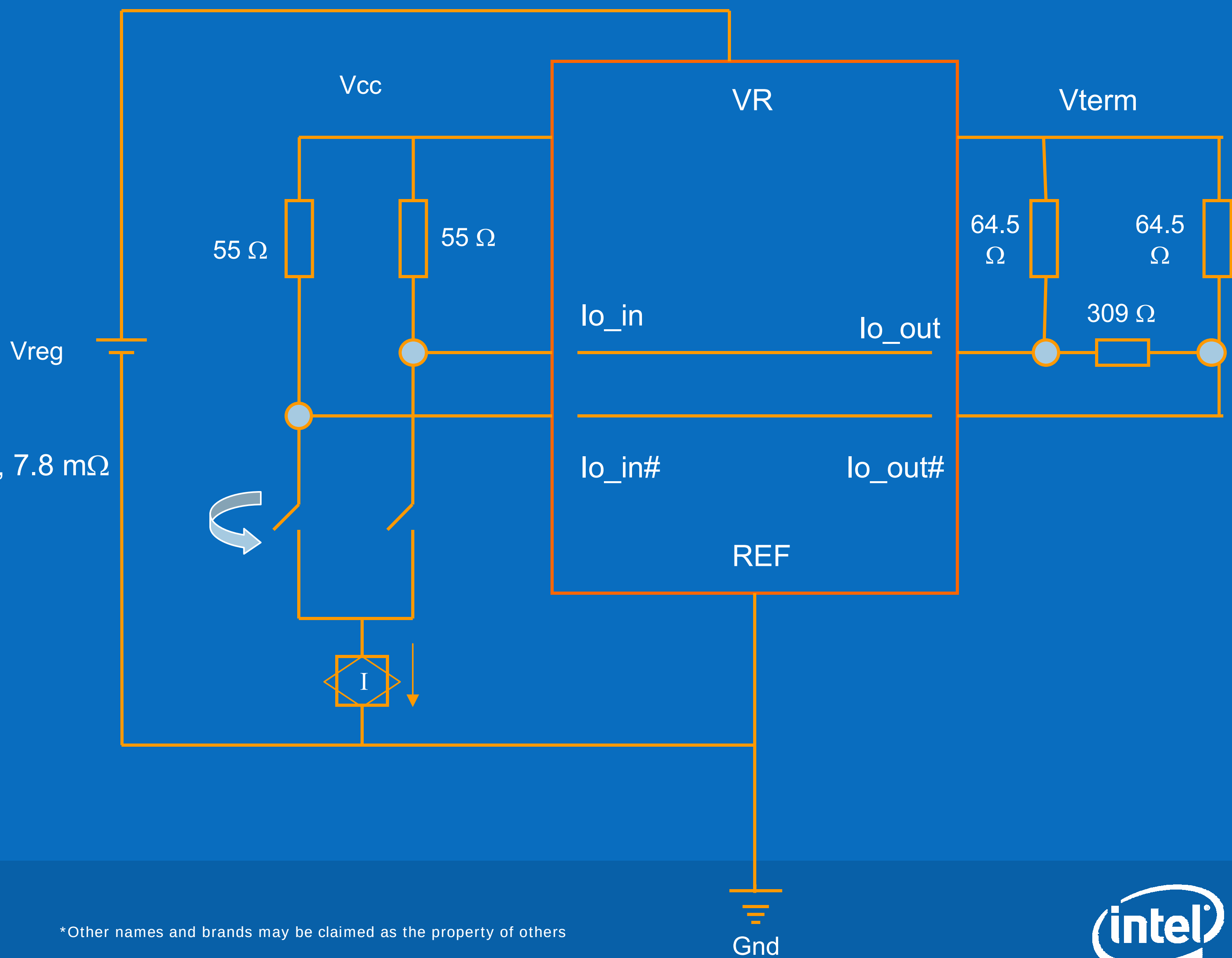
Current (vssq) ≠ Current (vccq) (1)

Currents in Tlines: Summation ≠ 0

Voltages in Tlines

(1) Currents will be equal depending on the cap charge up time, and cap value

Termination #4: π



Vreg model:
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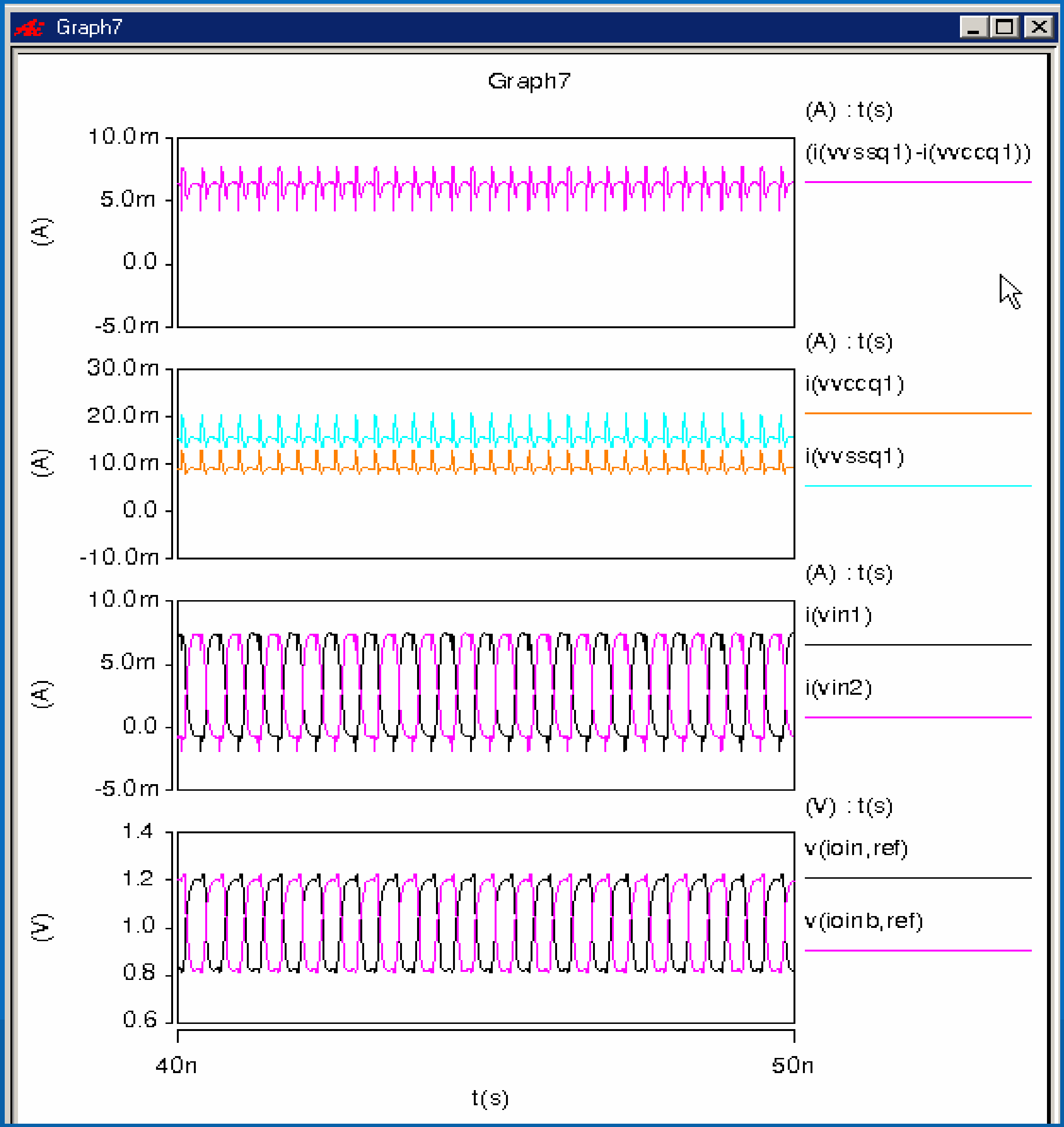
Normal Operating Conditions



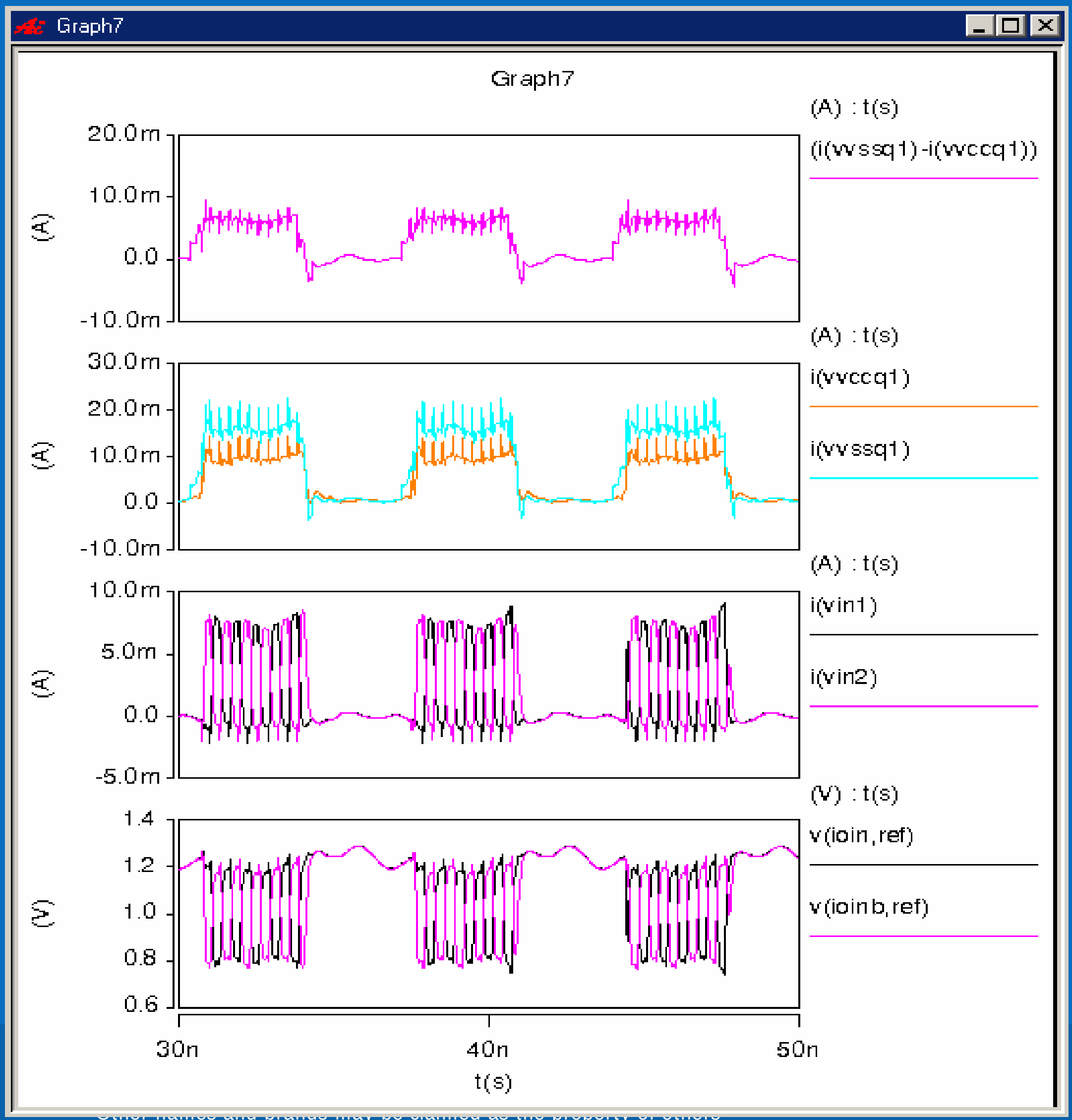
Difference Current:
Large DC, Small AC

Current (vssq)
≠
Current (vccq)

Currents in Tlines:
Summation ≠ 0

Voltages in Tlines

Driver Power On / Off



Difference Current:
Large DC & AC

Current (vssq)
≠
Current (vccq)

Currents in Tlines:
Summation ≠ 0

Voltages in Tlines

Summary of Current Profiles

Comparison of termination schemes

Terminations	I(sig) and I(sig#)	I(Power) and I(Ground) at driver
Power	$I(sig) + I(sig\#) \neq 0$	$I(Power) \neq I(Ground)$
Between lines	$I(sig) + I(sig\#) = 0$	$I(Power) = I(Ground)$
Ground with AC coupling	$I(sig) + I(sig\#) \neq 0$ (0 after charge up of cap)	$I(Power) \neq I(Ground)$ (equal after charge-up of cap)
PI	$I(sig) + I(sig\#) \neq 0$	$I(Power) \neq I(Ground)$

Significance of Current Profiles

- I(sig) and I(sig#) at driver
  - For half differential driver, the currents in the lines may or may not be equal and opposite.
  - In normal operation, when I(sig) $\neq$ I(sig#)
    - AC amplitude may be equal but centered around some DC value
    - Net non-zero DC return current
  - In the driver on/off scenario, summation of I(sig) and (sig#) may result in net DC+AC current

- I(power) and I(ground) at driver
  - In normal operation , when I(power) $\neq$ I(ground), some DC shift is present
    - AC current may be equal
  - Consider these currents in the driver on/off scenario
    - di/dt will be different for power and ground in this case

Observations re Energy in PDN and Noise

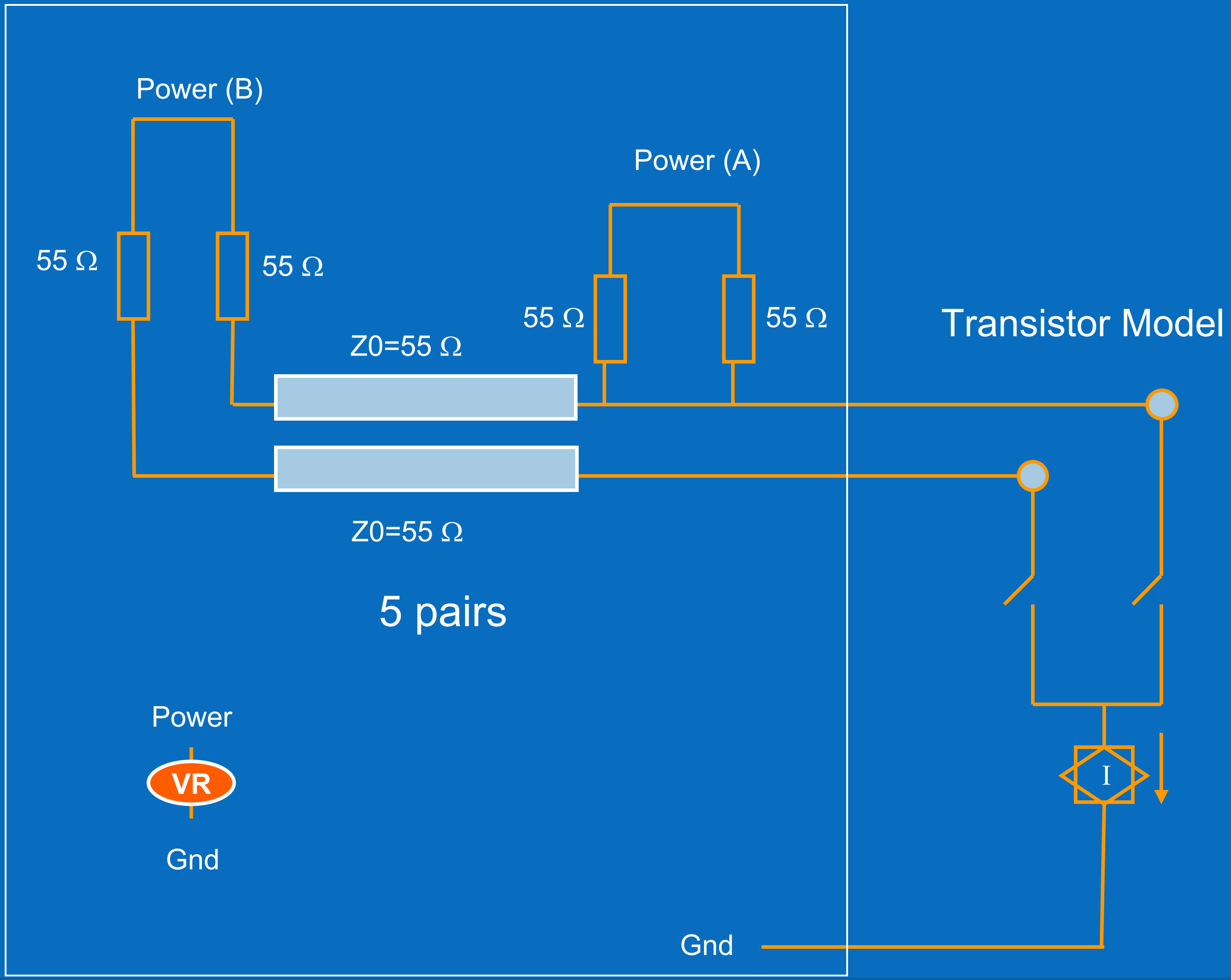
- Half differential driver designs utilize a current source
- High-frequency energy in Power Delivery Network (PDN) is small compared to that in driver power on/off scenario
- Power delivery solution space (die decoupling, package and board) depends on di/dt
- Noise produced in normal operating condition is smaller than that for driver power on/off condition
- Worst case occurs when driver power on/off cycles occur at resonant frequency of the PDN

Modeling Differential Systems

- Different modeling approaches for half differential driver
  - Transistor models
  - Icc(t) method
  - IBIS models

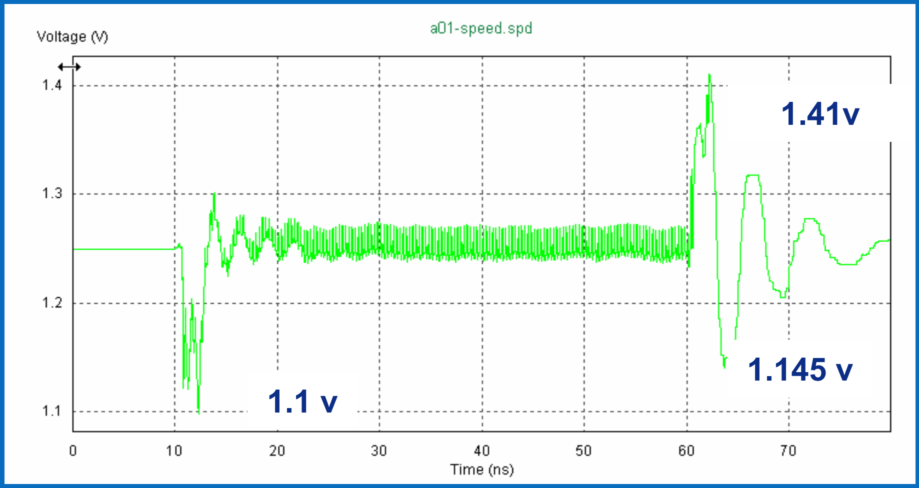
- In a differential system, each modeling approach needs to address
  - Termination schemes' dependence on system currents
    - Currents in power and ground
    - Currents in sig and sig#
  - The solution space is dependent on the currents

Transistor Model: SPEED2000* example



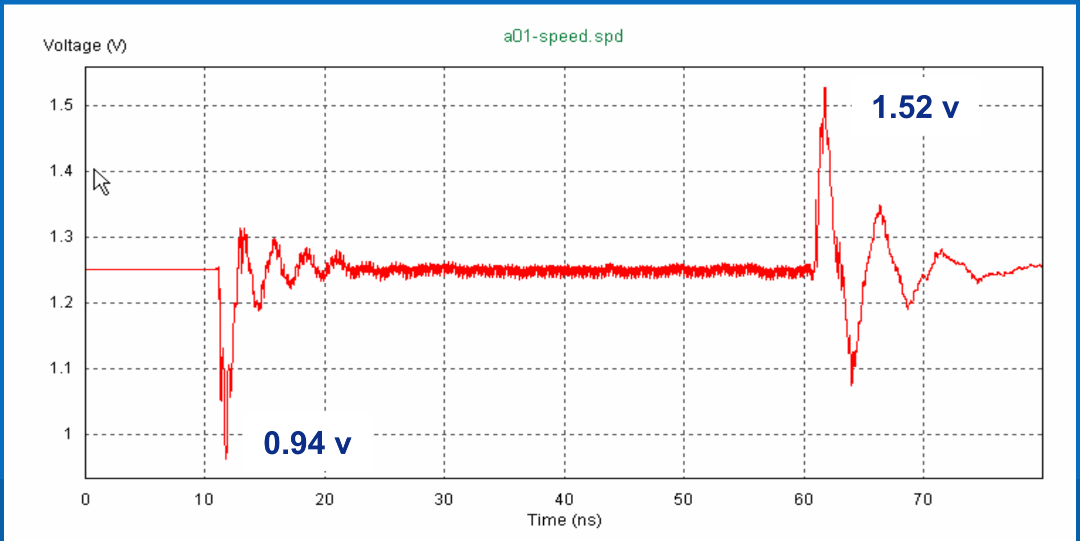
Box represents
a planar 3-D model;
Power and Gnd are
not single nodes

Sigrity SPEED2000* + Synopsys HSPICE* In Co-simulation



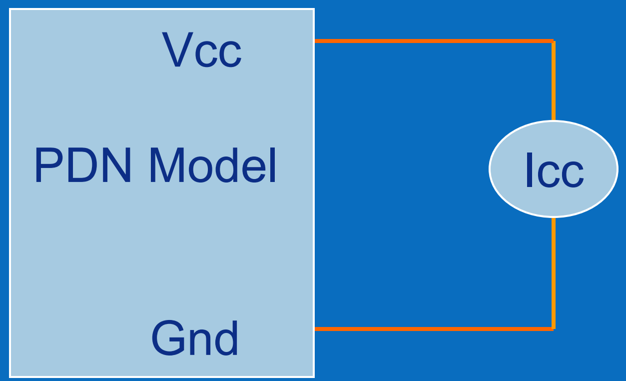
Noise at driver (A)

Noise at termination (B)



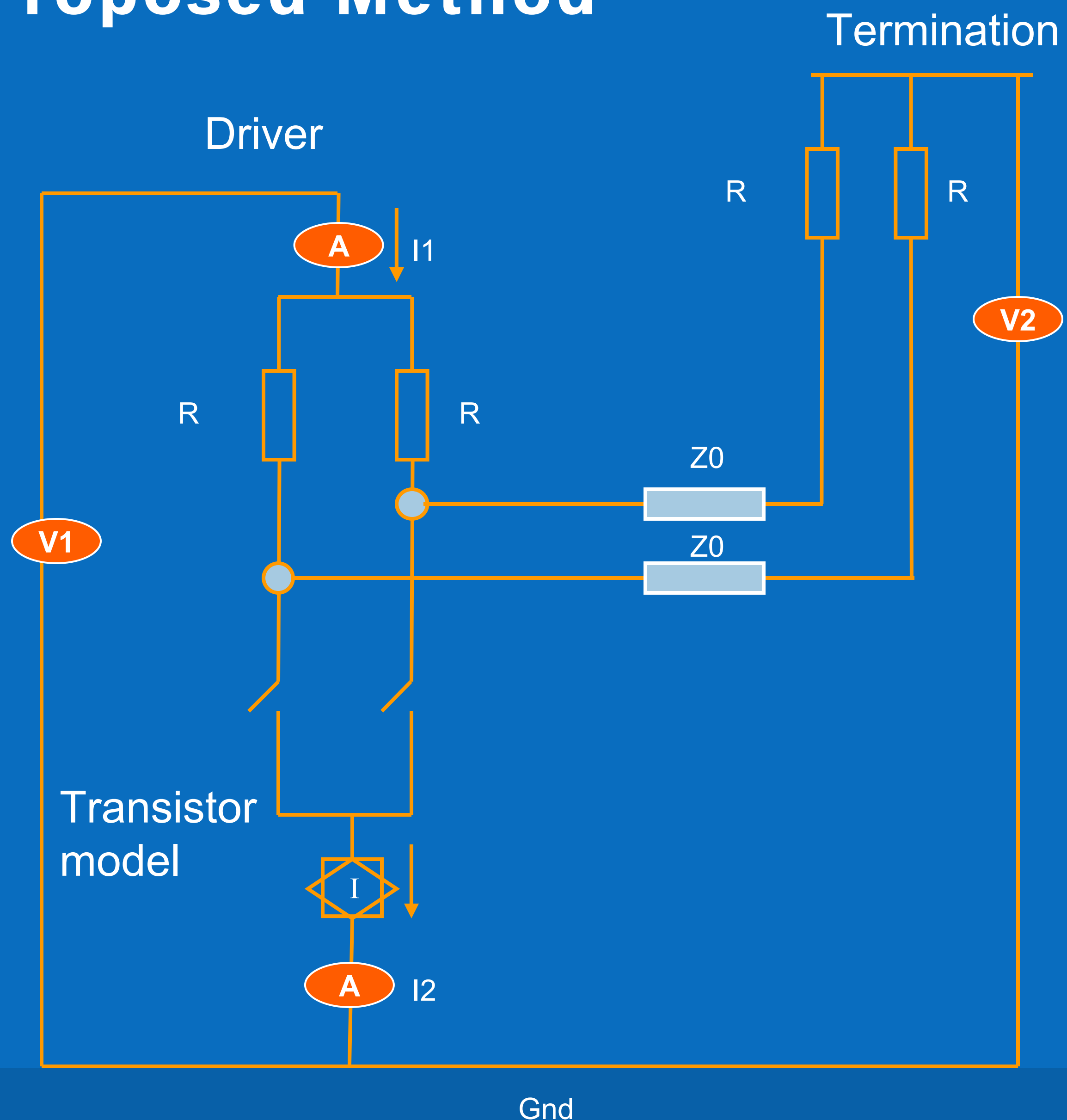
Driver power on/off event

Contemporary Icc(t) methods



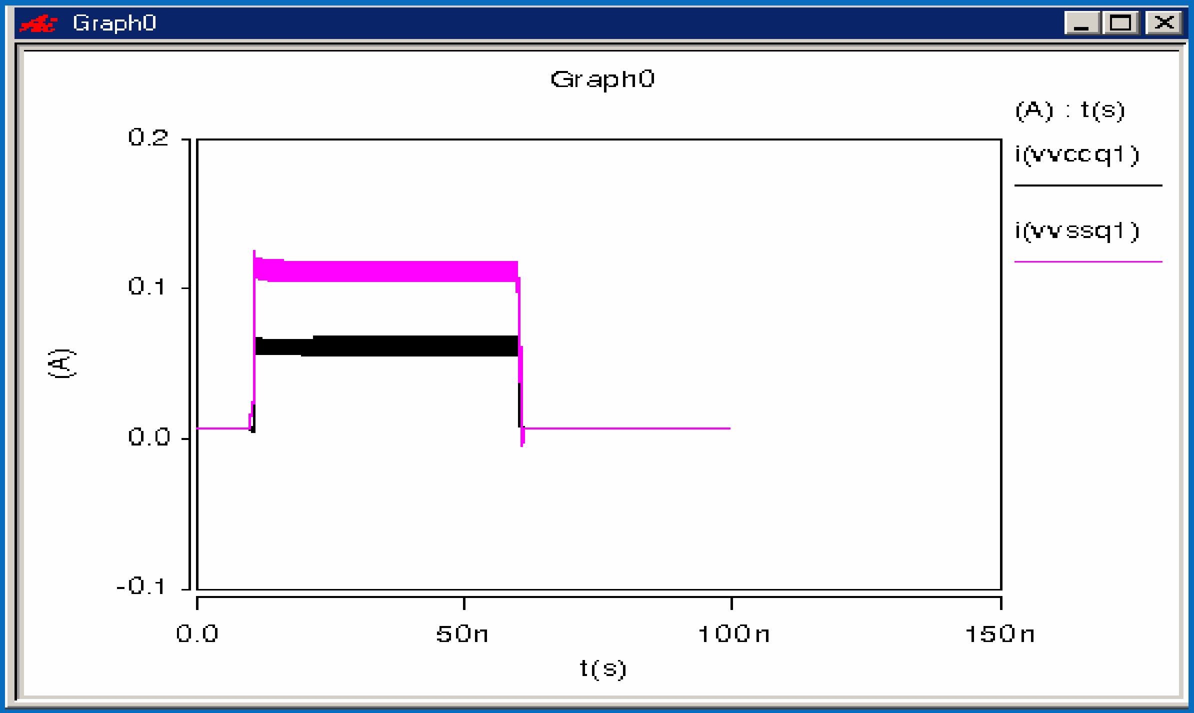
- Typical Icc(t) approach assumes equal currents in power and ground
- Termination schemes MATTER when computing Icc(t)
- Currents in power and ground may or may not be equal
- *Monitoring Ivcc and Ivss a must*

Icc(t): Proposed Method



Icc(t) for 5 Buffers

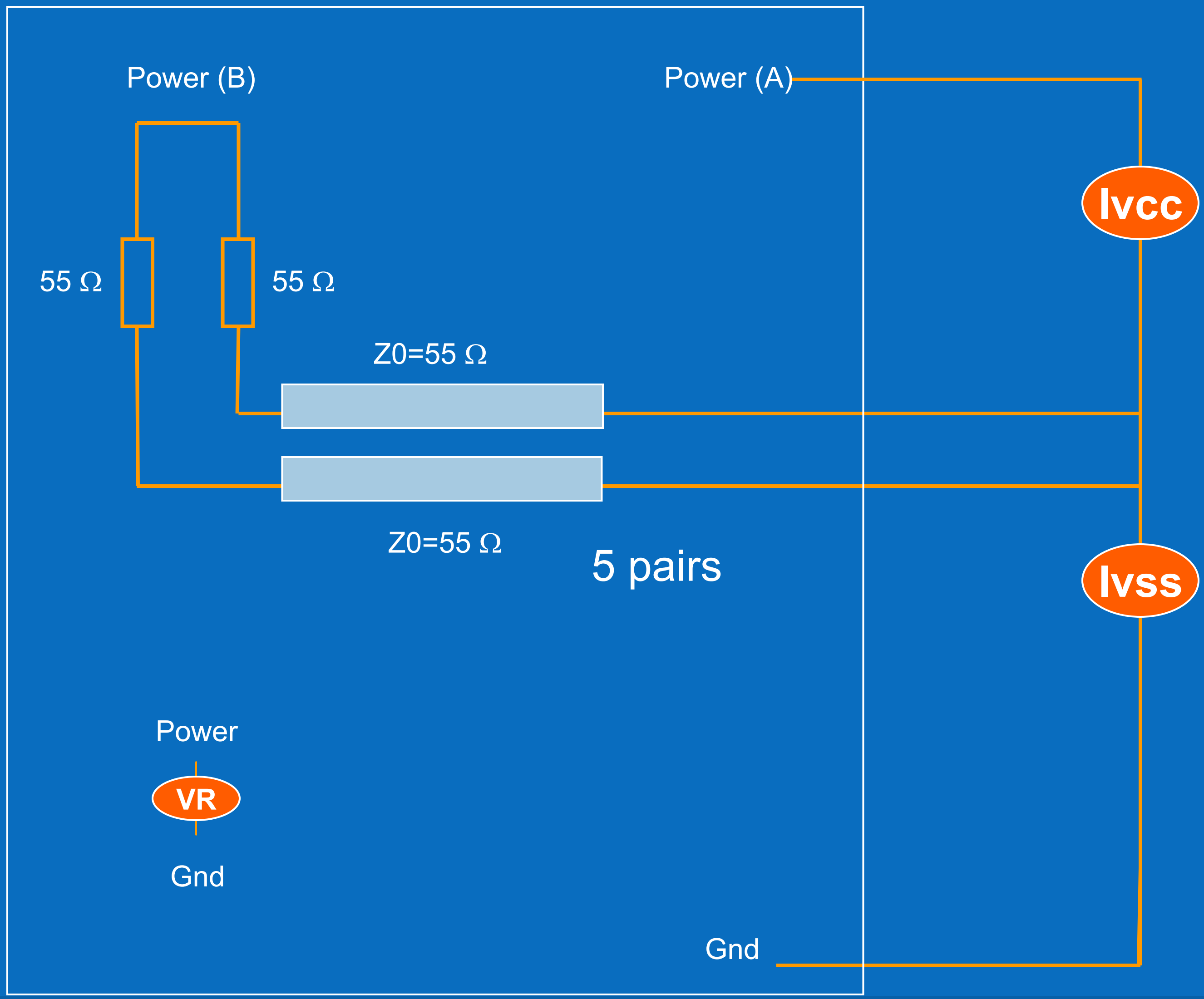
Driver power on/off event



Current in power

Current in ground

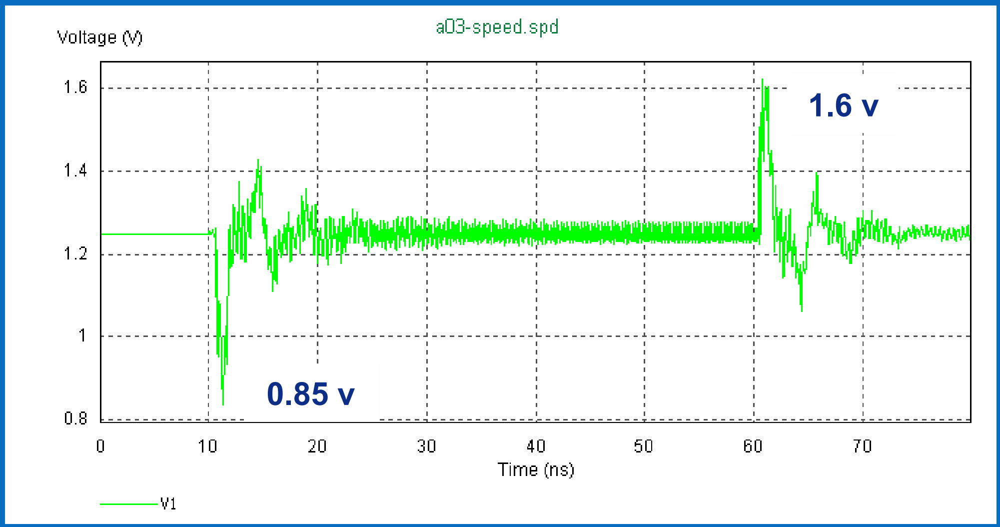
Icc(t) Model: SPEED2000* example



Box represents a planar 3-D model; Power and Gnd are not single nodes

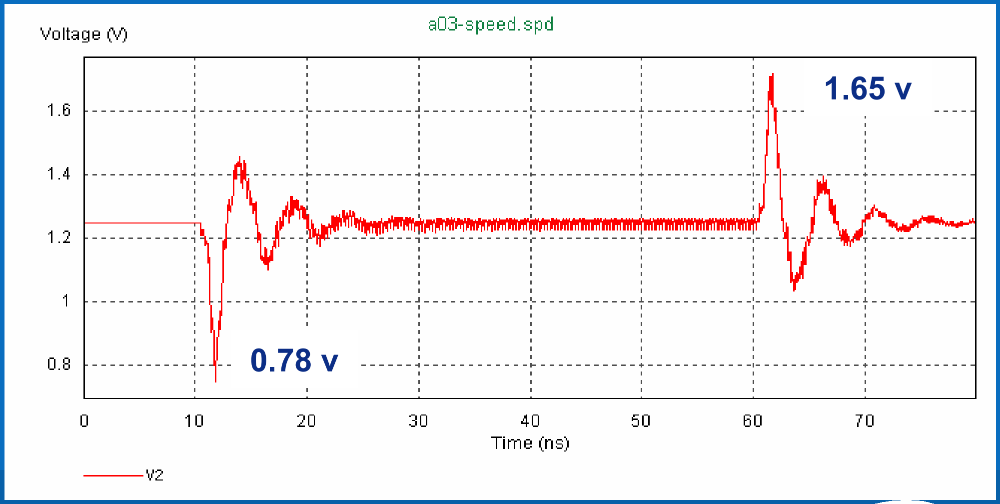
Ivcc, Ivss under Sigrity SPEED2000*

Noise at source (A)

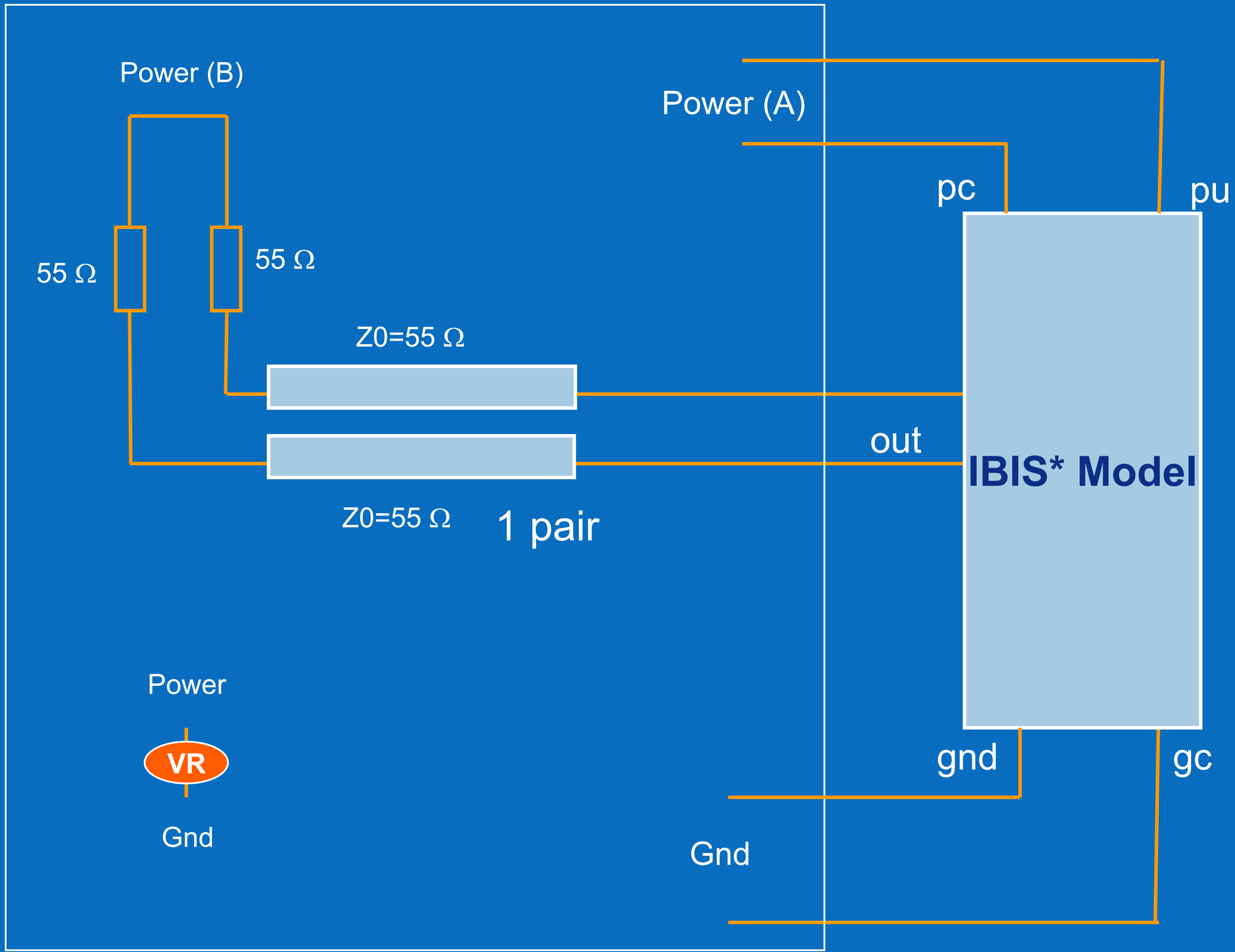


Noise at termination (B)

Driver power on/off event



IBIS model: Sigrity SPEED2000* Example



Box represents
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Power and Gnd are
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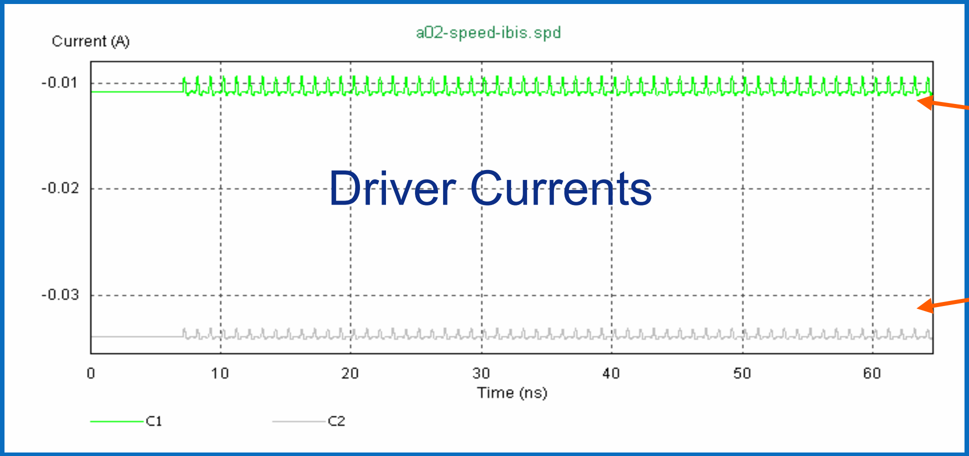
Normal Operation

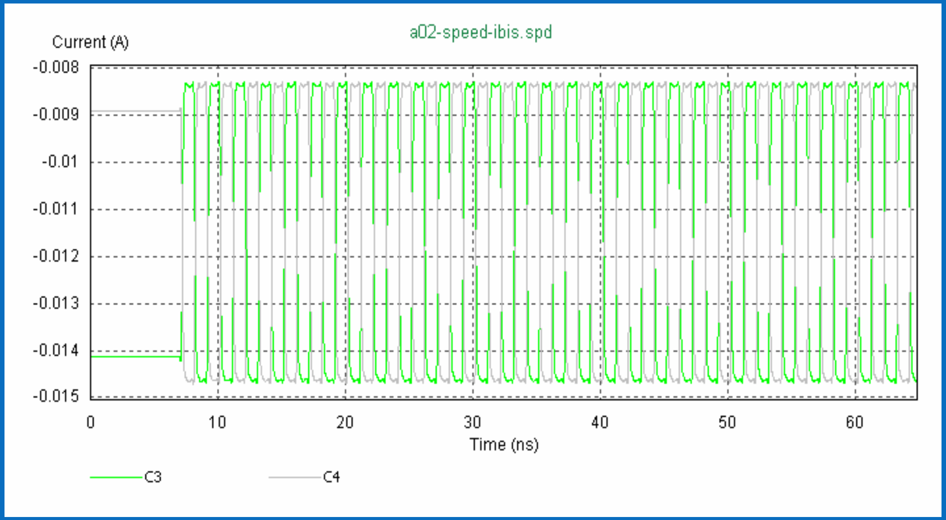


Current in Power

≠

Current in Ground

Summation of currents in transmission lines ≠ 0



Driver Power On/Off

- For optimum power delivery system design, driver power on/off behavior of the buffer must be analyzed

- For IBIS*, the output only model cannot be switched off
  - Removing power from the buffer may not be accurate

- I/O model can be powered off through the Enable control
  - Implementation is tool-dependent

*Other names and brands may be claimed as the property of others

Conclusions

- For half differential system
  - Currents in differential lines are <u>not</u> always equal and opposite
  - Currents in power and ground are <u>not</u> always equal
  - Termination schemes play an important role

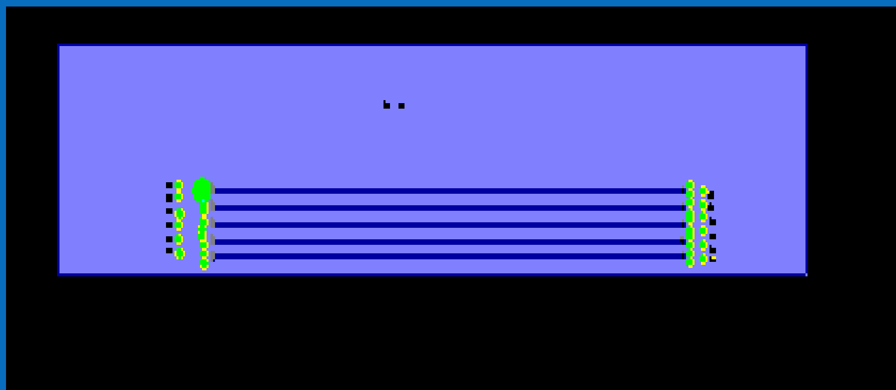
- For differential systems, power delivery design must consider
  - Normal operation vs. power on/off events
  - Decoupling solutions to mitigate worst case operating conditions

- Different modeling approaches need to accommodate this behavior

- Key questions for industry
  - Do today's tools support driver power on/off event simulations?
  - Can IBIS* be used reliably for driver power on/off analyses?
  - Does BIRD95 include all the data needed for this kind of analysis?

Backup

Geometry and Stackup



Trace width: 5 mils
Trace spacing: 7 mils

Stackup

Layer Icon	Layer Name	Thickness(mil)	Conductivity(S/m)	Color	TraceWidth(mil)	Shape Name	Permittivity	Loss Tangent
	Medium_AIR	7.4803e-001					3.4000	0.0000
	Signal01	2.0984e+000	5.8000e+007		3.9370e+000			
	Medium06	4.2520e+000					3.9000	0.0000
	Plane_MB_VCC	1.4016e+000	5.8000e+007			Shape_MBVCC		
	Medium_MB_CORE	3.9728e+001					4.0000	0.0200
	Plane_MB_VSS	1.4016e+000	5.8000e+007			ShapeMBVSS		
	Medium07	4.2520e+000					3.9000	0.0000
	Signal02	2.0984e+000	5.8000e+007		3.9370e+000			
	Medium05	7.4803e-001					3.4000	0.0000

Total Thickness: 5.6728e+001 mil

Unit: mil

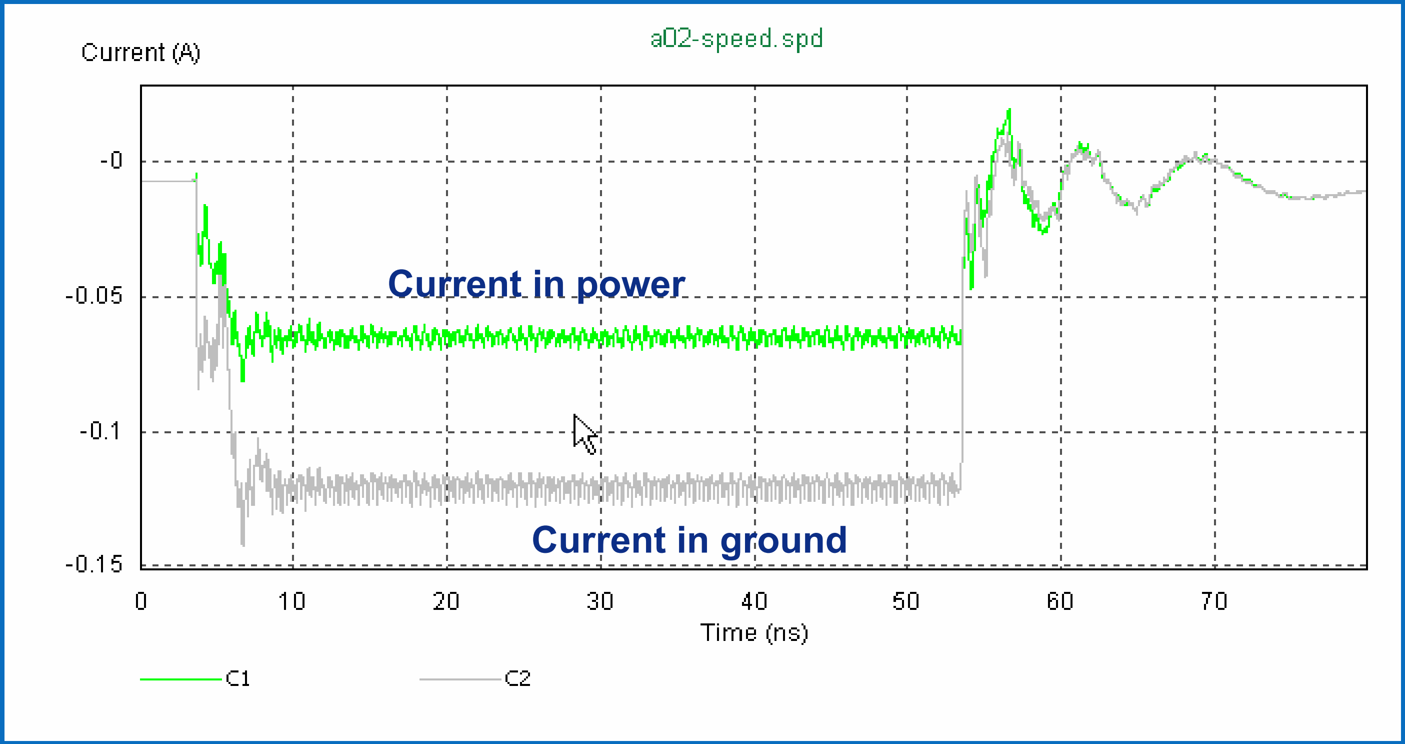
View Material

Icc verification with co-simulator

Co-simulator: Sigrity SPEED2000* + Synopsys HSPICE*

Current flow at drivers

Driver on/off event



5 Diff Drivers are used

*Other names and brands may be claimed as the property of others