Fiberhome Telecommunications Technology Experiences with IBIS Models

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Overview

IBIS Models have played an important role in signal integrity analysis

- Access Buffer Characteristics
- Waveform Quality Check
- Timing Analysis

What Information can we get ?

- Use V-I Curves to calculate the driver output impedance
- V-t Curve provides the Buffer's transition time
- C_comp provides intuitional info of the load

Waveform Quality Check

Critical Net check

- Edge Trigged Signals
- Clocks

Check Contents

- Incident Voltage
- Edge Monotonic
- High /Low noise margin
- Source/sink currents

Flight Time Calculating

- Flight Time provides more reasonable descriptions than T.L Propagation Delay in Timing Budgets calculation
- T.L Delay ,loads and topology effects are taken into consideration

Mostly used model parameters

- IBIS 1.0 V-I Curves
- IBIS 1.0 C_comp
- IBIS 2.1 rise/fall waveforms
- IBIS 2.1 Pin mapping

- IBIS 3.2 seldom
- IBIS 4.0 seldom

Typical Problems

- Non-monotonic data in PU/PD table
- DC point does not match I-V load line
- V-t tables End slope not flat
- …

Always tools will filter these points,but good Understanding of these warning is necessary

Successful stories

- Multi-Drop bus Analysis

  When debugging we found data was improperly strobed .Post analysis shows there is non-Monotonic Clock Edge. Using high bandwidth probe check again and got it

- Timing Analysis

  Strong Driver results in Hold time conflict

Occurs at “Low Speed” situation

Behind these stories

IBIS models provides some clues in Waveform Quality check. But

- How Simulator processes the model is a black box
- Simulated result sometimes are tools relevant

Behind these stories

Timing Analysis

- Different Driver strength results in great different Delay
- Under low speed situation Timing analysis was proven and the IBIS model works well
- IBIS model can't describe the internal delay of the buffer . when doing timing analysis we always puzzle about the "Zero" reference point . especially when timing budgets is tight
- Closing the Timing loop requires Core-to-core timing

Problems

- High Speed Serial Interconnect have widely used . But effective analysis was lagged
- Find Bugs of Serial Interconnect is more difficult than old designs . Maybe it is an impossible task

We are expecting