Splitting C_comp for Power Integrity Simulations

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Content

- Why C_comp and its split ratio are important for power integrity simulations?
- The procedures to extract the C_comp and C_decap values from HSPICE simulations
- Simulation results for Micron U27_a_dq buffer

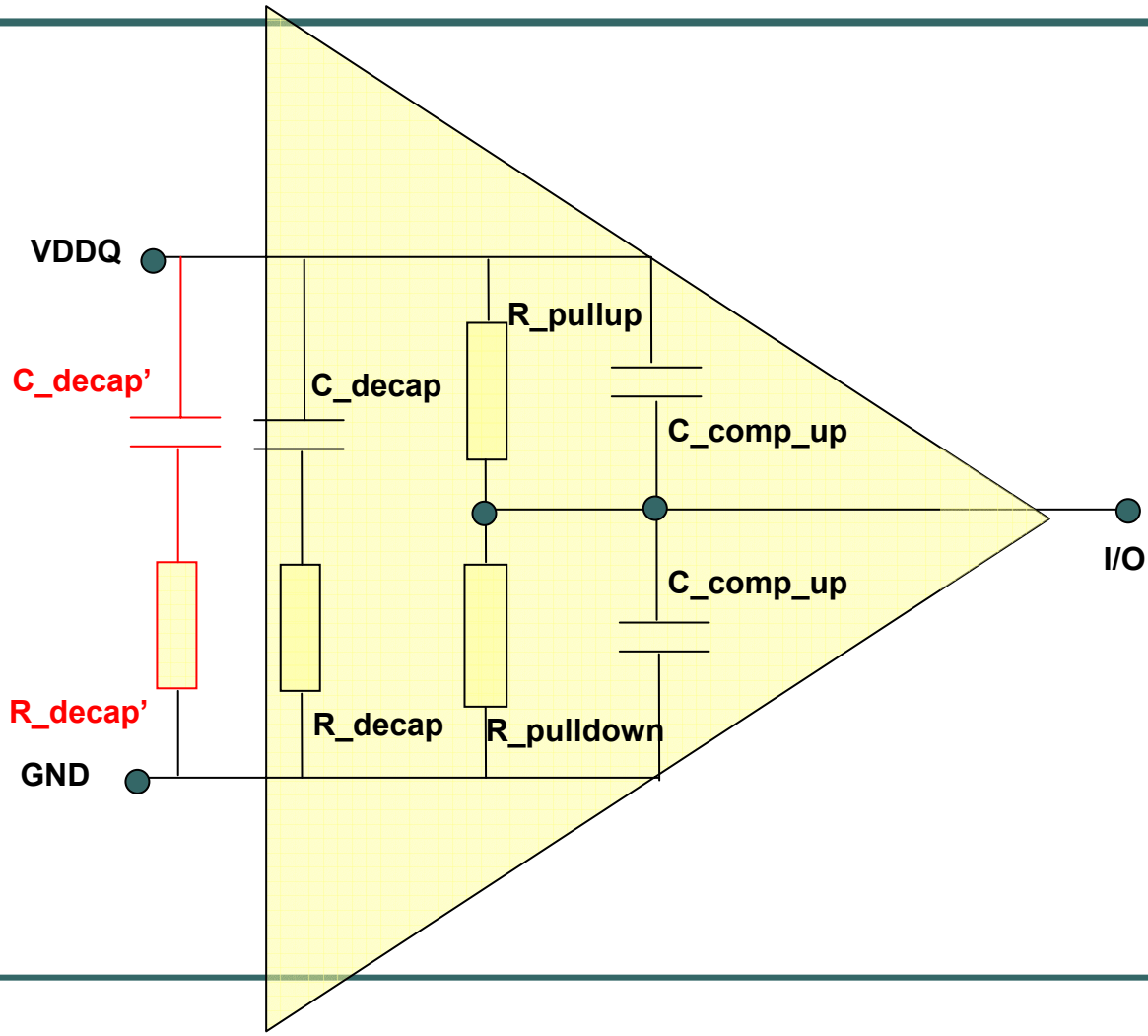
Why C_comp and its split ratio are important for power integrity simulations?

C_comp could impact the power integrity simulations in following ways:

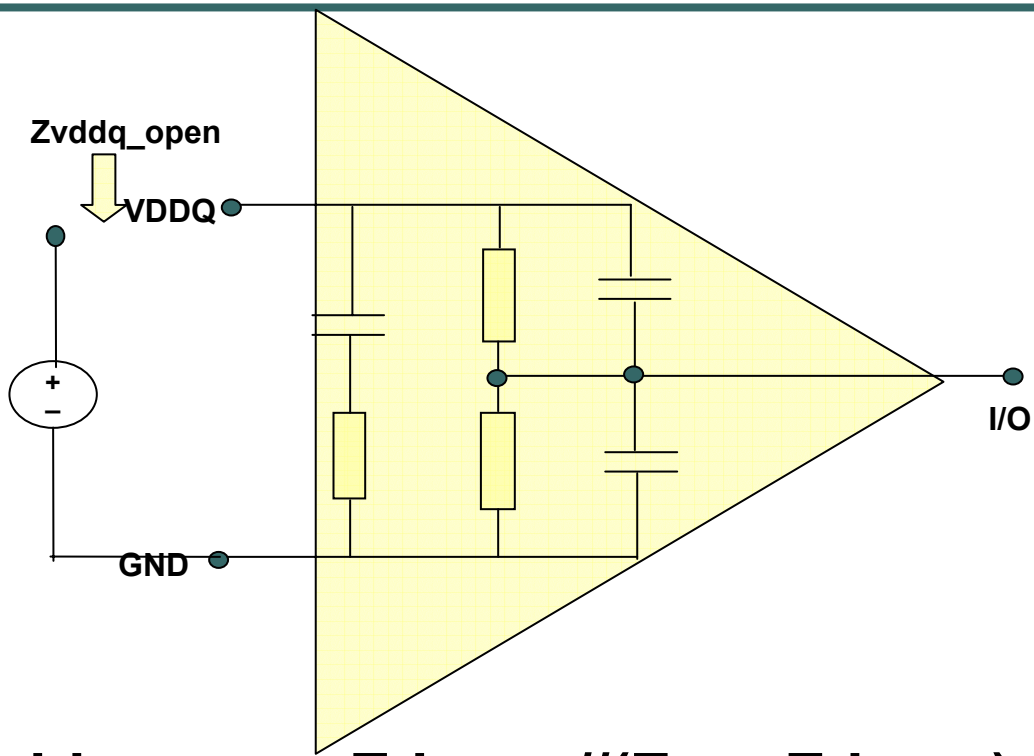
- C_comp at non-switching I/O could act as effective local decoupling caps. The ratio has a big impact.
- C_comp split ratio heavily impacts the noise level coupled from power supply to quite I/O pins, especially at high frequency.
- C_comp split ratio will have direct impact on dynamic current distribution for switching I/O buffers

Note: C_comp split ratio has no impact on SI simulations when voltage supply is ideal.

Simplified I/O model for IBIS specification



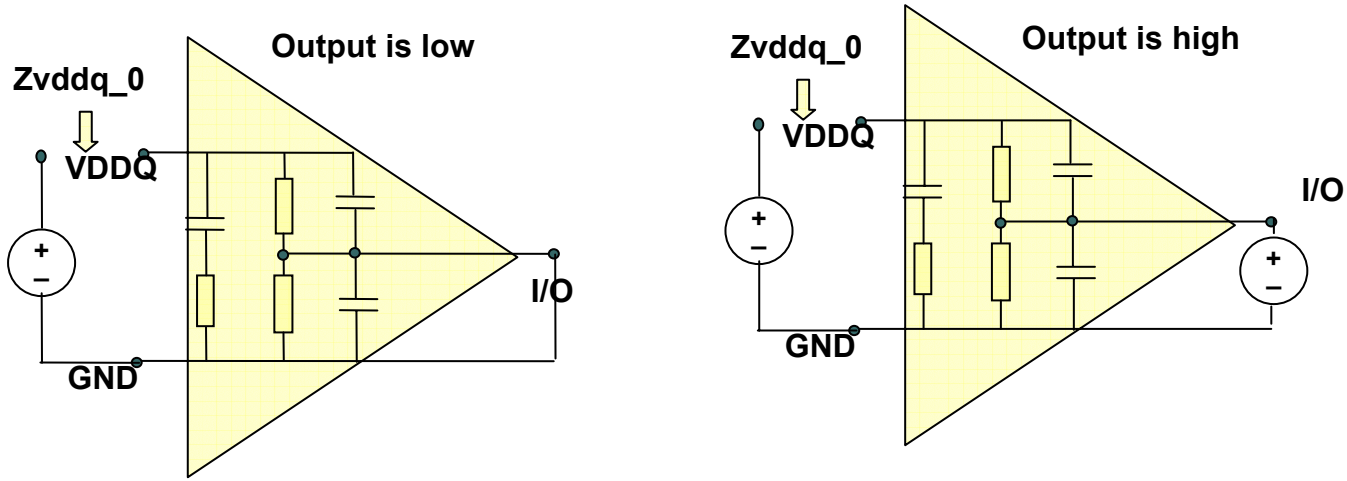
Zvddq_open



$$Zvddq\_open = Zdecap // (Zup + Zdown) \quad (1\text{-}1)$$

$$Yvddq\_open = Ydecap + (Yup * Ydown)/(Yup + Ydown) \quad (1\text{-}2)$$

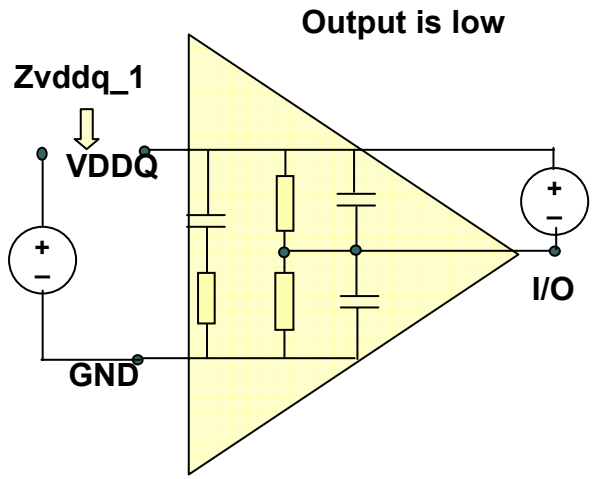
Z_vddq_short_to_gnd

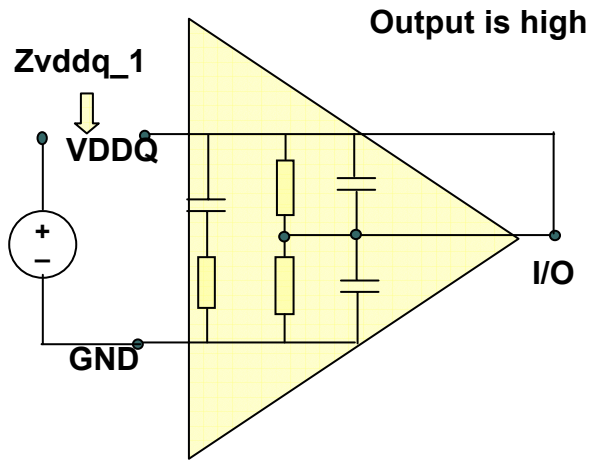


$$Zvddq\_0 = Zdecap // Zup \quad (2\text{-}1)$$

$$Yvddq\_0 = Ydecap + Yup \quad (2\text{-}2)$$

Z_vddq_short_to_pwr

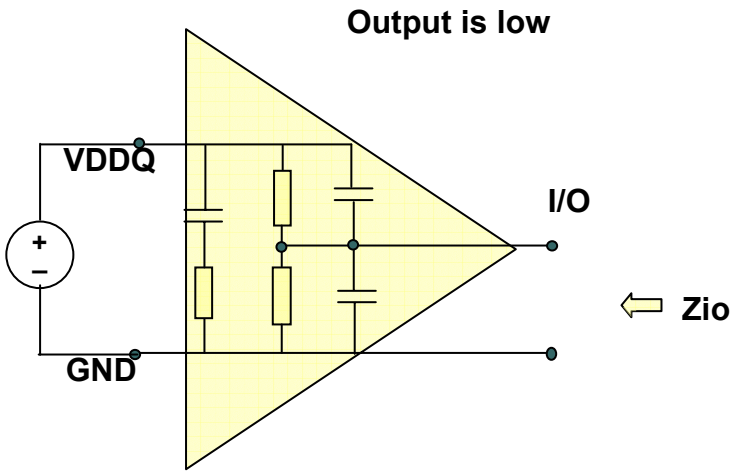


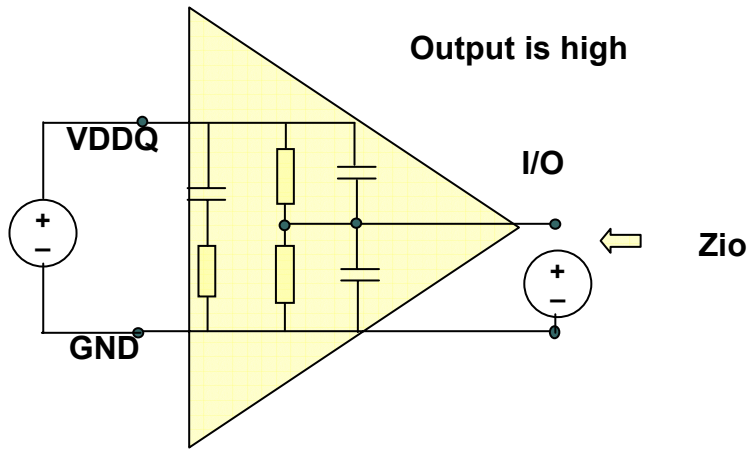


Zvddq_1=Zdecap//Zdown (3-1)

Yvddq_1=Ydecap+Ydown (3-2)

Z_io





$$Zio = Zdown // Zup \quad (4\text{-}1)$$

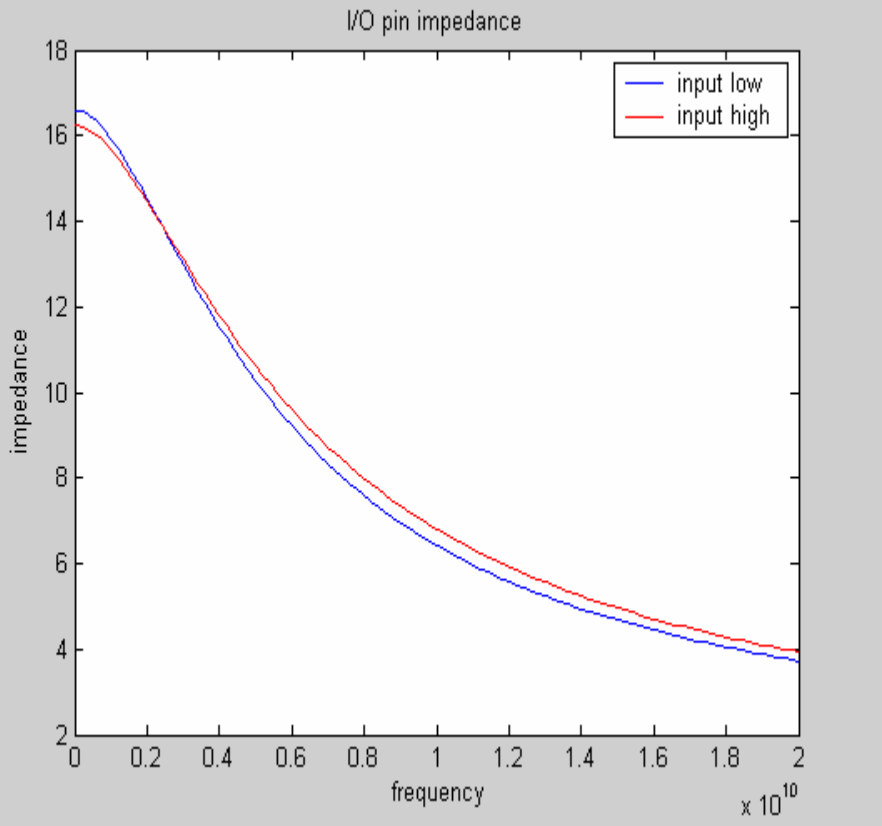
$$Yio = Ydown + Yup \quad (4\text{-}2)$$

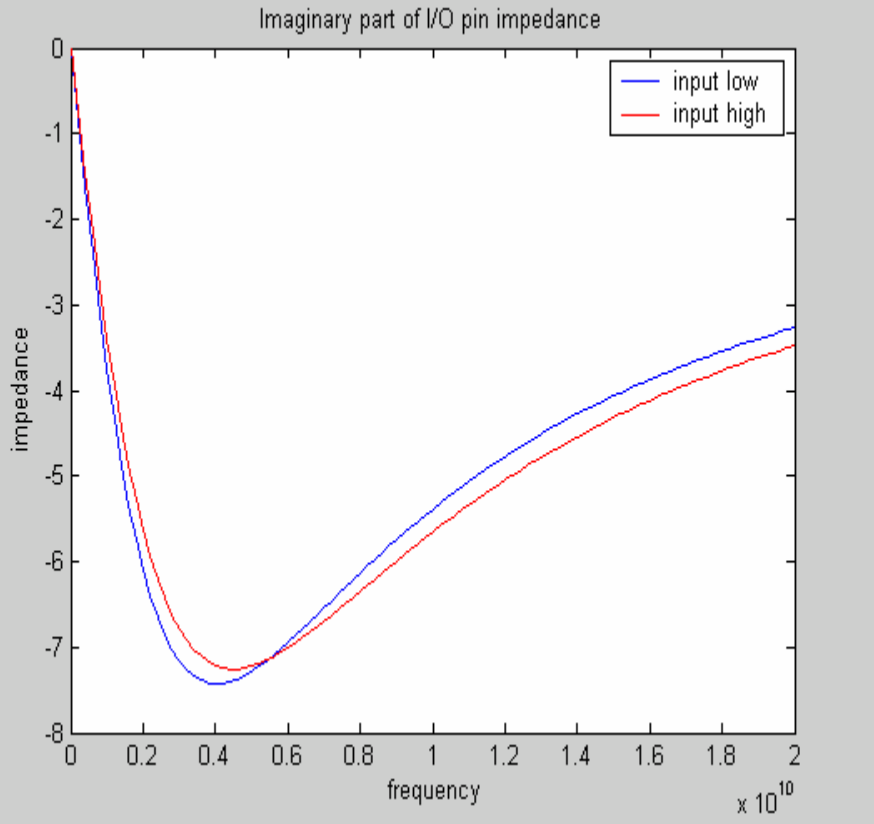
Extraction of Yup, Ydown and Ydecap

- Yvddq_0=Ydecap+Yup (2-2)
- Yvddq_1=Ydecap+Ydown (3-2)
- Yio=Yup+Ydown (4-2)

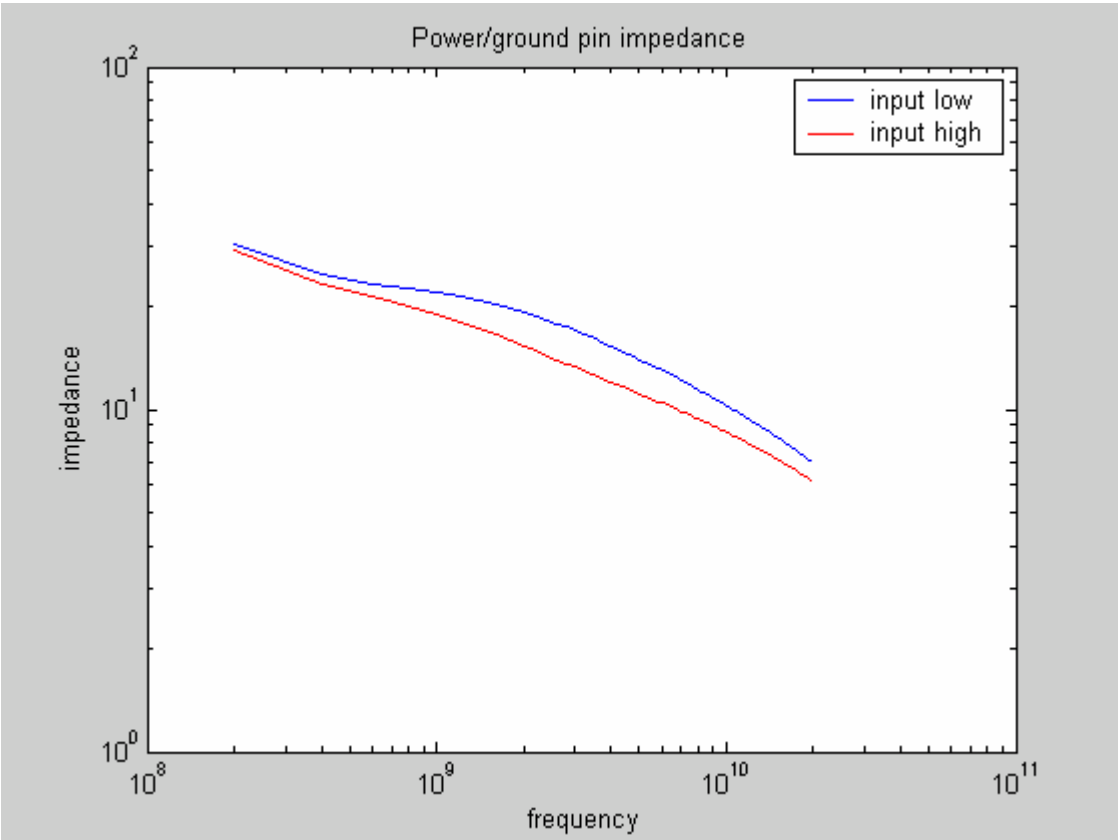
- Yup=(Yvddq_0+Yvddq_1+Yio)/2-Yvddq_1 (5-1)
- Ydown=(Yvddq_0+Yvddq_1+Yio)/2-Yvddq_0 (5-2)
- Ydecap=(Yvddq_0+Yvddq_1+Yio)/2-Yio (5-3)

I/O pin impedance

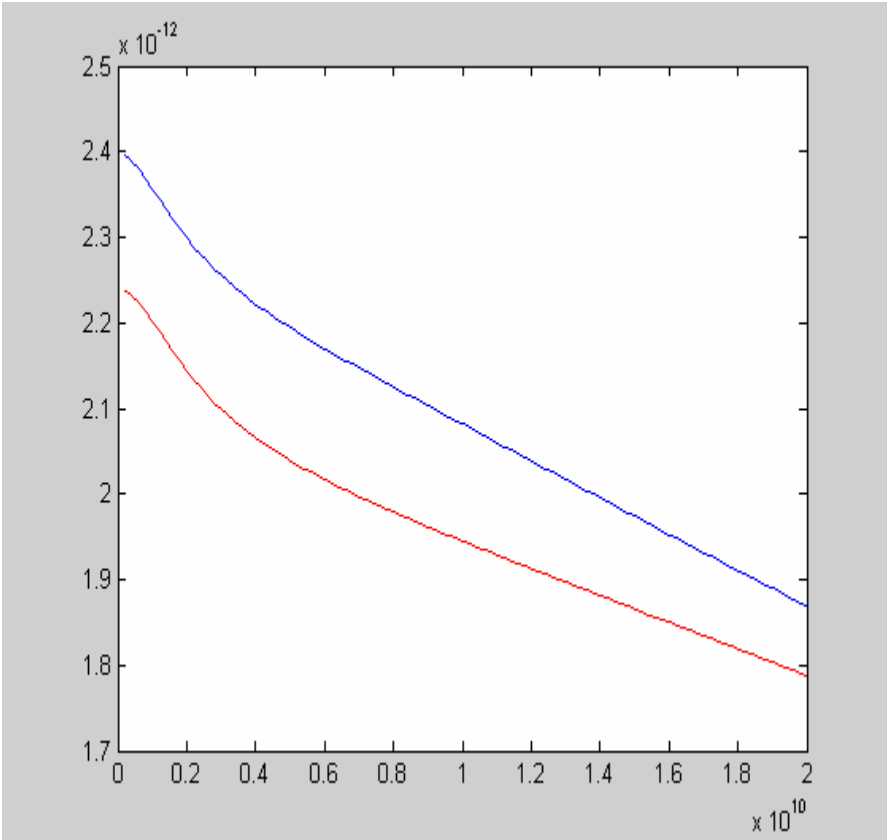




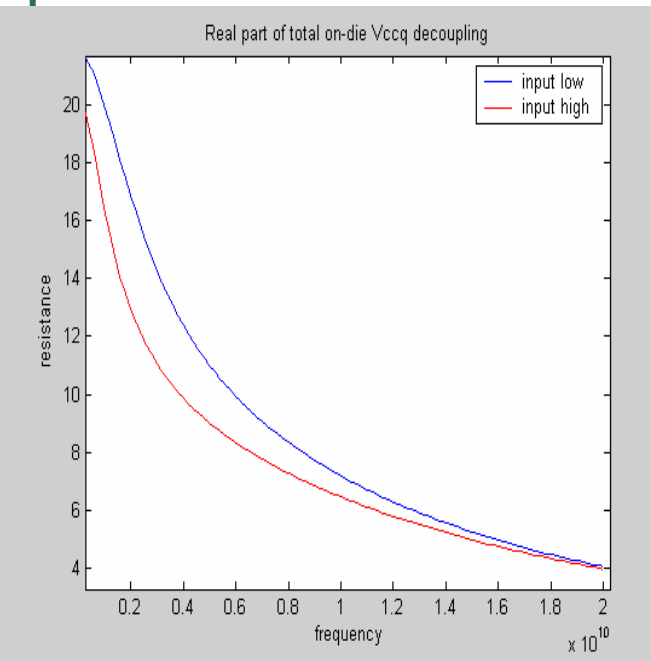
Power/ground impedance when I/O pin is open



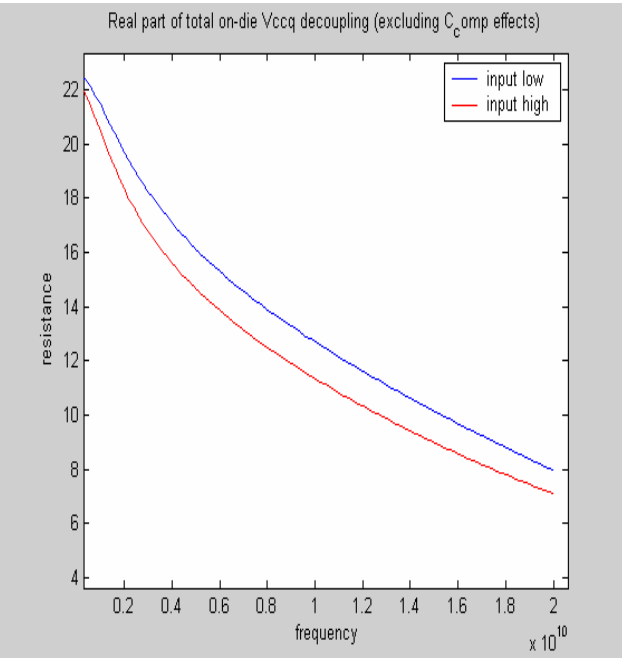
I/O pin capacitance



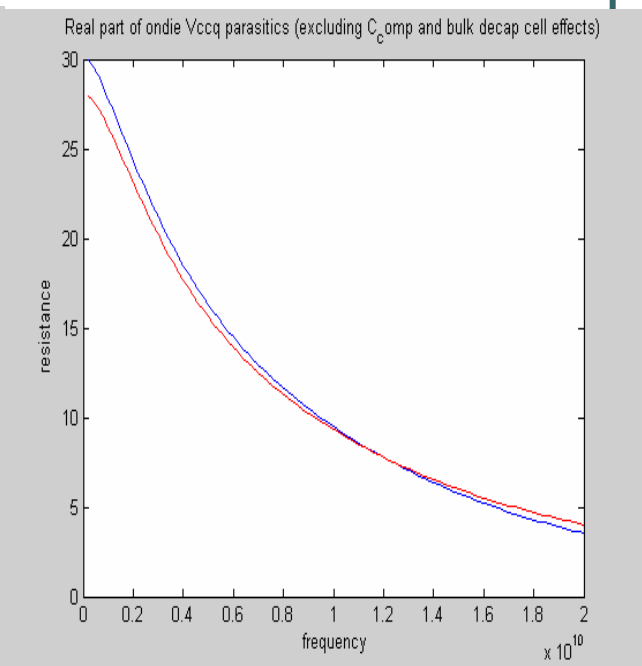
Vccq parasitic resistance



Everything included

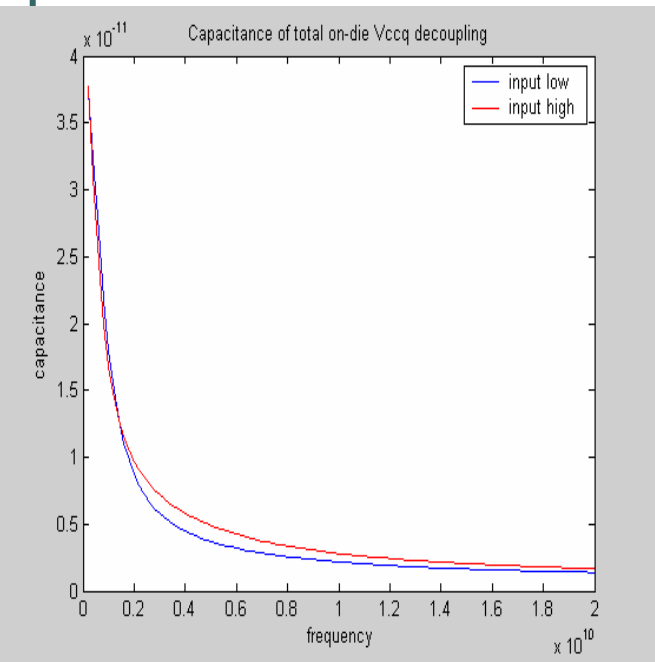


C_comp effect excluded

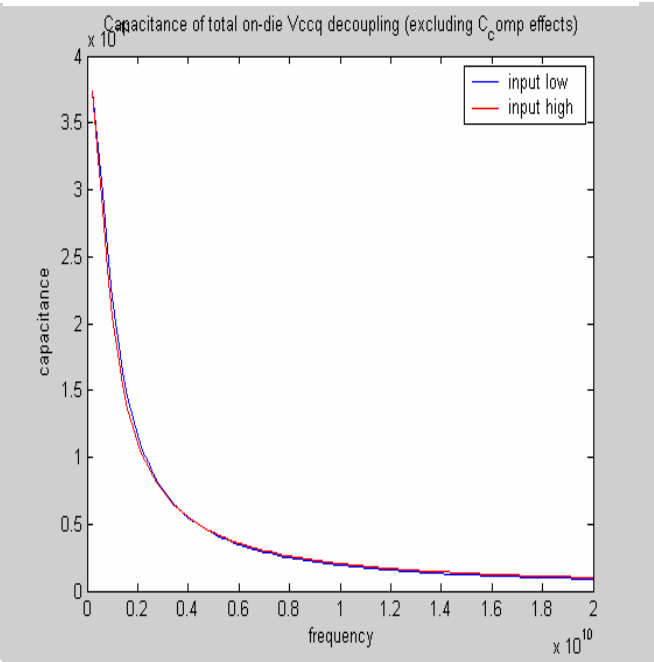


C_comp and lumped decap cell effect excluded

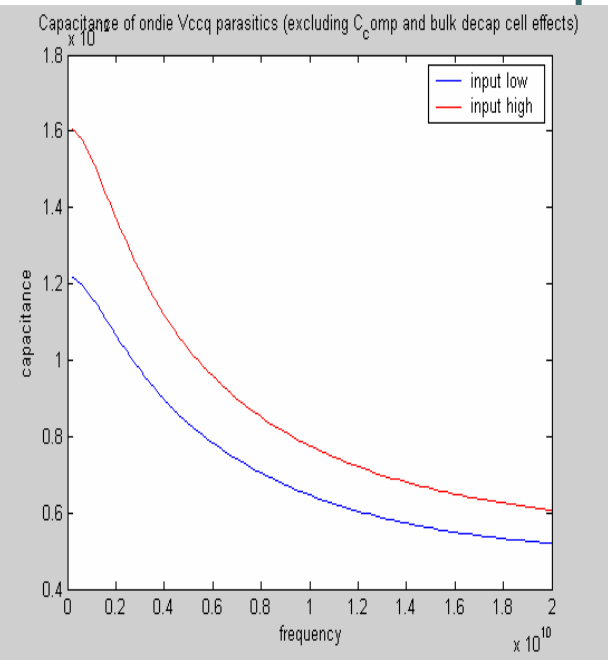
Vccq parasitic capacitance



Everything included

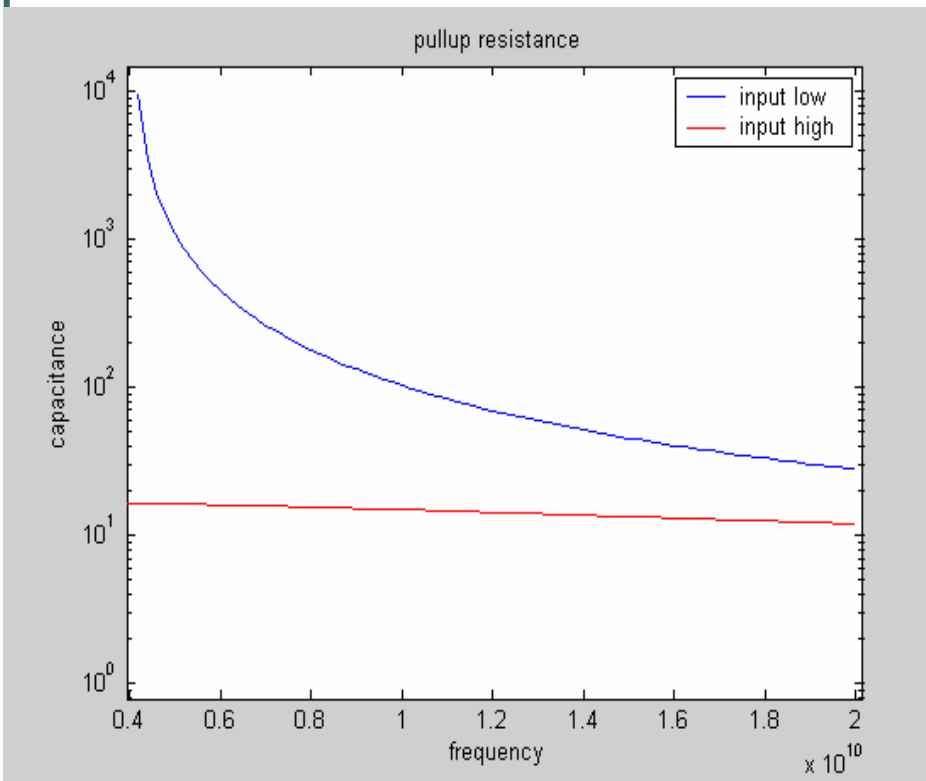


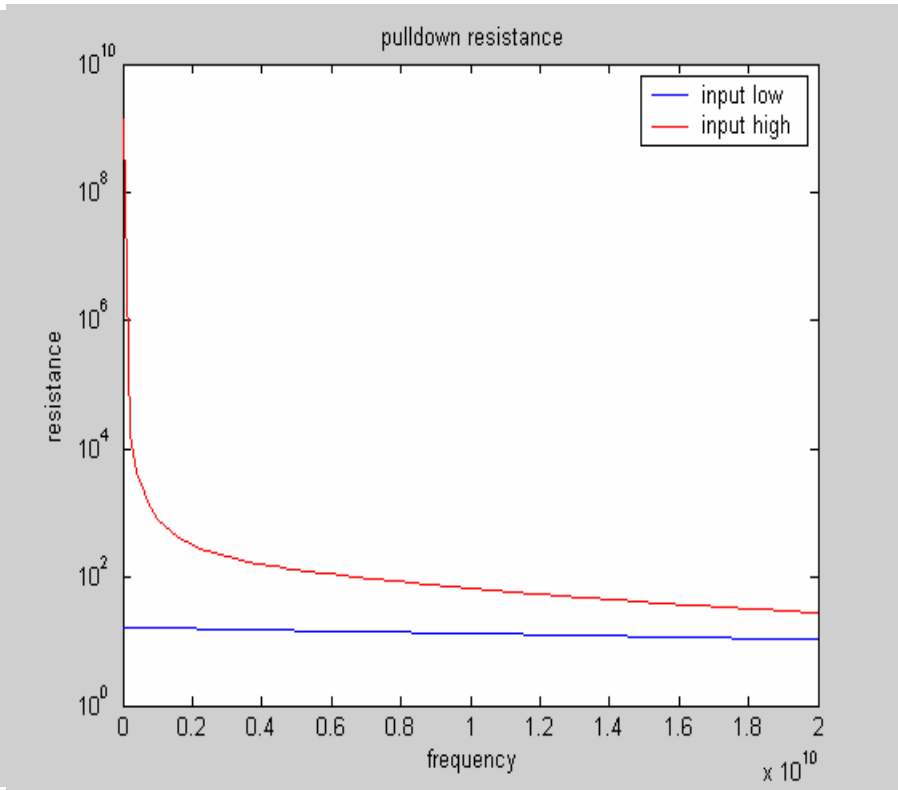
C_comp effect excluded



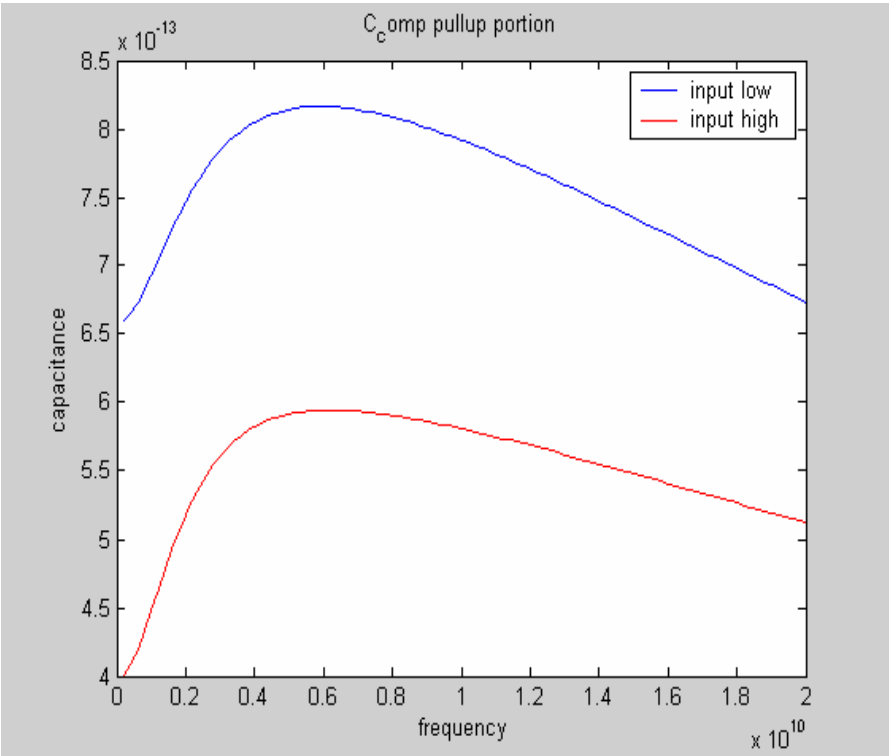
C_comp and lumped decap cell effect excluded

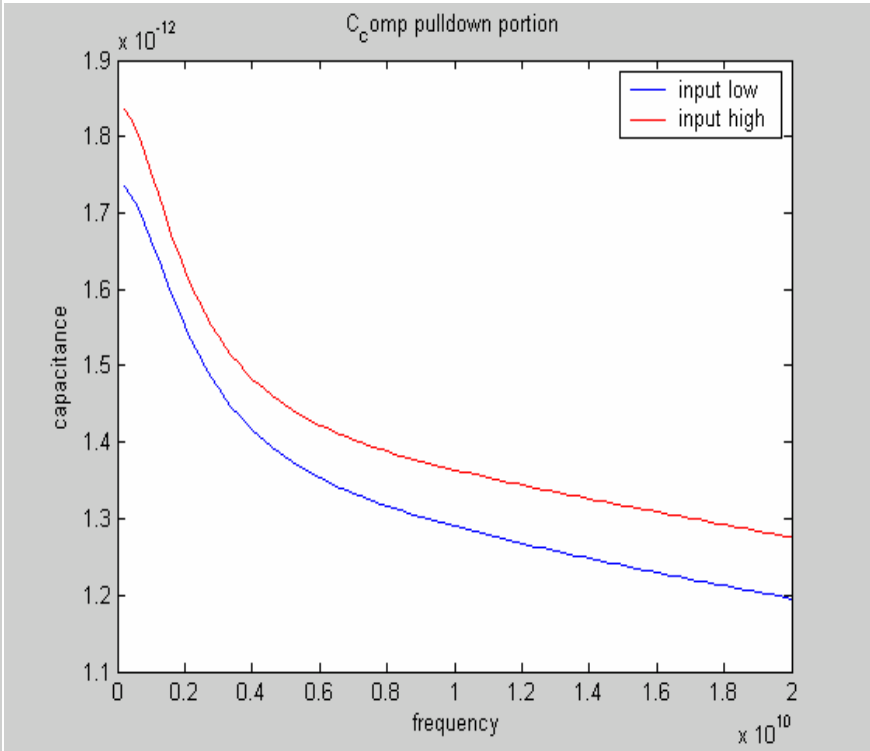
Pull_up and Pull_down resistance





Pull_up and Pull_down capacitance





Conclusions

- C_comp is frequency and state dependent
- C_comp split ratio is also frequency and state dependent
- C_comp and its split ratio are very important factors for correct power integrity simulations
- Existing C_comp and I/V table may not completely model the frequency dependent property of I/O buffer, even at steady state.

Q&A

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