

IBIS在信号完整性分析中的应用

Using IBIS for SI Analysis



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Outline

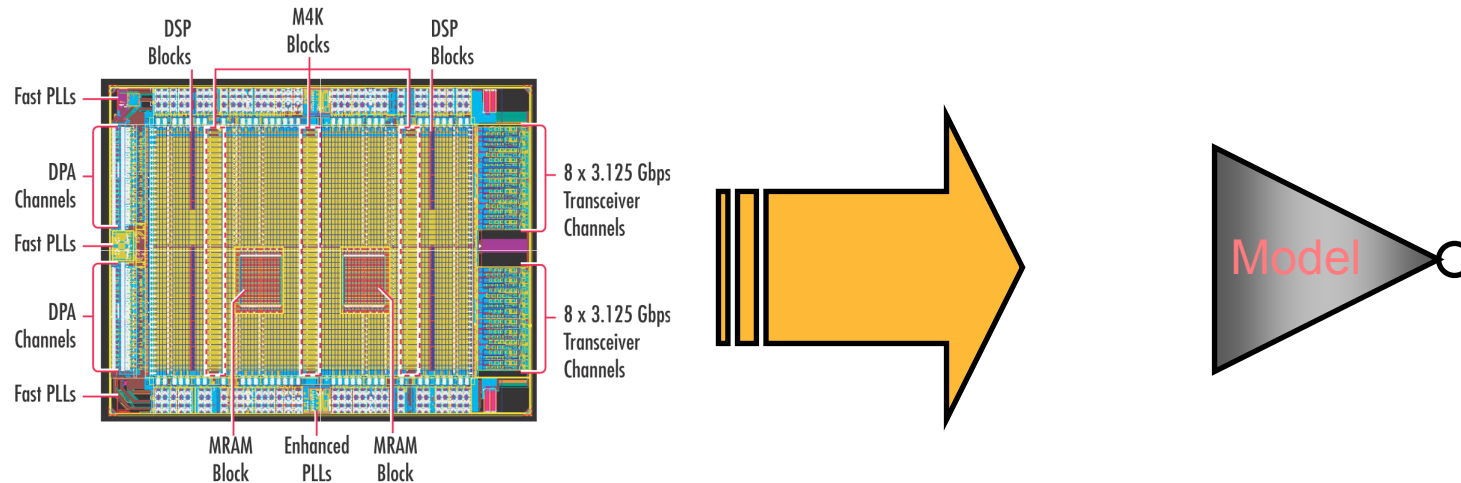
- What happened on IBIS （IBIS历史）
- Why IBIS （IBIS的好处）
 - Speed and Accuracy （速度和精度）
 - Industrial Examples （工业化例子）
- Advanced IBIS Technologies （加强型IBIS技术）
 - Complex-IO Devices （复杂I/O器件）
 - Macromodeling is a solution （宏模型解决方案）
 - Experiences and Industrial Examples （经验和工业化例子）

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- **What happened on IBIS** （IBIS历史）
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What happened on IBIS

- Spice Transistor Level Models (晶体管级模型建模流程)

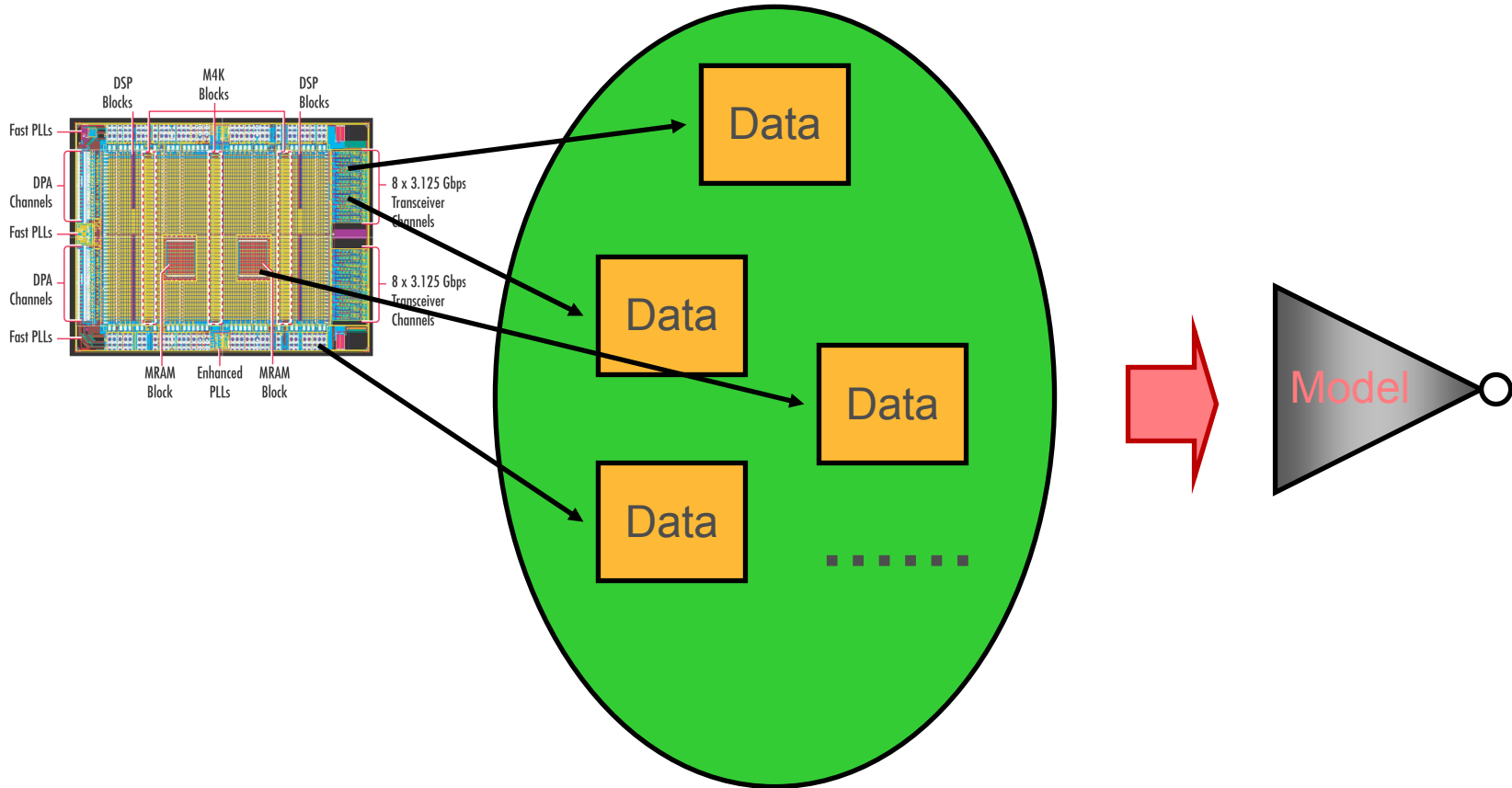


Layout Extractions (非选择性提取)

- Very Complicated
- A lots of unusable stuff
- Too slow in the simulations

What happened on IBIS

- Behavioral Models (行为级模型建模流程)

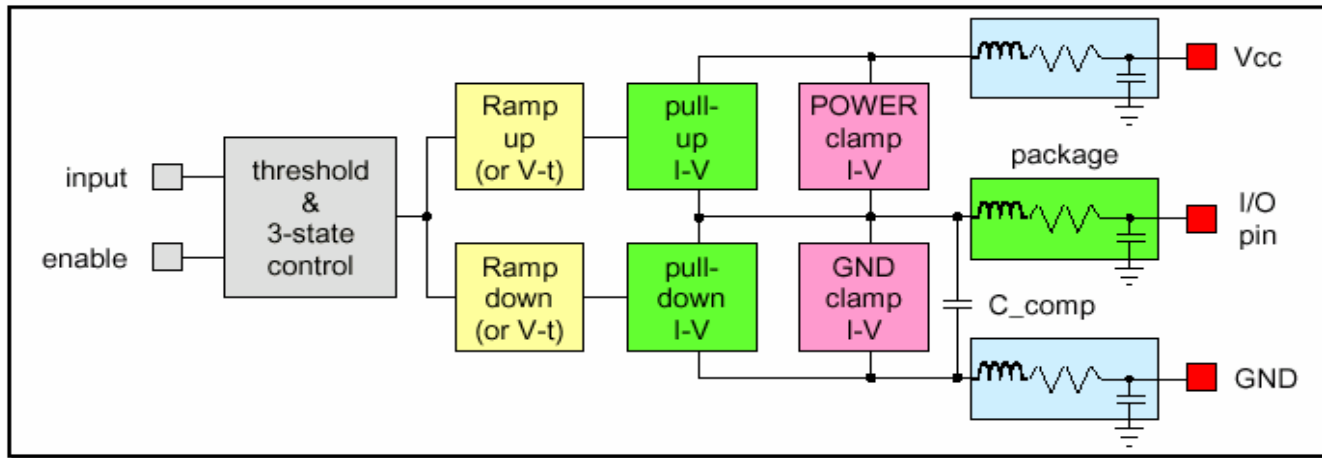


Behavioral Extractions 选择性提取

What happened on IBIS

- IBIS is behavioral Model (IBIS是行为级模型)

IBIS model



Block diagram of CMOS buffer

A basic IBIS model consists of:

four I-V curves: - pullup & POWER clamp
- pulldown & GND clamp

two ramps: - dV/dt_{rise}
- dV/dt_{fall}

die capacitance: - C_{comp}

packaging: - RLC values

for each buffer on a chip

What happened on IBIS

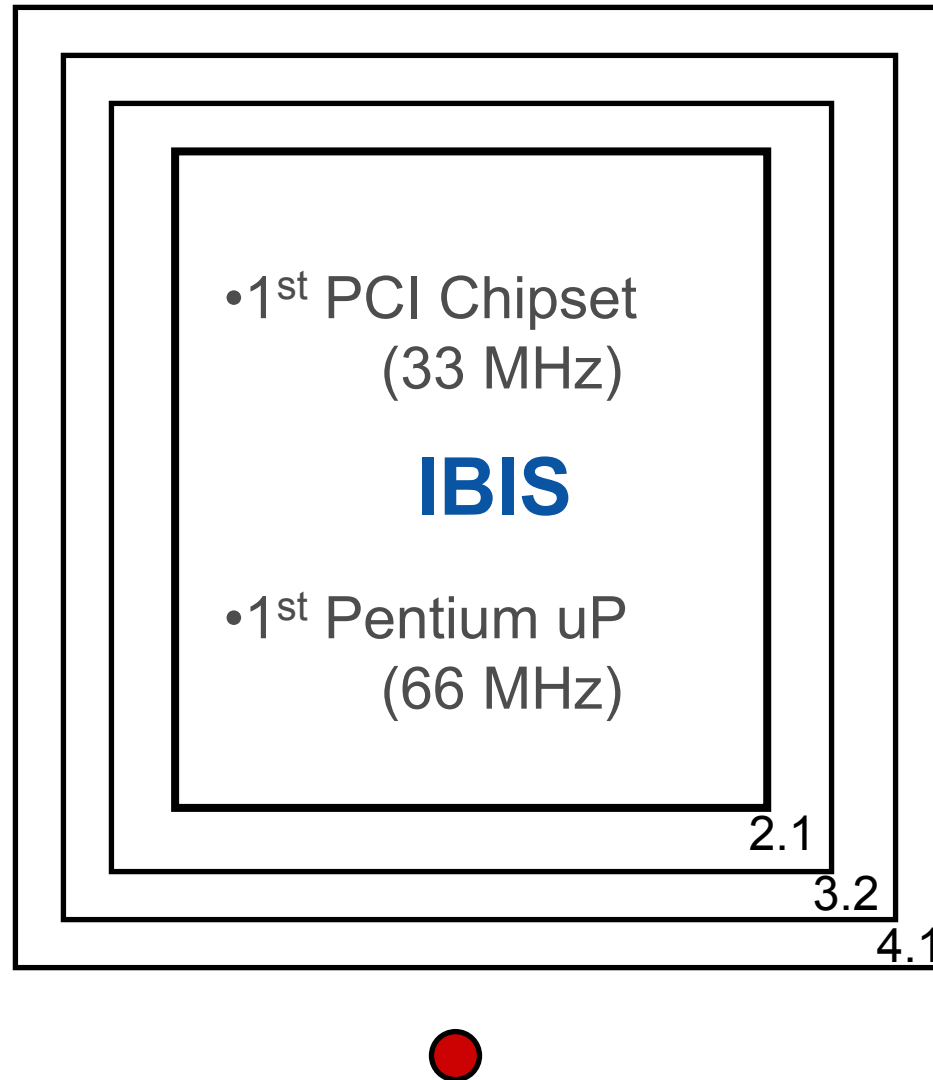
- The Original “Box”

- 1st PCI Chipset
(33 MHz)

IBIS

- 1st Pentium uP
(66 MHz)

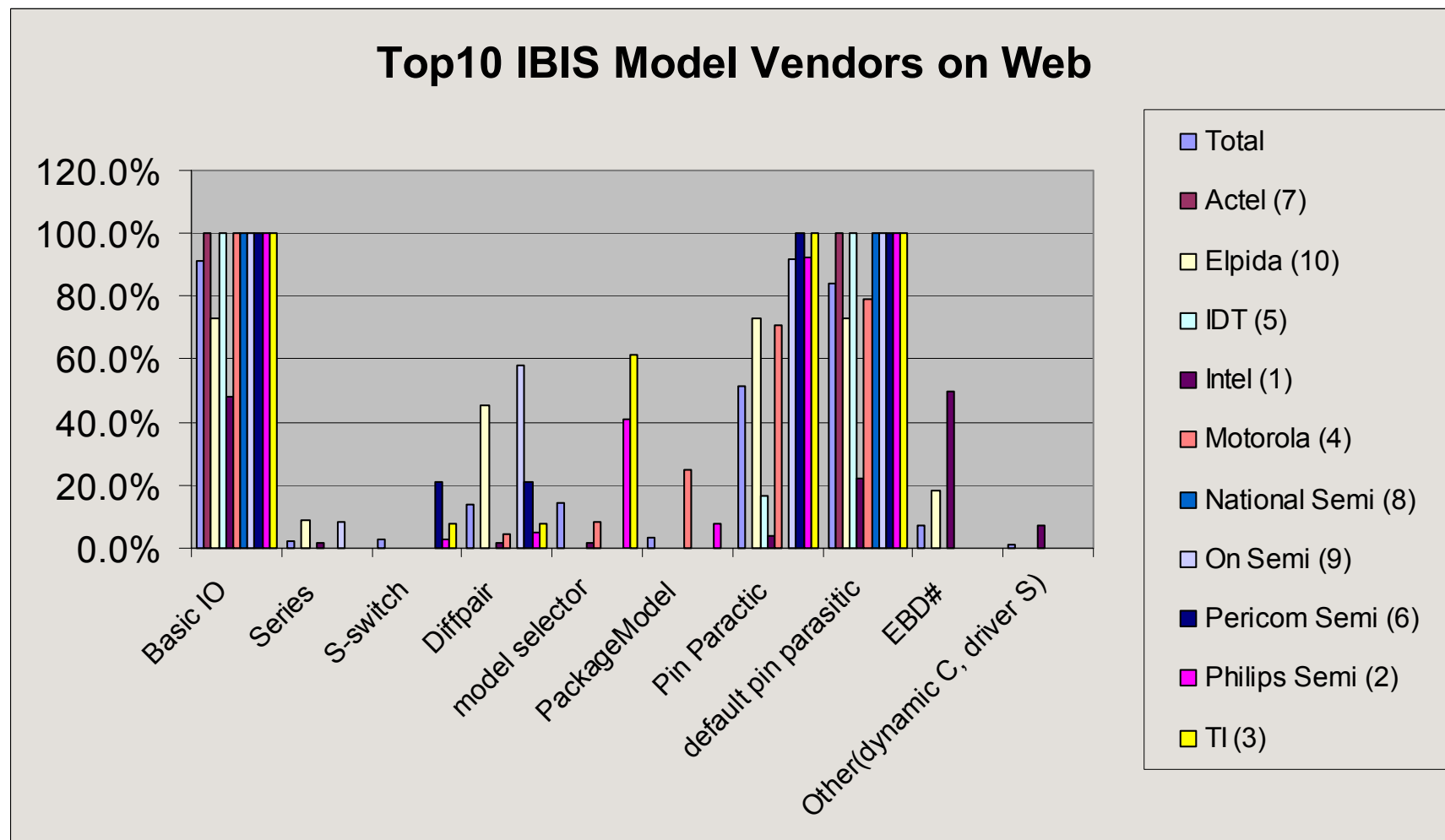
...and the “Box” did grow



*An increasing
amount of Complex
IO models are
missing the box*

What happened on IBIS

- IBIS Model Vendors (IBIS模型提供者)



What happened on IBIS

- IBIS in EDA Tools (IBIS在EDA工具中的应用)

- Major EDA Simulators are supporting IBIS now
 - Cadence
 - Mentor

SPICE Simulators are taking IBIS now !!!

- Agilent

And many, many more

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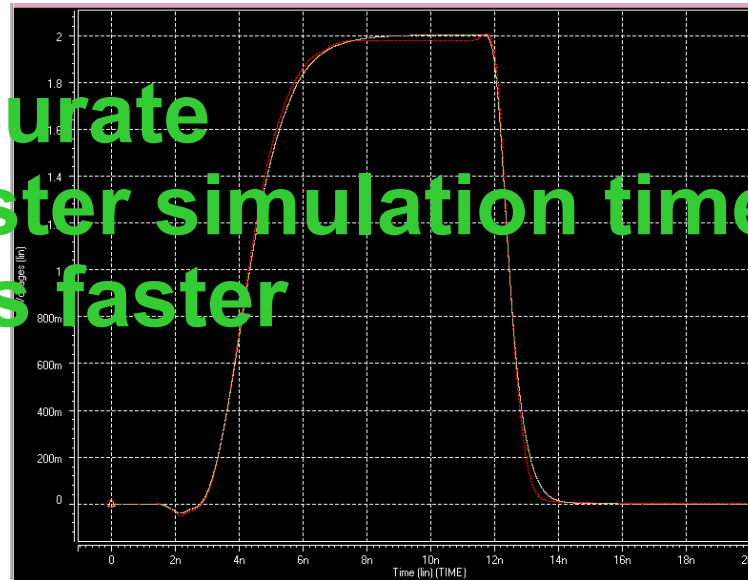
Why IBIS (IBIS的好处)

-Speed and Accuracy (速度和精度)

- Behavioral data in Spice simulators

$$I(\text{pad}) = I_{pd}(V(\text{pad}) - V(\text{gnd})) * W_d(t) + I_{cd}(V(\text{pad}) - V(\text{gnd_c})) \\ + I_{pu}(V(\text{pad}) - V(\text{pwr})) * W_u(t) + I_{cu}(V(\text{pad}) - V(\text{pwr_c}))$$

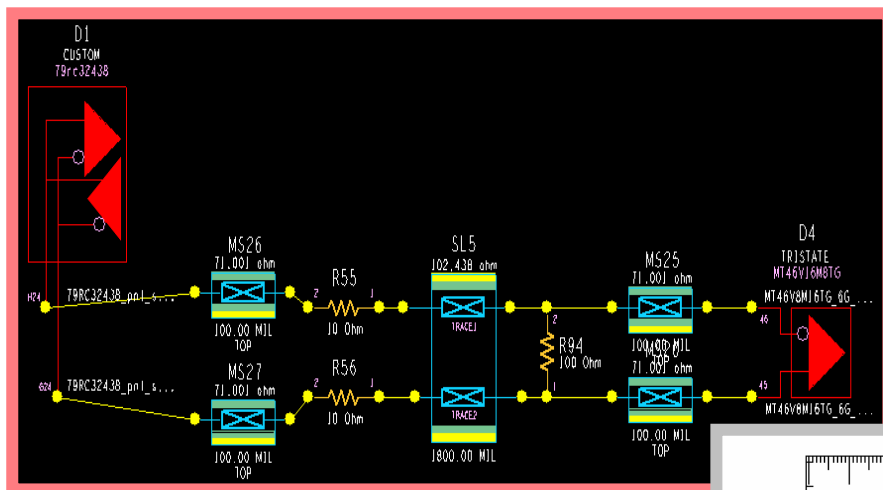
- Results are accurate
- Much, much faster simulation time
 - 20-1000 times faster
- IP Protected



HSpice Transistor Model vs. IBIS Model

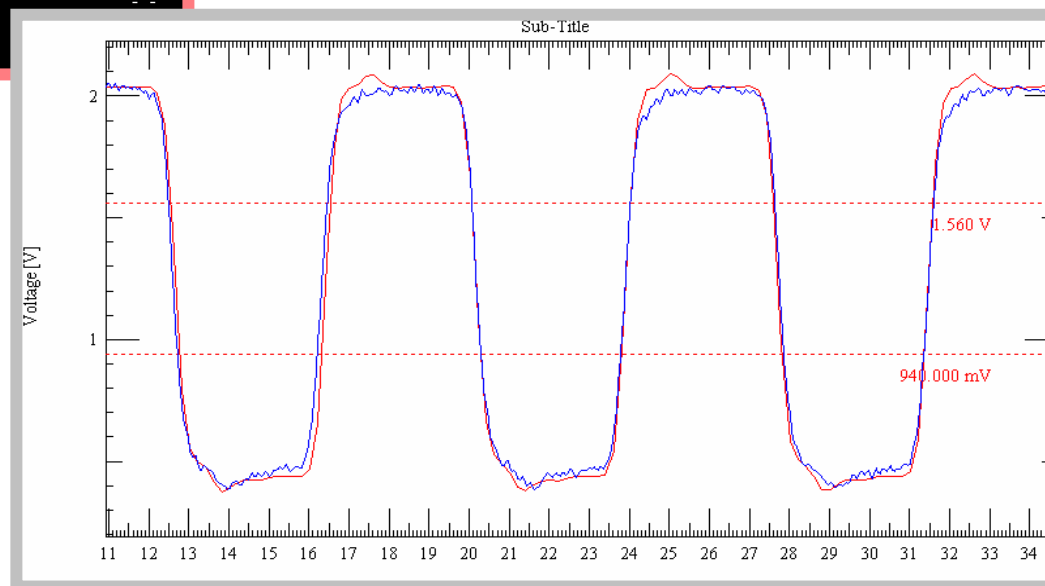
Why IBIS (IBIS的好处)

- Industrial Examples (工业化例子) (133MHz)



Driver: IDT 79RC32438

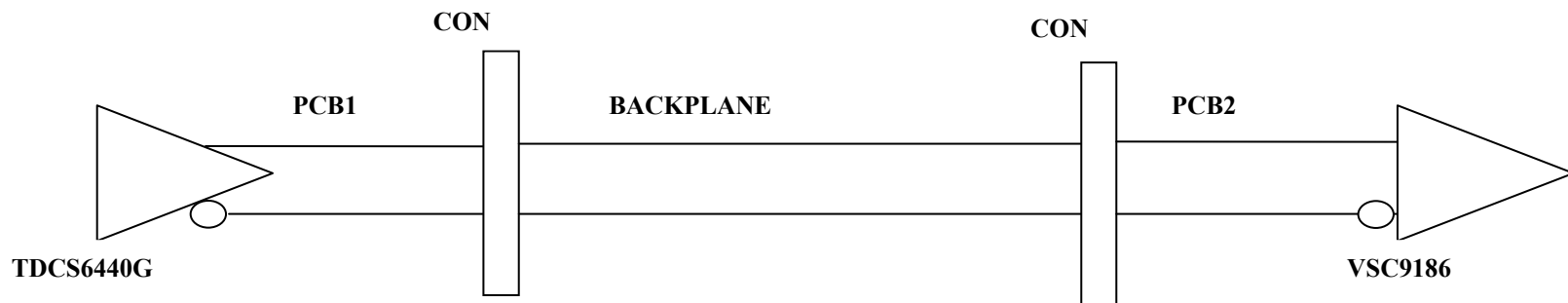
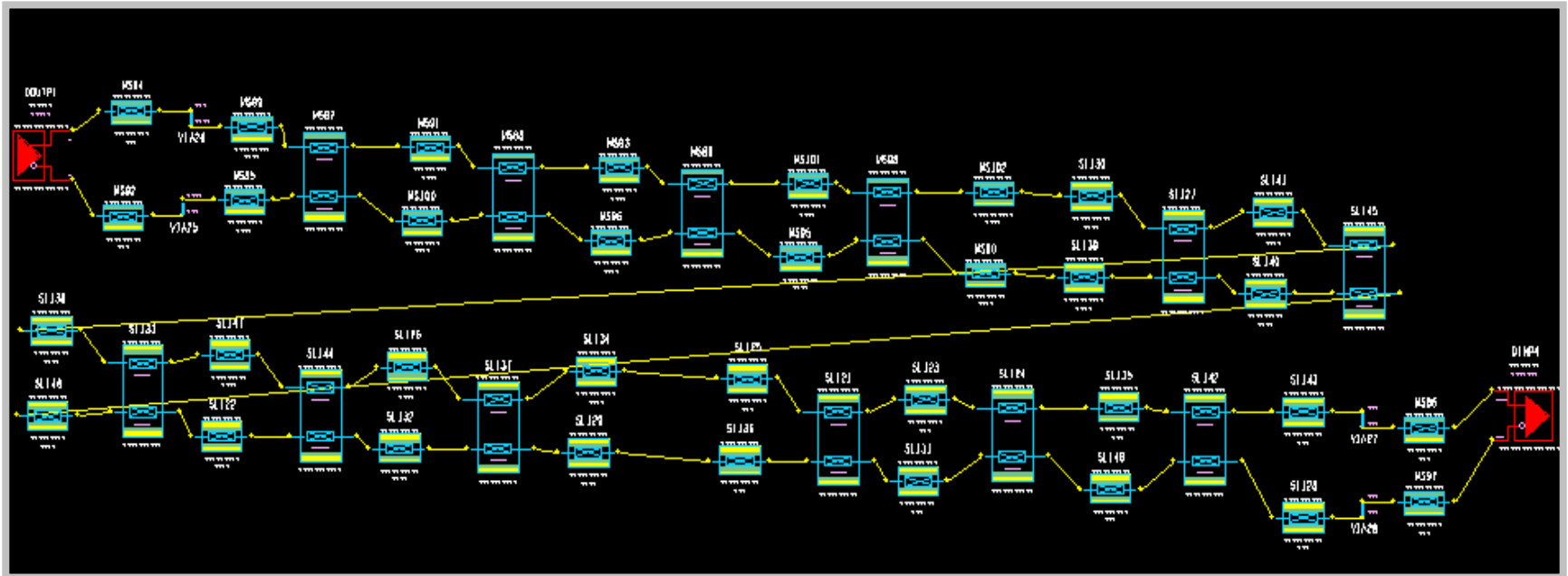
Receiver: Micron MT46V16M8TG



Blue: Measured result

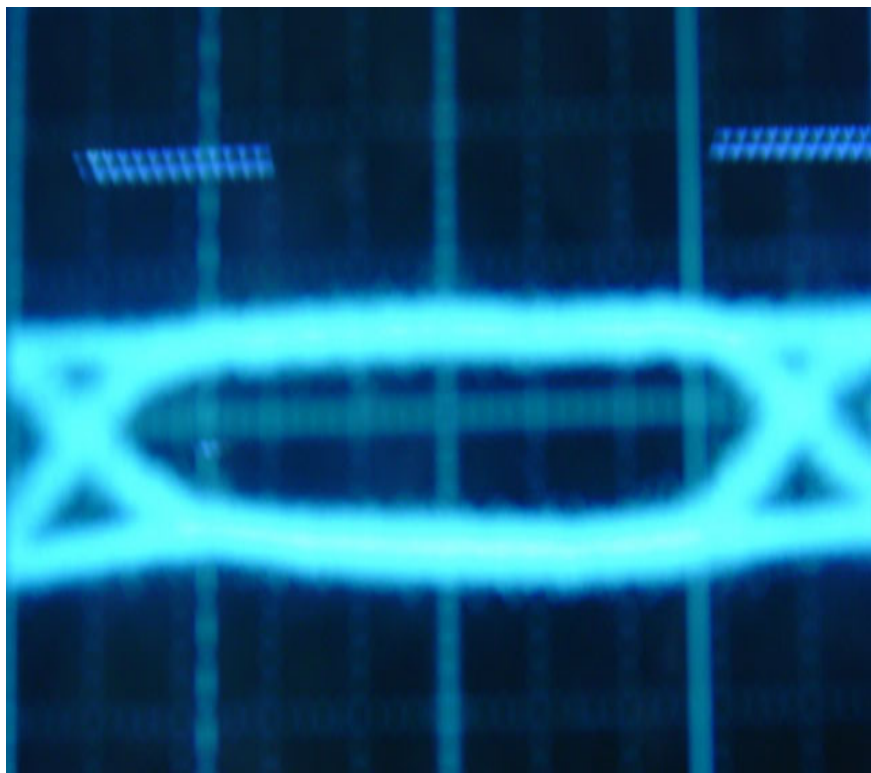
Red: Simulated result

- Industrial Examples (工业化例子) (622Mbps)



Why IBIS (IBIS的好处)

- Industrial Examples (工业化例子) (622Mbps)

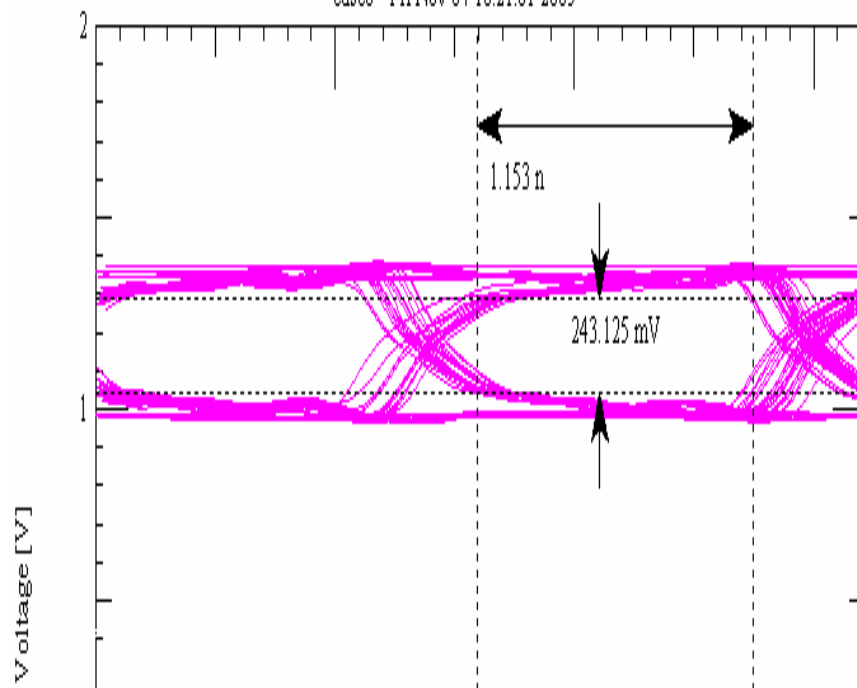


Eye Height: 210mV

Eye Width: 1.1ns

sim1: (B DOUTP1 1) B DOUTP1 1 Pulse Typ Reflection

case0 - Fri Nov 04 18:21:01 2005



Eye Height: about 240mV

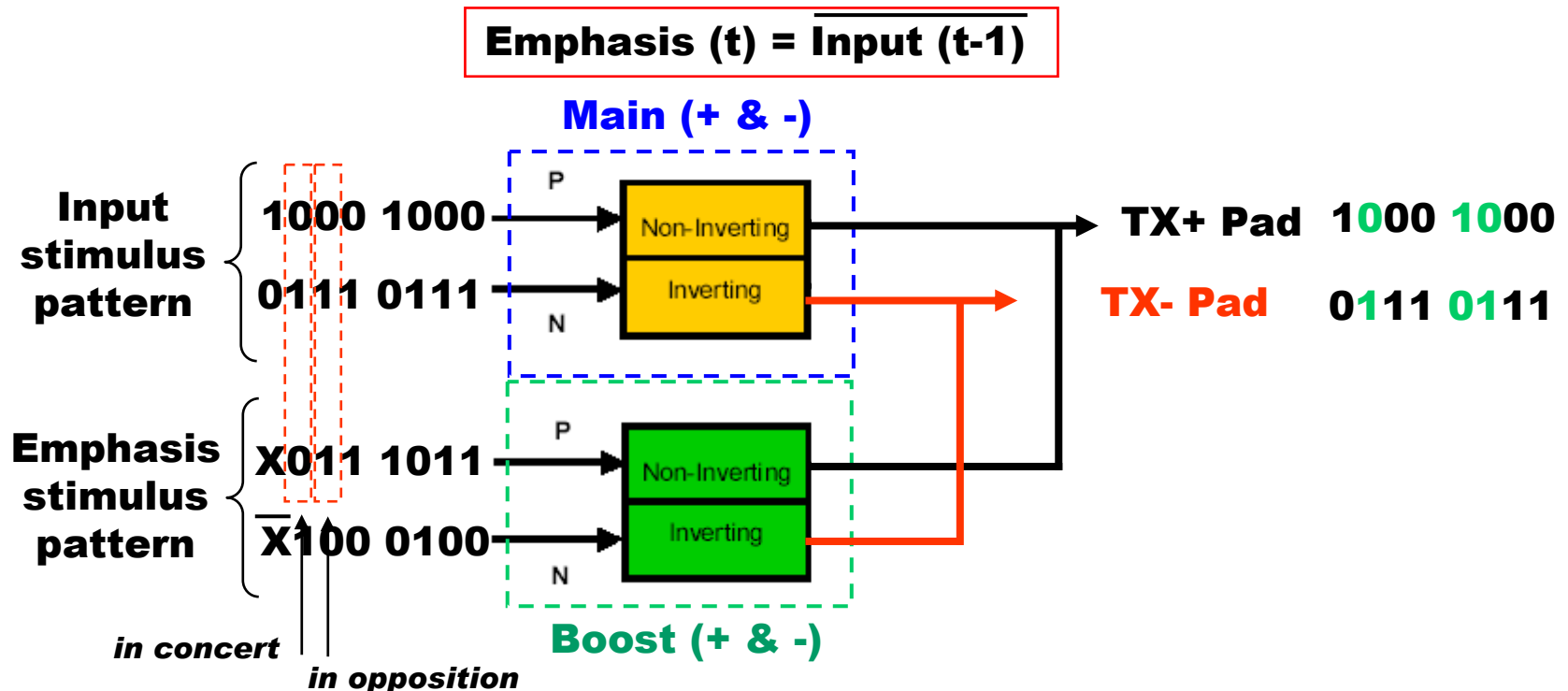
Eye Width: about 1.15ns

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Complex-I/O Devices (复杂I/O器件)

Pre-emphasis预加重/De-emphasis去加



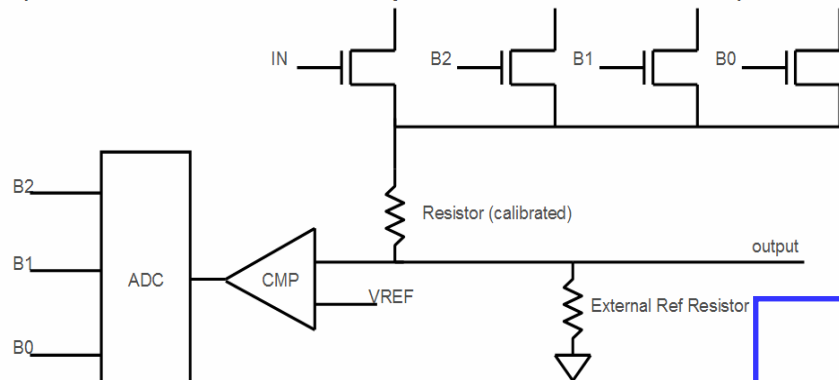
Picture from Michael Mirmak's presentation in DesignCon East IBIS Summit 2004

Complex-I/O Devices (复杂I/O器件)

Self calibrating driver

(Calibrating Output Impedance only)

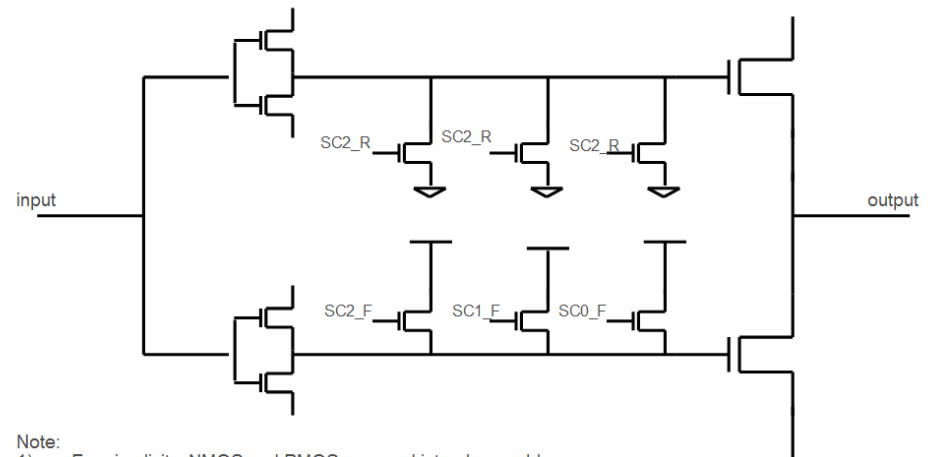
(For DDR2, when controller in a read cycle, the receiver is terminate)
(50 ohms. The resistor also requires to calibrate at run-time)



Note:

1) PMOS side is not being shown here.

Driver with Slew Rate Control



Note:

- 1) For simplicity, NMOS and PMOS are used interchangeably.
- 2) Independent slew control for Rise and Fall.

What is MacroModeling and Why?

KEY Conclusions

Equation-based macromodeling of LVDS drivers

❖ Flexible methodology

- no specific assumption on device internal structure (preserve IP)
- handle drivers with enhanced features (e.g., control ckts)

❖ Accurate and efficient macromodel (5÷10x speed-up)

- ❖ Can directly provide SPICE/VHDL/AMS implementations
- ❖ Ready available also for EDA SI tools via the IBIS multilingual extension

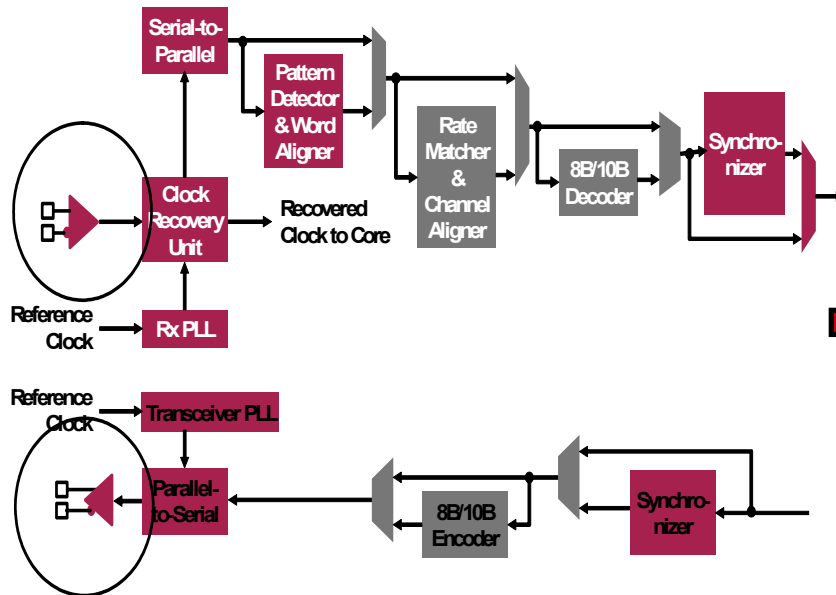
Methodology only

Macromodeling is a Methodology !!!

Macromodel from architecture templates

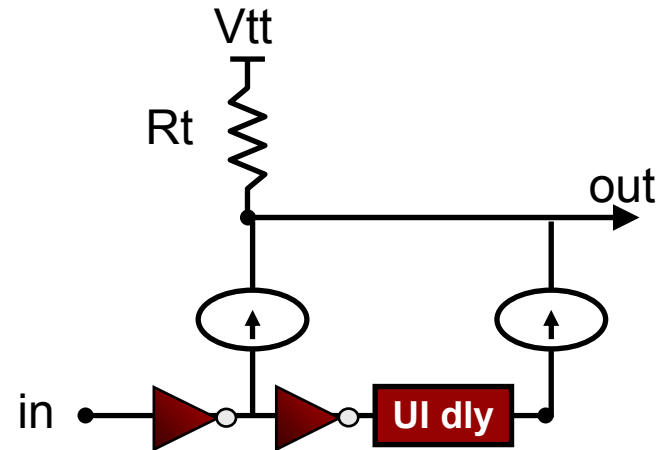
从器件结构中得出宏模型

- Most modern devices are based on known DSP circuit architectures



Known circuit architecture

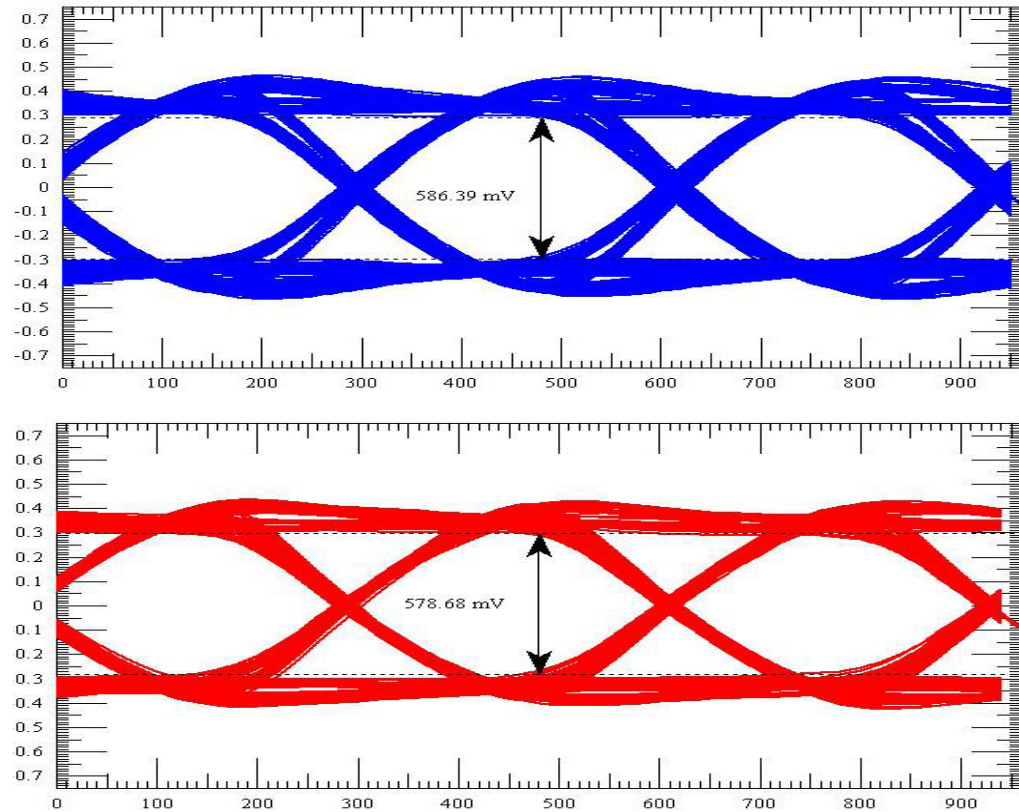
Match template parameters to Layout model to get an accurate macromodel



Macromodel template with parameters

Industry example- Altera Stratix GX

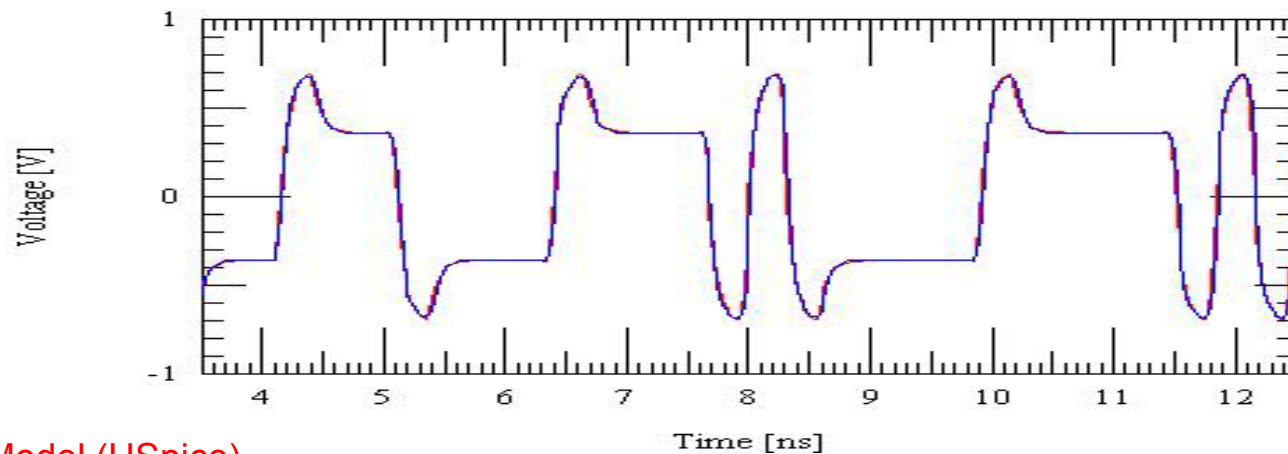
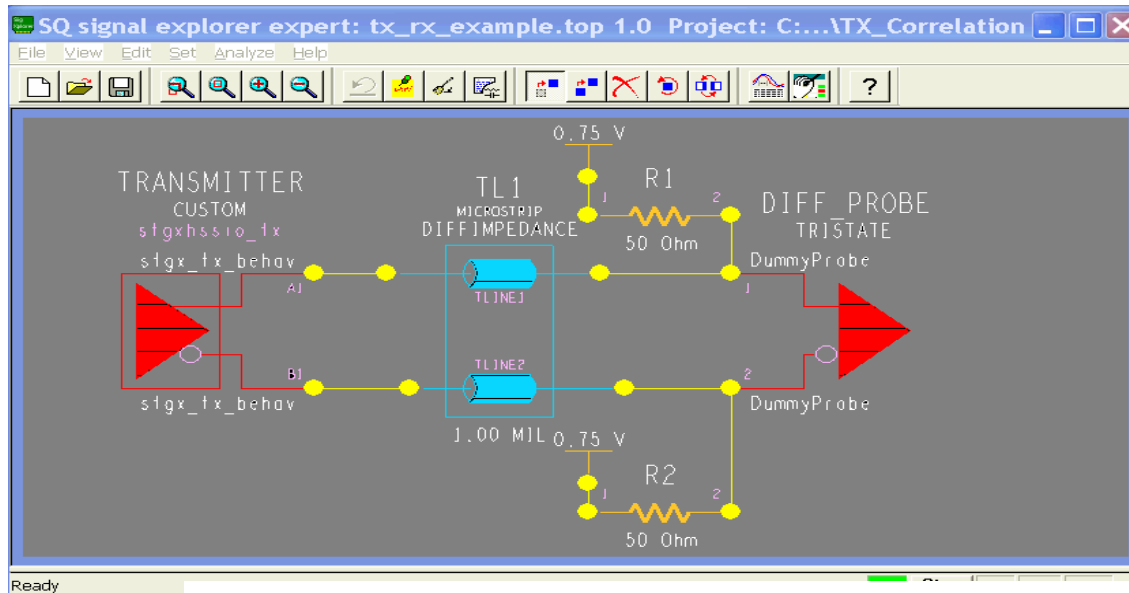
“Altera successfully adapted the MacroModel templates to produce fast and accurate models of our multi-gigabit transceivers. Not only did the resulting model correlate well, it also simulates between 20 to 400 times faster than its transistor-level counterpart. And the model can be easily adjusted to match the behaviors of actual silicon measured in the lab.”



Correlation: MacroModel vs TransistorModel

“Overall, the templates were simple to work with and very valuable amidst the challenges of multi-gigahertz design.”

Correlation - Altera Stratix GX



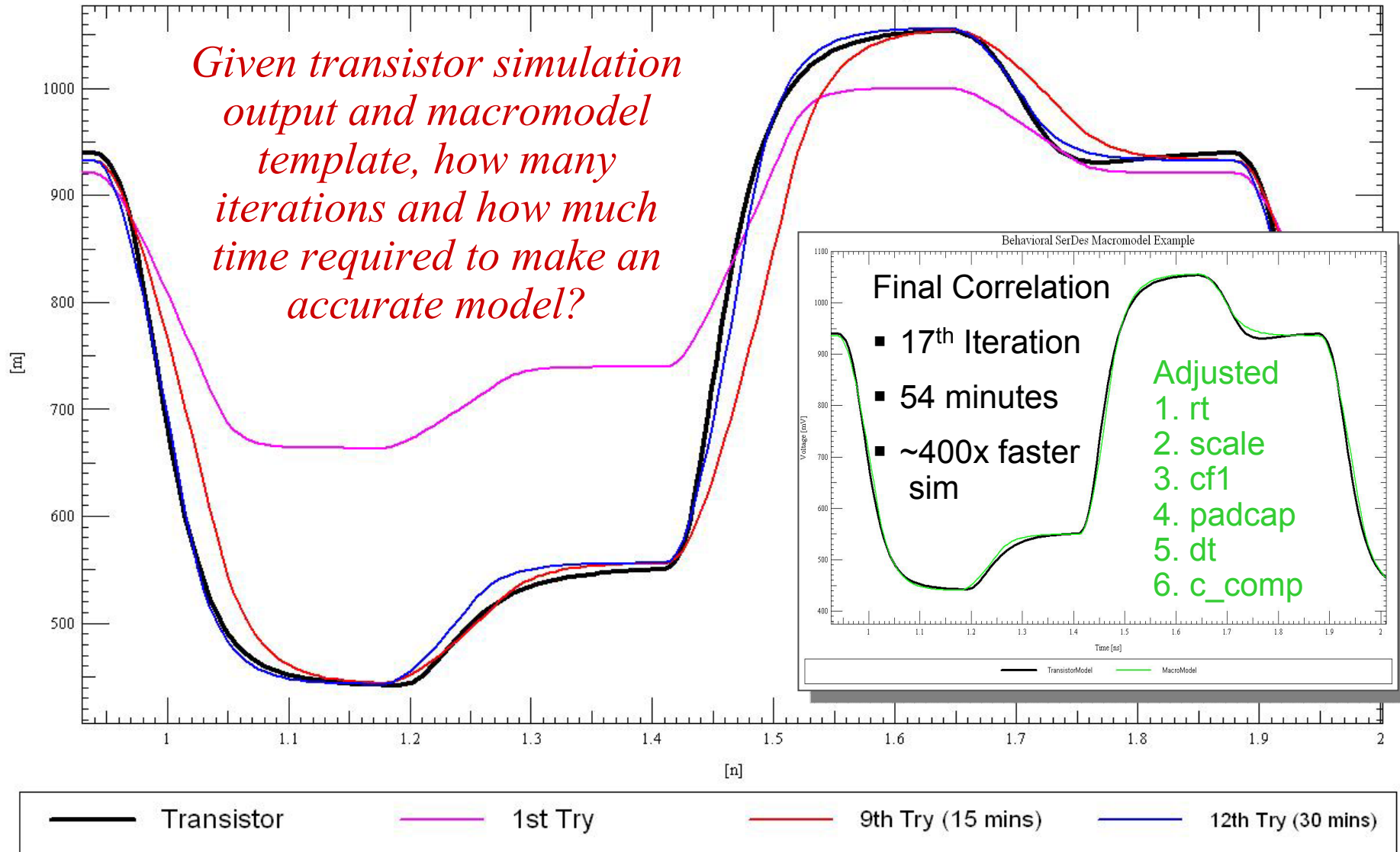
- Transistor Level Model (HSpice)
- Spice Macromodel (Cadence DML)

Transmitter output at factor=5

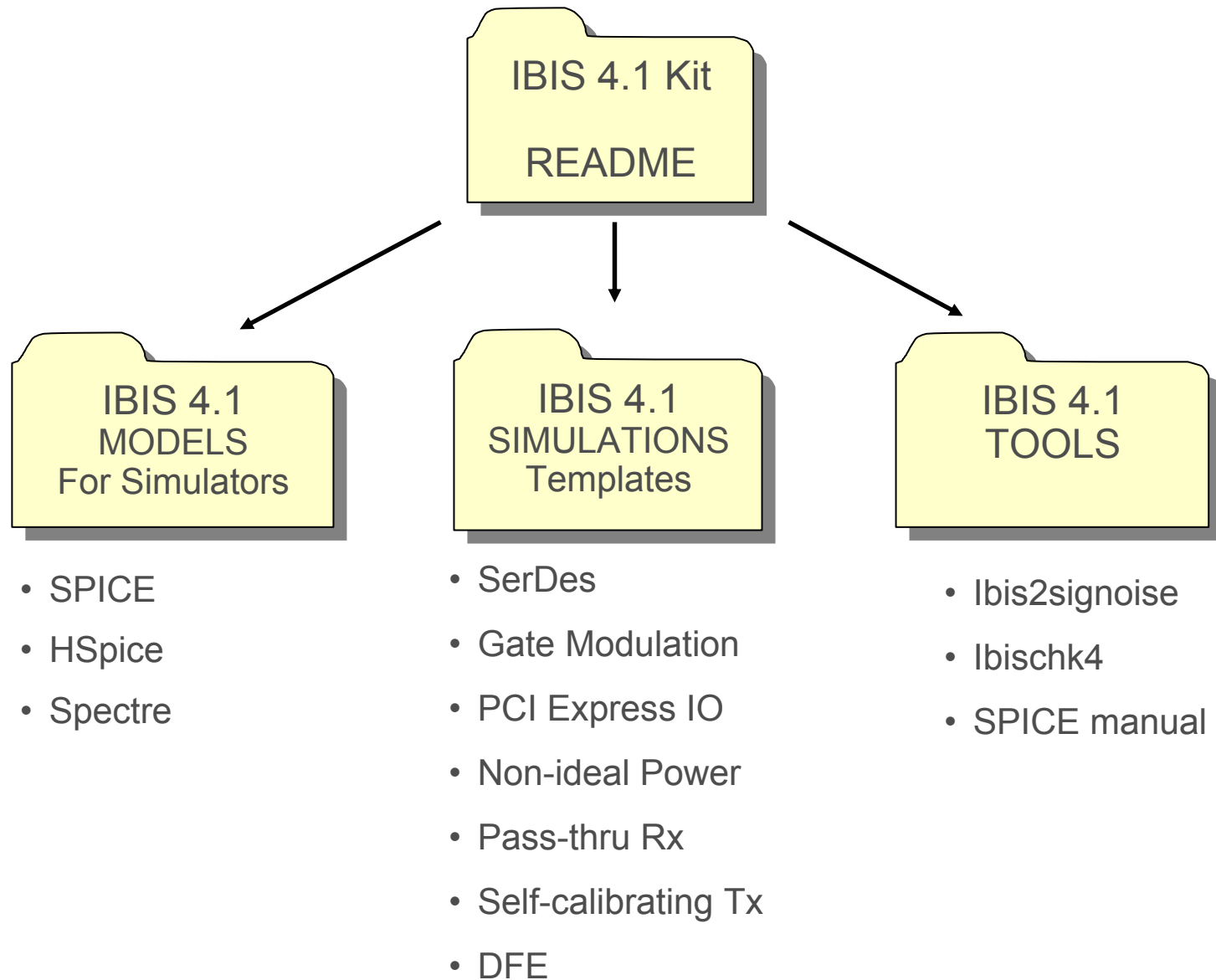
Case Study: Agere Systems 4 Gbps SerDes

Behavioral SerDes Macromodel Example

Given transistor simulation output and macromodel template, how many iterations and how much time required to make an accurate model?



Cadence IBIS 4.1 Kit





Thank You

謝謝

