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# Simulation with IBIS in Tight Timing Budget Systems


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# *Agenda*

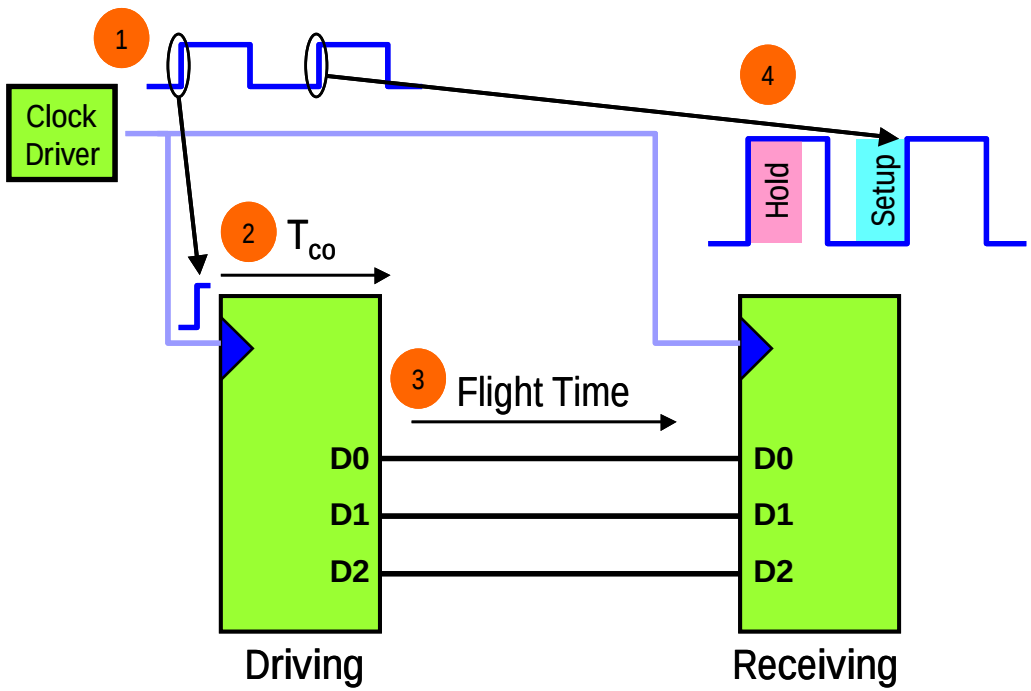
- Basis of system timing analysis
- Simulation with IBIS in tight timing budget systems
- Analysis methods

# *Timing Analysis Basis*

- **Systematic timing analysis identifies**
  - Timing topology
  - Setup and hold time margins
  - The risk of timing violations

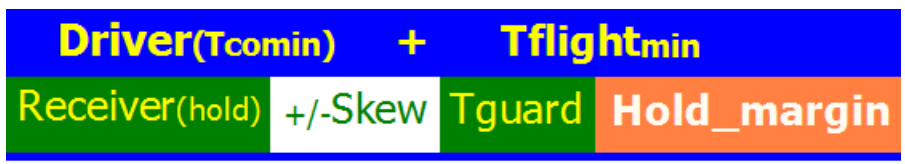
# Common-Clock Synchronous System

- **Timing topology**



# Timing Margins of CCS System


Setup_margin=Clock Period-Driver(Tcomax)-Tflightmax-Skew-Jitter-Tguard-Receiver(setup)




Hold_margin=Driver(Tcomin)+Tflightmin-Skew-Tguard-Receiver(hold)

# *Loose Timing Budget System Analysis*

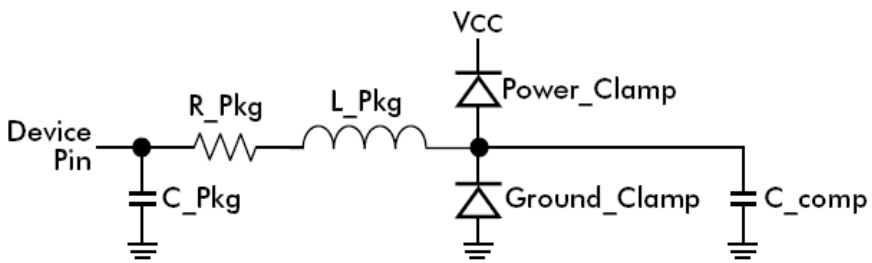
- **Definition**
- **Required inputs**
  - Timing topology
  - Component-level timing data
  - Operating clock frequency
  - Approximated flight time and guard band

# *Tight Timing Budget System Analysis*

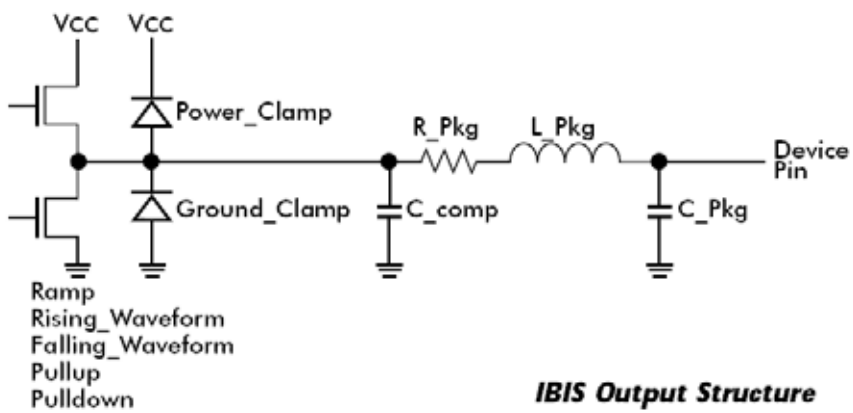
- **Definition**
- **Required inputs**
  - Timing topology
  - Component-level timing data
  - Operating clock frequency
  - *Simulation with component models is mandatory*
  - *More sophisticated numerical processing needed*

# IBIS Models Do Good Job in Simulation

- **Available**
- **Effective**




*IBIS Input Structure*

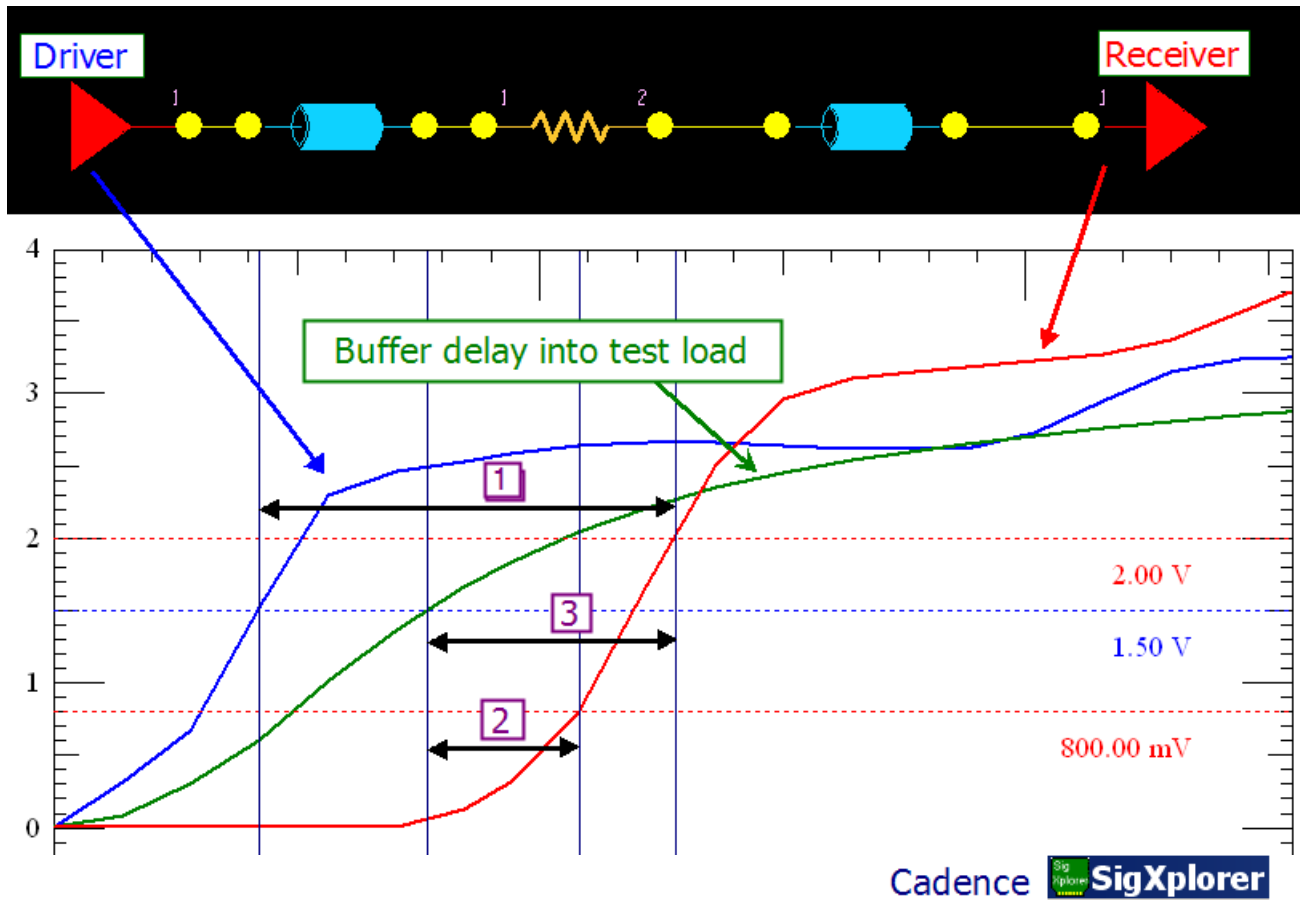



*IBIS Output Structure*

# *Flight Time*

- **Flight time vs. propagation delay**
  - Propagation delay
    - The sum of T-line delays in the path
  - Flight time
    - The time it takes the data out from the driver to settle at the receiver's input
  - For tight budget designs the flight time should be simulated with cautions

# Flight Time Simulation




- **Questions**
  - **Is delay1 flight time?**
  - **What are delay2 and delay3 ?**

# *Flight Time Simulation with IBIS*

- **Cautions**
  - Check component datasheet and IBIS model
  - Avoid double counting C_comp and load
  - Receiver thresholds

# IBIS vs. Datasheet Consistency

- **Test loads should match**

[Model] output

Model_type 3-state

Polarity Inverting

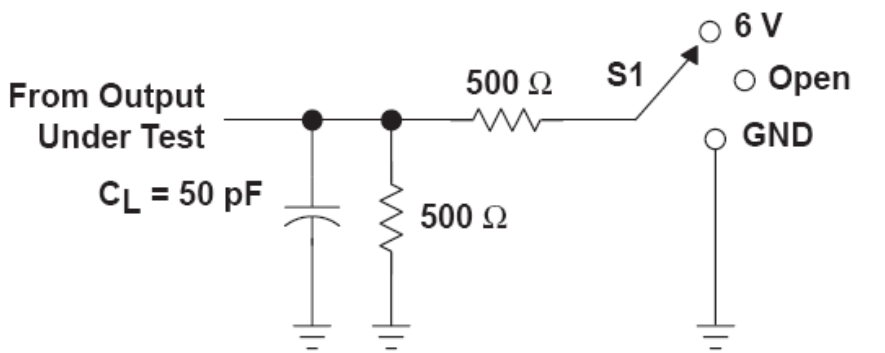
Enable Active-Low

Vmeas =1.5v

Cref =50pf

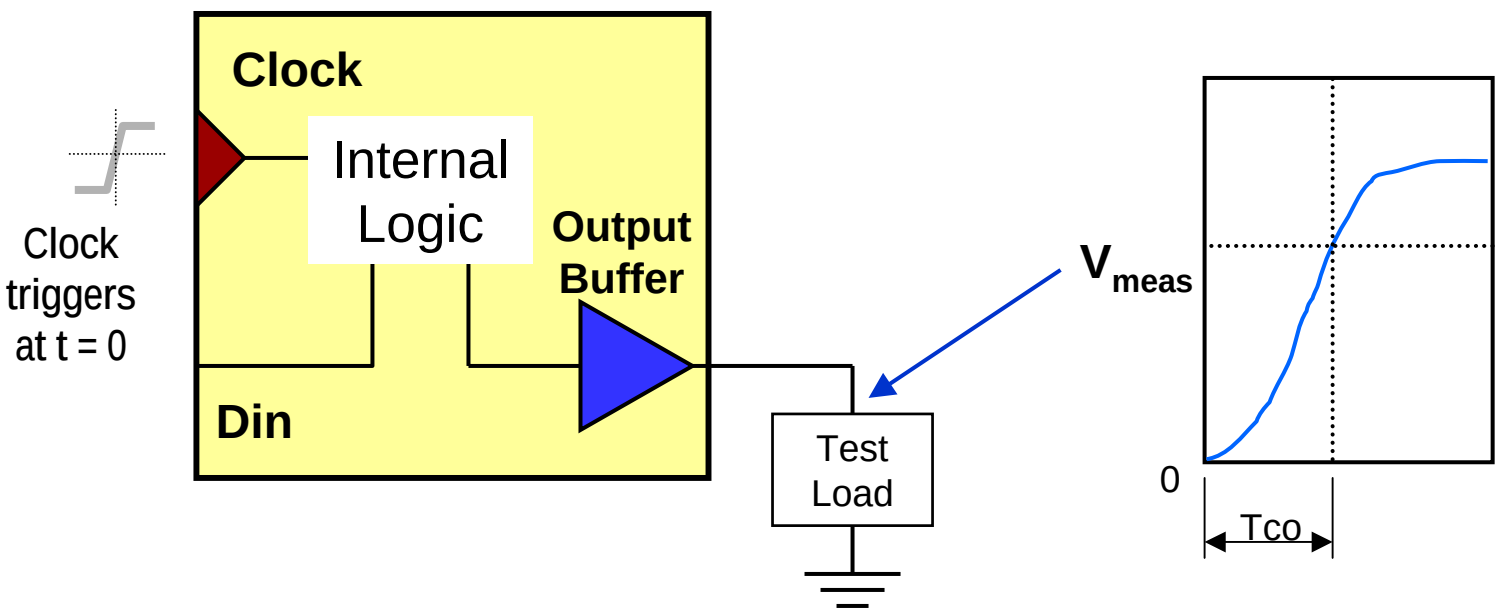
Rref = 500

Vref = 0.000




LOAD CIRCUIT In datasheet

# Tco Measurement



# *Avoid Double Counting*

- **Avoid double counting output C_comp**
- **Avoid counting both test load and load**
- **Method 1**
  - Compensate from simulated flight time
- **Method 2**
  - Subtract their effect from Tco

# *Negative Flight Time*

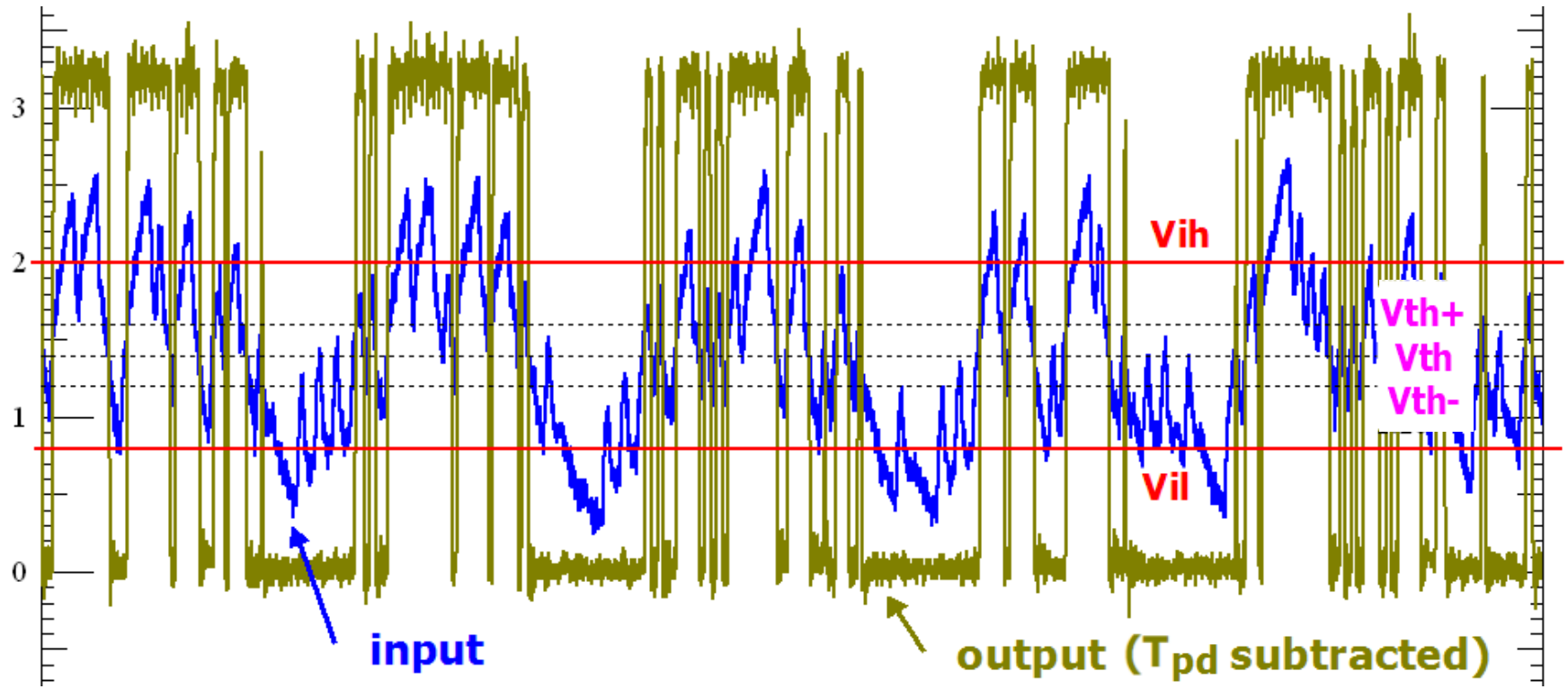
- **Negative flight time happens when**
  - Test load for Tco measurement is heavier than actual load
  - The interconnect is short

# *Include Corners in Simulation*

- **Parts behave diversely**
- **Simulate including strong and weak buffers**

# Receiver Thresholds

- **Test example**



# Receiver Thresholds

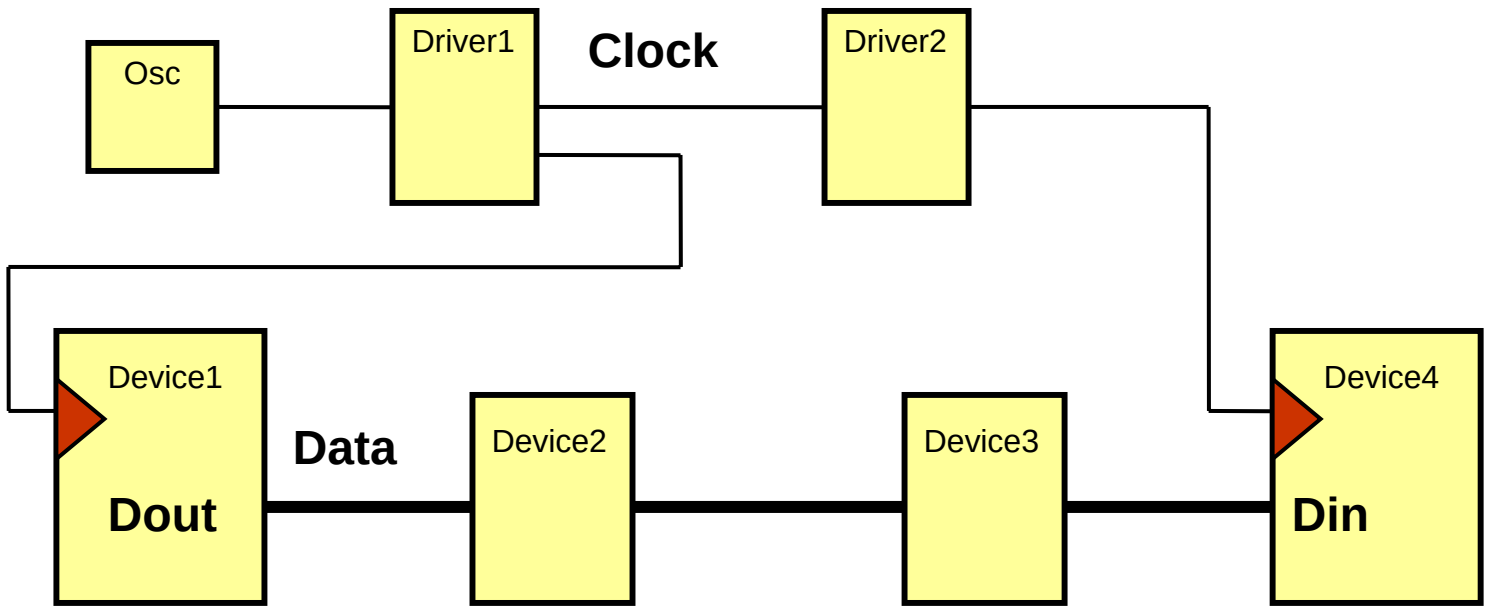
- **Use Vih and Vil as initial choice**
- **Use Vth when available**
- **IBIS Ver 4.0**
  - [Receiver Thresholds] sub-parameters
    - Vth,Vth_min,Vth_max
    - Vinh_ac,Vinl_ac, Vinh_dc,Vinl_dc
    - Tslew _ac

# Guard Band Time

- **Effects likely not included in your simulation**
  - Simultaneous switching output
    - Ver4.0 and earlier models do not include SSO in data tables
  - Crosstalk
  - Inter-symbol interference
  - Power supply noise
- **Guard band time ensures margins existence**
- **Obtained from simulation or measurements**

# Deal with Complex Topology

- **Example**



# Deal with Complex Topology

- **Adding components in path**
  - Path delay deviations increase
  - Timing margins decrease
  - Alternative analysis methods are needed to put the simulated interconnection delays together

# *Timing Analysis Methods*

- **Worst case timing analysis**
- **Statistical timing analysis**
  - Root Sum Square timing analysis
  - Monte Carlo timing analysis

# Worst Case Timing

- **Path delay**
  - Maximum worst-case path delay

$$t_{path}\max\ \text{worst - case delay} = t_p\max(\text{device 1}) + t_p\max(\text{device 2}) + t_p\max(\text{device 3}) + \cdots + t_p\max(\text{device N}) +$$
$$t_p\max(\text{interconnect1}) + t_p\max(\text{interconnect2}) + t_p\max(\text{interconnect3}) + \cdots + t_p\max(\text{interconnectN})$$

  - Minimum worst-case path delay

$$t_{path}\min\ \text{worst - case delay} = t_p\min(\text{device 1}) + t_p\min(\text{device 2}) + t_p\min(\text{device 3}) + \cdots + t_p\min(\text{device N}) +$$
$$t_p\min(\text{interconnect1}) + t_p\min(\text{interconnect2}) + t_p\min(\text{interconnect3}) + \cdots + t_p\min(\text{interconnectN})$$

# Statistical Timing Analysis(1)

- **Root sum square timing analysis**
  - Maximum RSS path delay

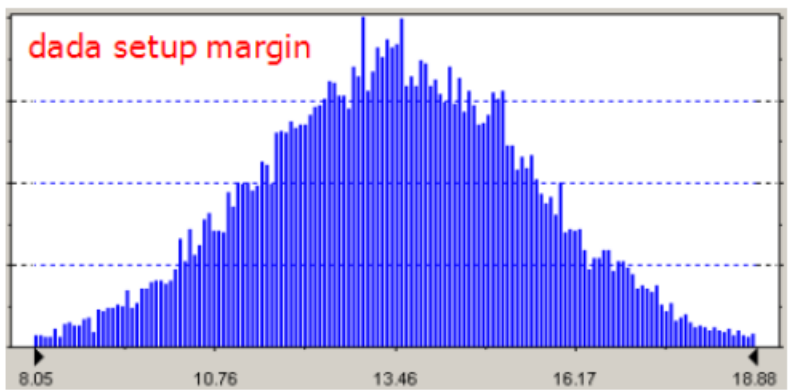
$$t_{\text{path}}\max \text{RSS delay} = t_{\text{path}}\text{typ} + \sqrt{(t_p\max 1 - t_p\text{typ}1)^2 + \cdots + (t_p\max N - t_p\text{typ}N)^2}$$

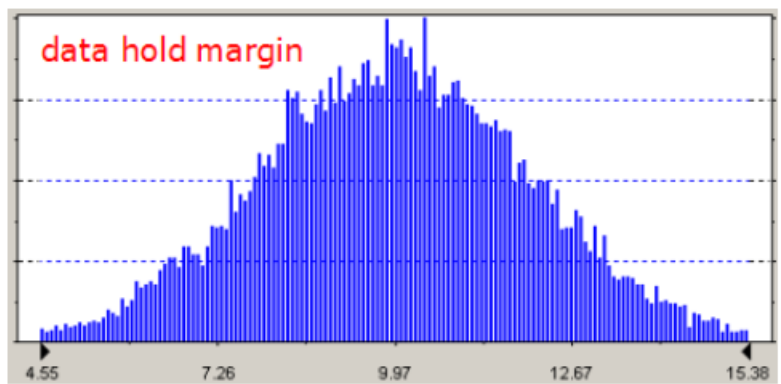
  - Minimum RSS path delay

$$t_{\text{path}}\min \text{RSS delay} = t_{\text{path}}\text{typ} - \sqrt{(t_p\text{typ}1 - t_p\min 1)^2 + \cdots + (t_p\text{typ}N - t_p\min N)^2}$$

# Statistical Timing Analysis(2)

- **Monte Carlo timing analysis**
  - By random sampling delay values determines the timing attribute probability distribution



# Conclusion

- **Cautions with simulation in tight timing budget system**
  - Check component test load
  - Avoid double counting
  - Receiver thresholds
- **Simulated results analysis methods**
  - Worst case
  - RSS
  - Monte Carlo

# References:


James E. Buchanan ,"***Signal and Power Integrity in Digital Systems (TTL, CMOS, & BiCMOS)***", McGraw-Hill Inc., ISBN 0-07-008734-2

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Todd Westerhoff ,"***Closing the loop between timing analysis and signal integrity***" Cadence Design System