IBIS and Behavioral Modeling

Michael Mirmak
Intel Corporation
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迈克尔.莫马克
英特尔公司
IBIS 委员会主席

亚洲 **IBIS** 技术研讨会
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What is IBIS?

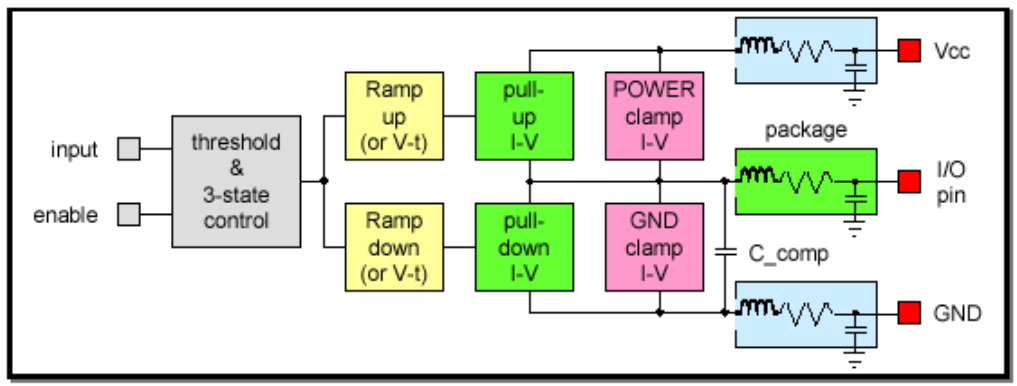
- IBIS* (I/O Buffer Information Specification)
  - A standard format for expressing I/O buffer electrical behavior plus component pin and package information
  - ANSI/EIA* 656-A, IEC* 62014

Most buffers expressed through

- Current vs. Voltage (I-V tables)
- Voltage vs. Time (V-T tables)
- Buffer capacitance (C_comp)

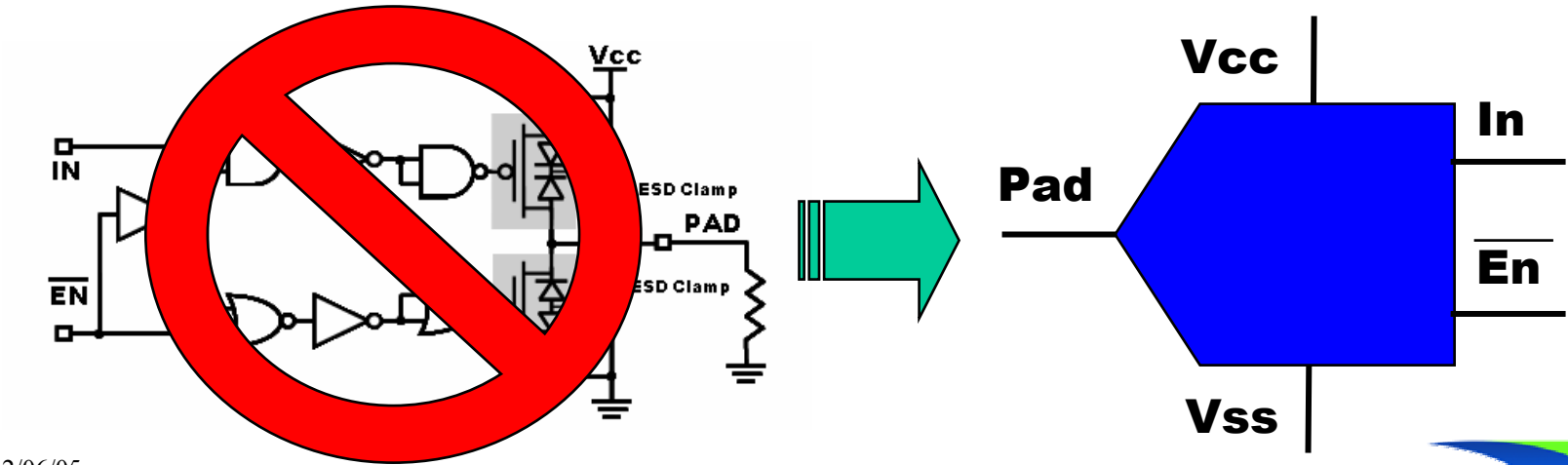
Components include

- Pin assignments and names
- Package information



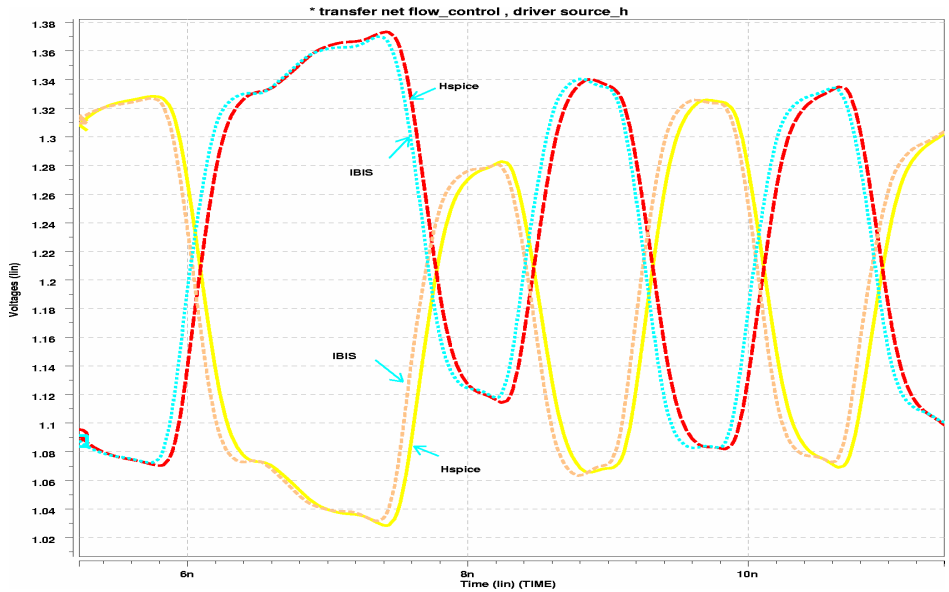
Behavioral Modeling

- IBIS is only one type of behavioral model
  - Others include:
    - ICM* (IBIS Interconnect Modeling Specification)
    - IMIC* (I/O Model for Integrated Circuits, JEITA* ED-5302)
    - ICEM* (Integrated Circuit Electrical Model, IEC 62014-3)
    - VHDL-AMS* (IEEE* 1076.1)
    - Verilog-AMS* (Accelera*)
- Behavioral models replace internal design information with *observations of electrical ports or terminals*



An Example

- IBIS, as a behavioral modeling standard, offers
  - Protection of internal design information
  - Availability under multiple software tools
  - Increases in simulation speed over transistor-based models
- IBIS behavioral vs. transistor-based models
  - For a serial-differential design, IBIS can be 100 times faster!
  - Careful model creation preserves accuracy



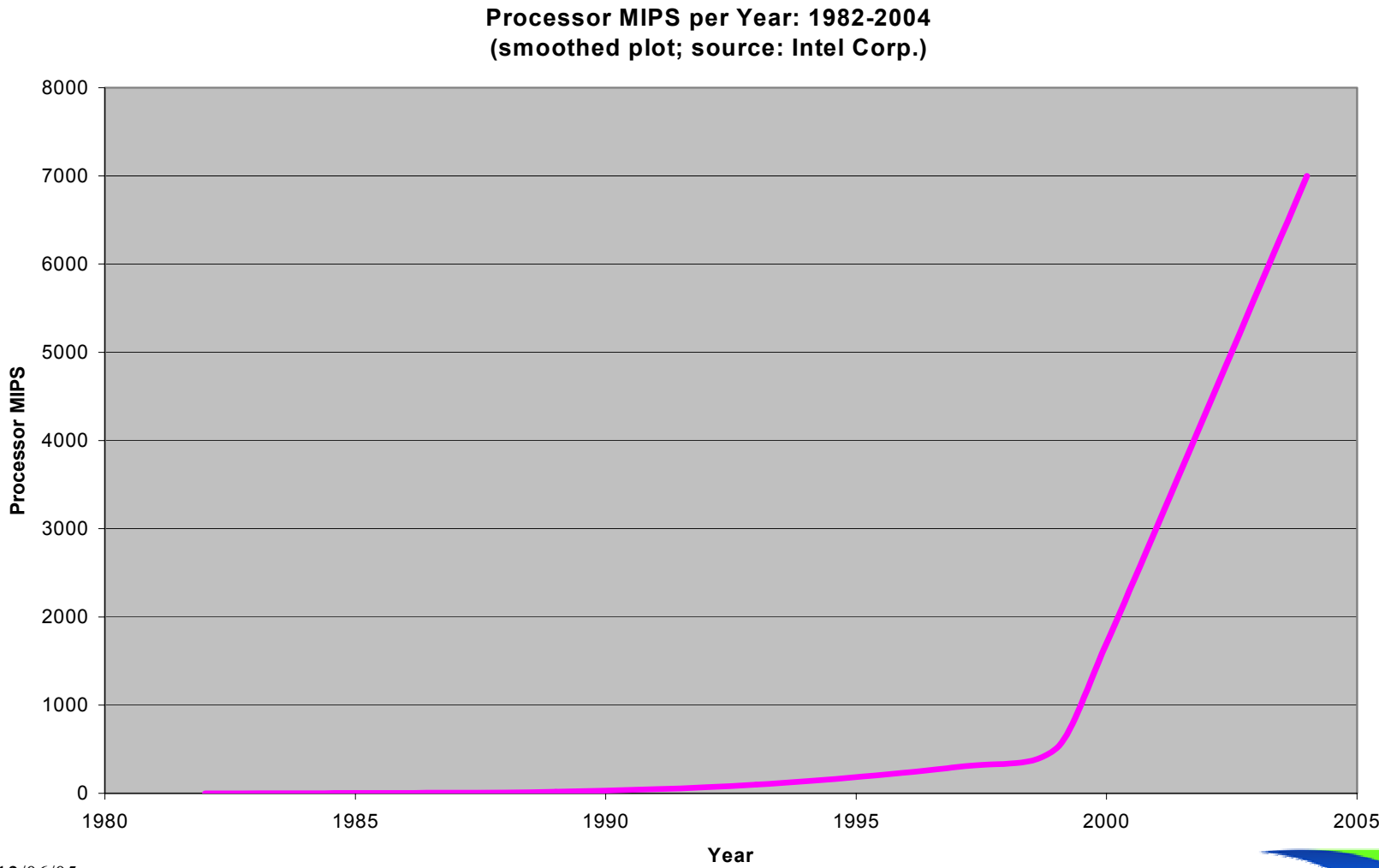
IBIS vs. SPICE*
(time-shifted to show correlation)

Image from SiSoft*:
IBIS Models at 2.5 GHz and Beyond; used with permission

Speed quotation from Multi-Gigabit SerDes System Level Analysis... by Huq/Dodd; used with permission

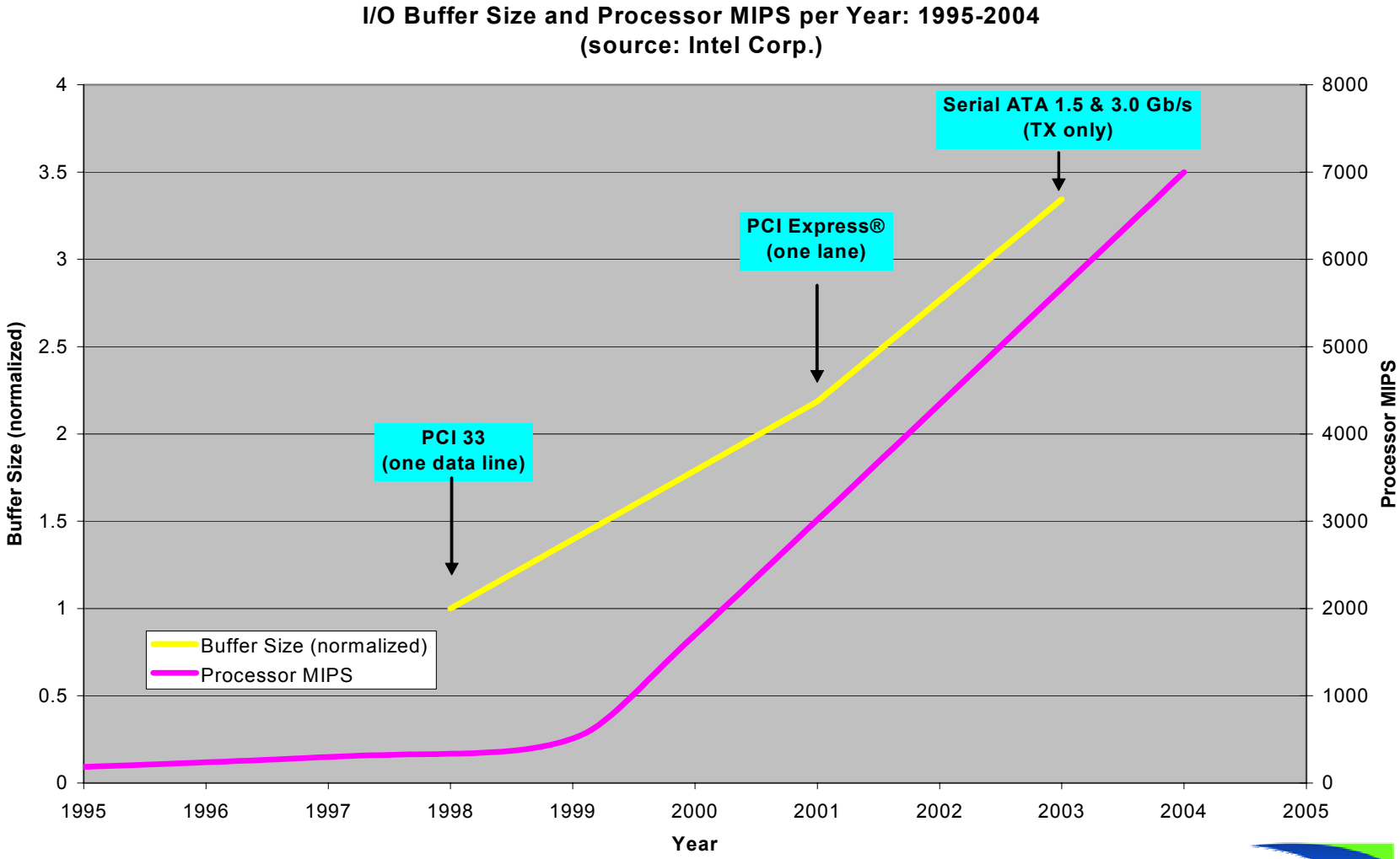
The Future of Modeling

- **Why behavioral instead of transistor-based models?**

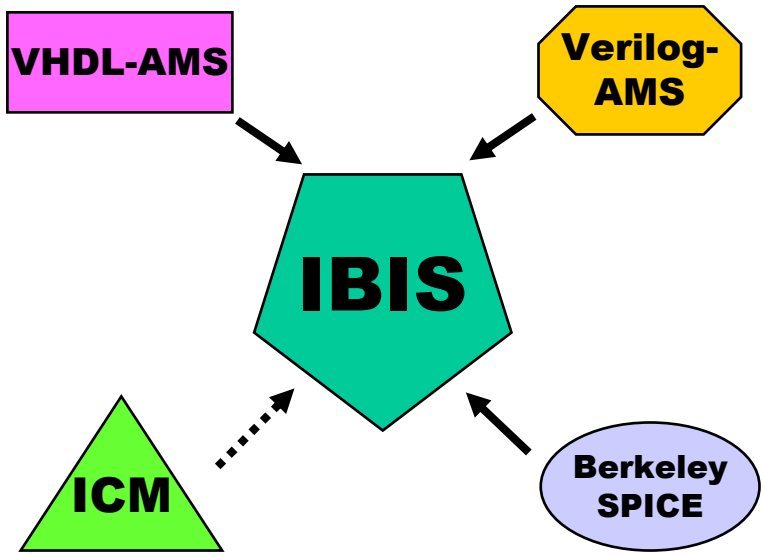


The Future of Modeling

- **Buffer complexity is keeping pace with processor power!**



Supporting Future Designs



- **Buffers becoming more complex**
  - Size is ***tracking processing power***
- **New designs need more analysis**
  - Power delivery and switching noise
  - Pre-emphasis, active feedback and compensation
- **IBIS expanding to address needs**
  - New links to VHDL-AMS, Verilog-AMS, Berkeley SPICE*
  - Enable equations within IBIS
  - Links to ICM are in development

The industry needs behavioral modeling for today and tomorrow

IBIS provides a standard, unified solution for behavioral buffer modeling

You Are Invited!

- **IBIS Welcomes Worldwide Participation!**

Specifications
- IBIS: http://www.eda.org/ibis/ver4.1/
- ICM: http://www.eda.org/ibis/icm_ver1.1/

Training
- Including IBIS history and tutorials
- http://www.eda.org/ibis/training/

IBIS Cookbook
- Features explained plainly
- http://www.eda.org/ibis/cookbook/

Task Groups
- Futures, Macromodel Library, Quality
- Free Model Review service!

http://www.eigroup.org/ibis/
http://www.eda.org/ibis/

IBIS appreciates your input and support!

BACKUP

A Related Specification: ICM

- ICM = IBIS Interconnect Modeling Specification
  - Standard text format for interconnect modeling data
  - "Interconnect" can be connector, cable, PCB traces or even an IC package
    - *Defines structure as path between "sections"*
    - *Defines the electrical data for each section*