IBIS Models for DDR2 Analysis

Asian IBIS Summit 2005

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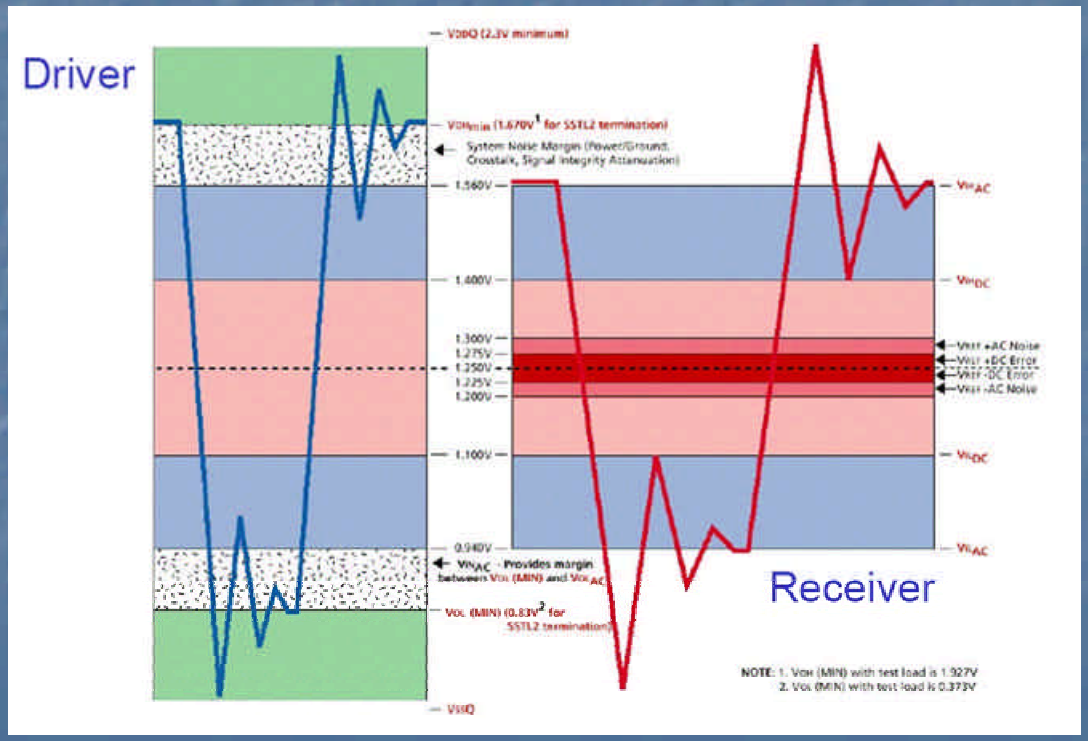
DDR Overview: *Theory of Operation*

- Data captured on both clock edges
- Data (DQ) driven source synchronously with strobe (DQS)
- Proper source sync operation requires two conditions:
  - DQS positioned to meet data Setup/Hold requirements
  - Fixed relationship between CK and DQS must be maintained
- DDR1 Clock (CK) range from 100MHz to 200MHz
  - DQ 200Mbs to 400Mbs
- DDR2 Clock (CK) range from 200MHz to 400MHz
  - DQ 400Mbs to 800Mbs

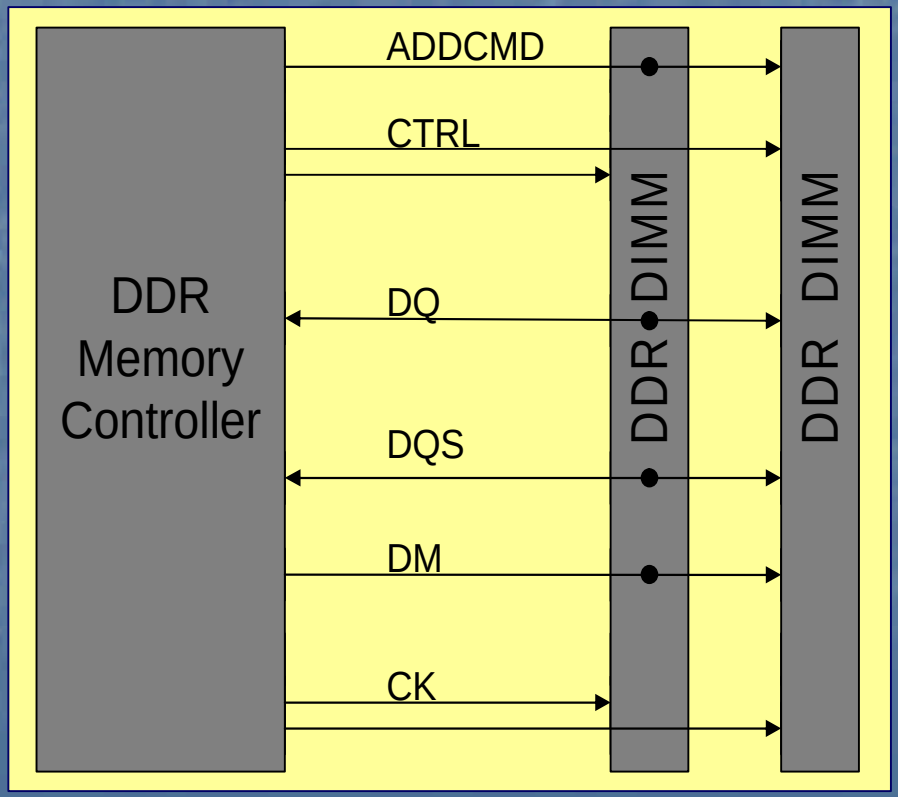
DDR Overview: *Theory of Operation*

- DDR1: 2.5V SSTL
- DDR2: 1.8V SSTL
- SSTL introduces concept of AC and DC levels



DDR System Configurations

- DDR1: One to four memory modules
- DDR2: One or Two memory modules
- Memory Modules
  - Registered and Unbuffered
  - 4 to 18 memory device



DDR2 Enhancements
Moving beyond DDR1

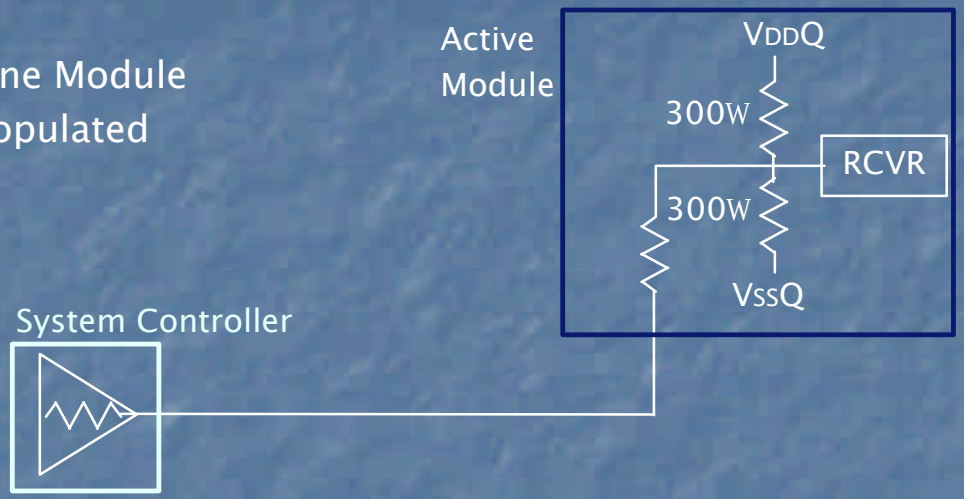
- Technology
  - FBGA Package
  - Reduced Supply Voltage (1.8V)
  - Optional Differential DQS
  - Improved DIMM routing Topologies
  - Improved Load Balancing
  - **On-Die Termination (ODT)**
    - **Increases number of combinations to simulate**
  - **Slew-Rate Derating**
    - **Modifies Setup/Hold requirements**

On-Die Termination

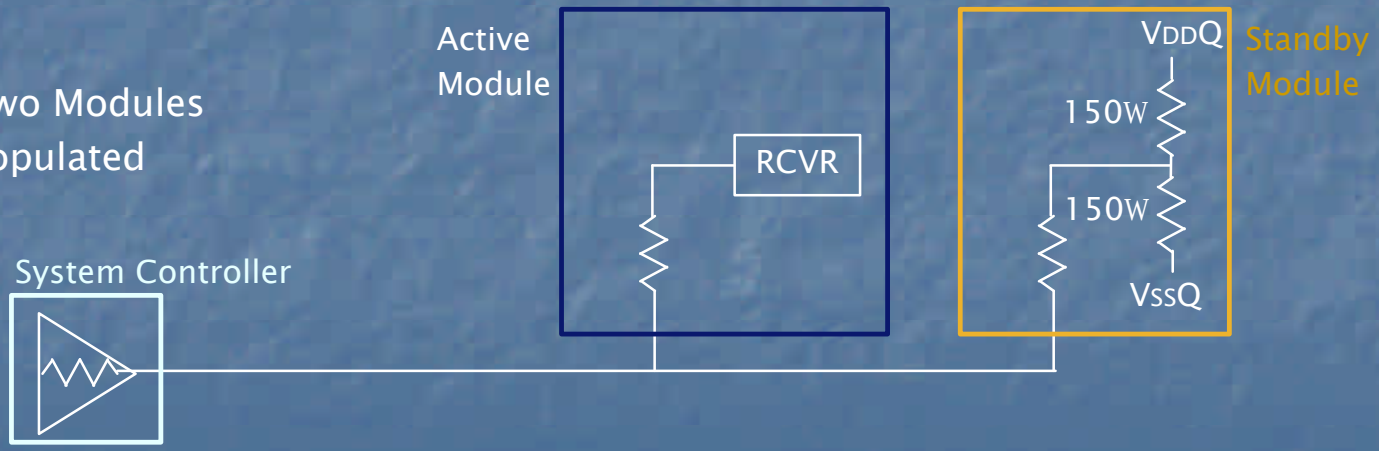
- DQ, DM, DQS signals only
- Memory controller defined
  - Transfer by transfer basis
  - Dependent on loading configuration
- Multiple values: 50, 75,150, and “off”
- Reduces PCB component count
- Simplifies system implementation
- Increases analysis complexity

Data Write ODT Configurations

One Module Populated

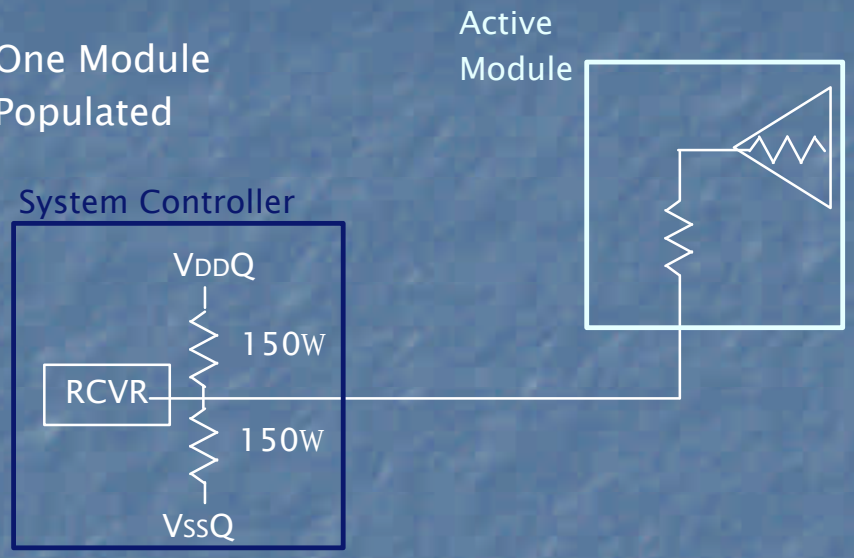


Two Modules Populated

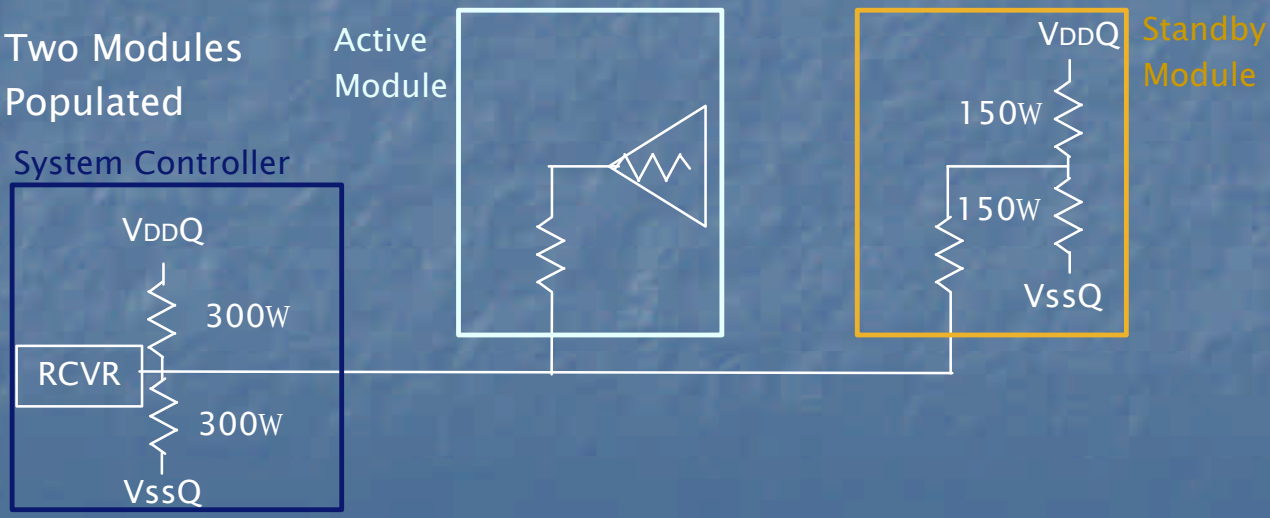


Data Read Configurations

One Module Populated



Two Modules Populated



DDR2 I/O Buffer Modeling Challenges

Spice vs. IBIS

- SPICE models
  - Accurate, allow for PVT variation, over-clockable
  - Slow simulation time
- IBIS models
  - Can closely match SPICE models for accuracy
  - Higher simulation performance
  - Multiple simulator support, readily available

DDR2 I/O Buffer Modeling Challenges

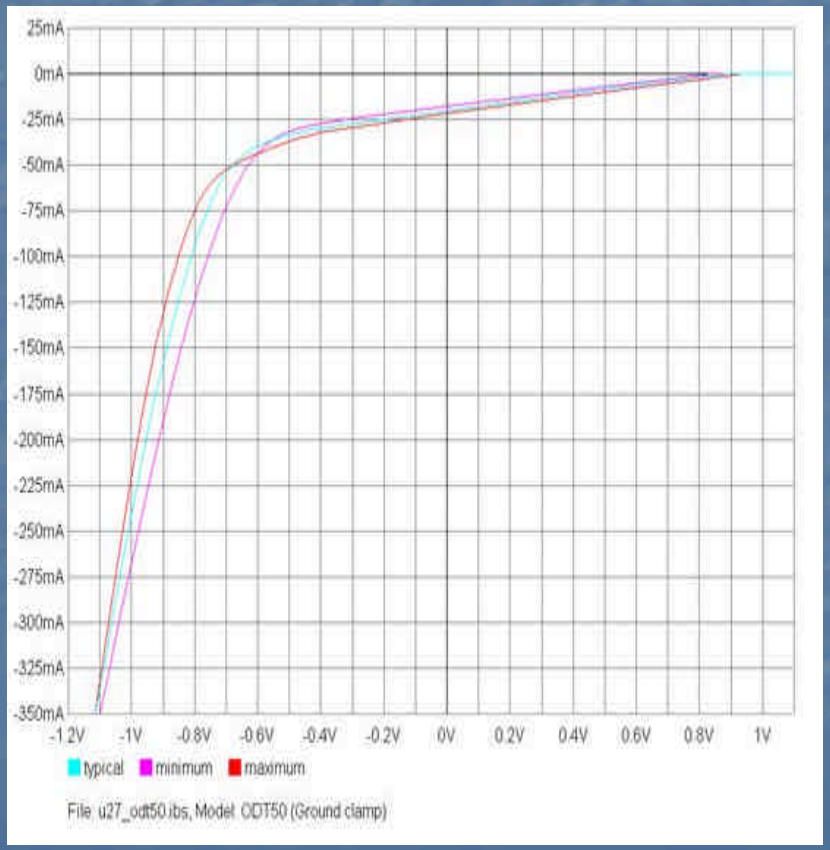
ODT Modeling in IBIS

- Three options for ODT modeling
  - 6 separate I-V curves
    - Normal [Pullup], [Pulldown], [POWER Clamp] and [GND Clamp] tables
    - ODT I-V curves included as [Submodel] tables
    - [Submodel] usage creates portability issues
  - Separate receive ODT-enabled model
    - Requires switching in of separate model
    - Increases complexity of simulation
    - Separate simulations for every case
  - 4 I-V curve model with ODT enabled in receive mode
    - Works well, but makes IBIS [Pullup] and [Pulldown] non-monotonic
      - This is OK because sum of [Pullup] and [Pulldown] with Clamp curves is monotonic

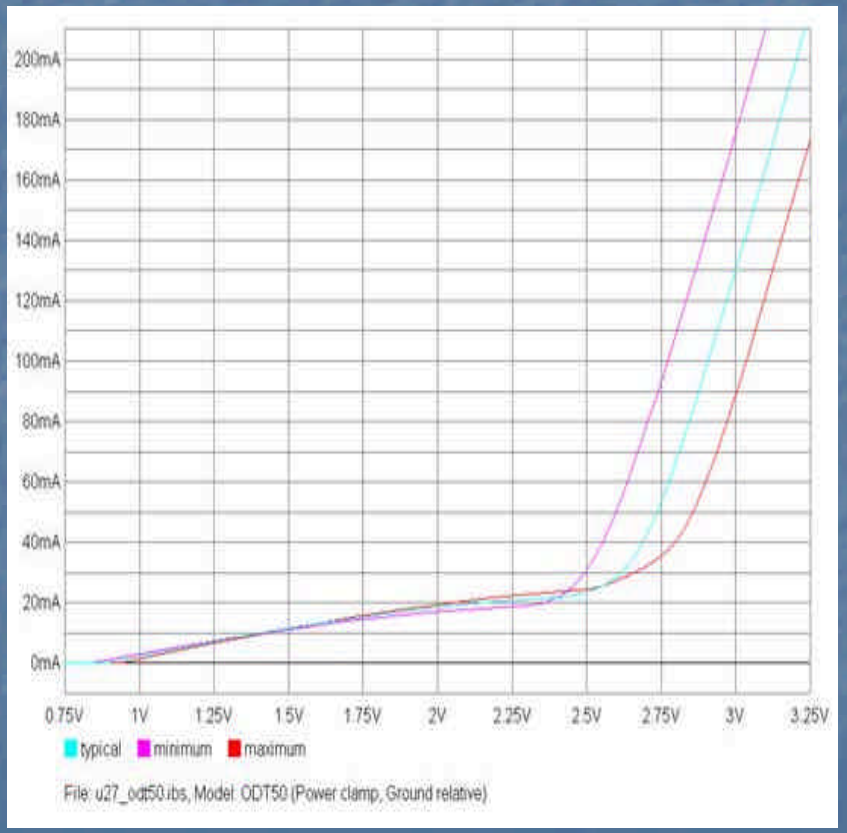
DDR2 I/O Buffer Modeling Challenges

ODT Modeling in IBIS – Thevenin ODT approach

50 O ODT model [GND Clamp]



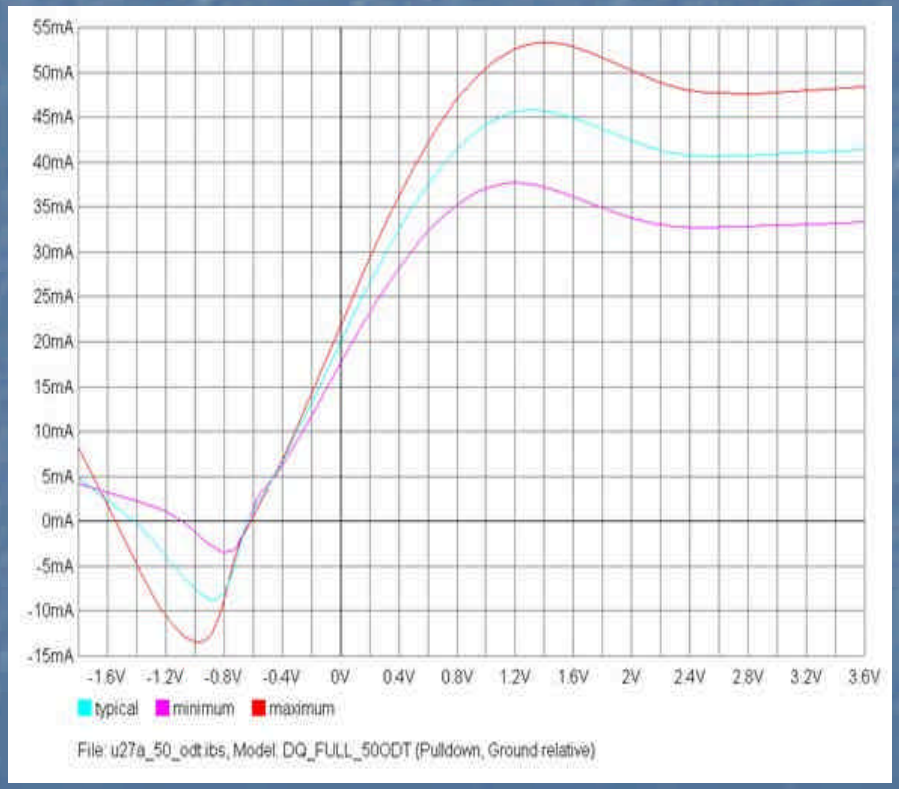
50 O ODT model [POWER Clamp]



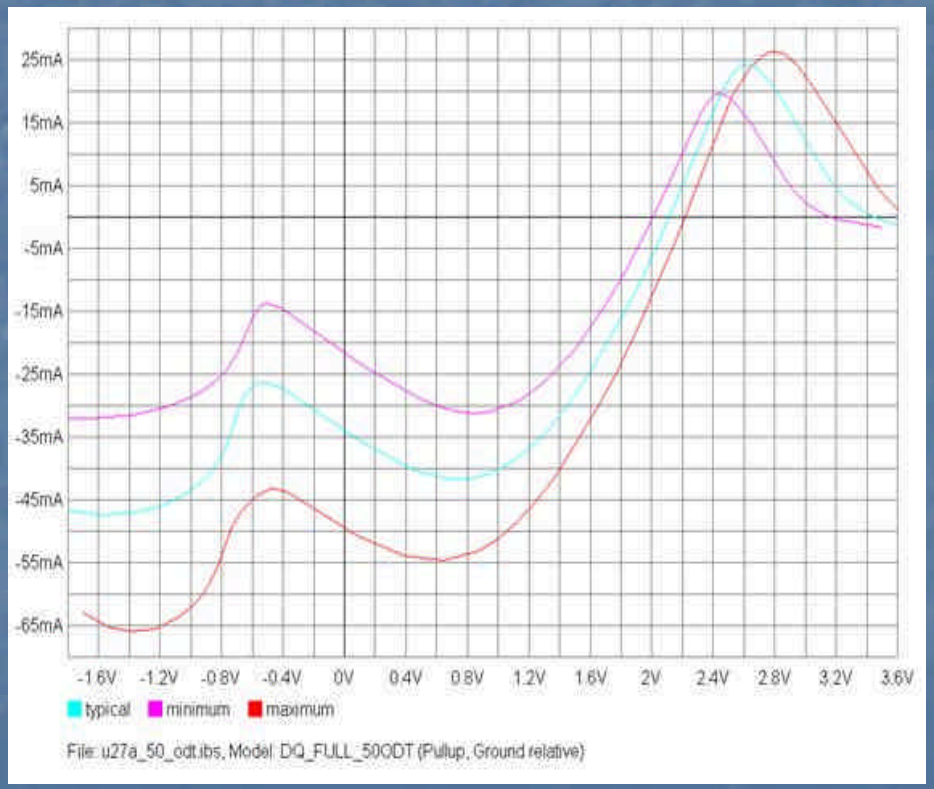
DDR2 I/O Buffer Modeling Challenges

ODT modeling in IBIS

[Pulldown] with 50 O ODT characteristics subtracted



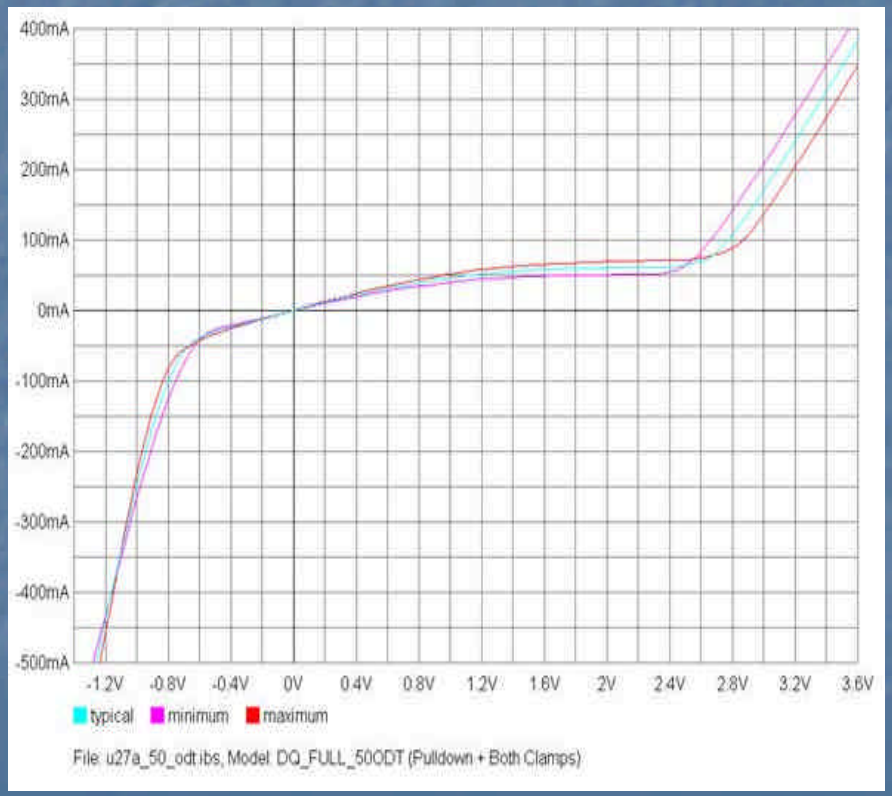
[Pullup] with 50 O ODT characteristics subtracted



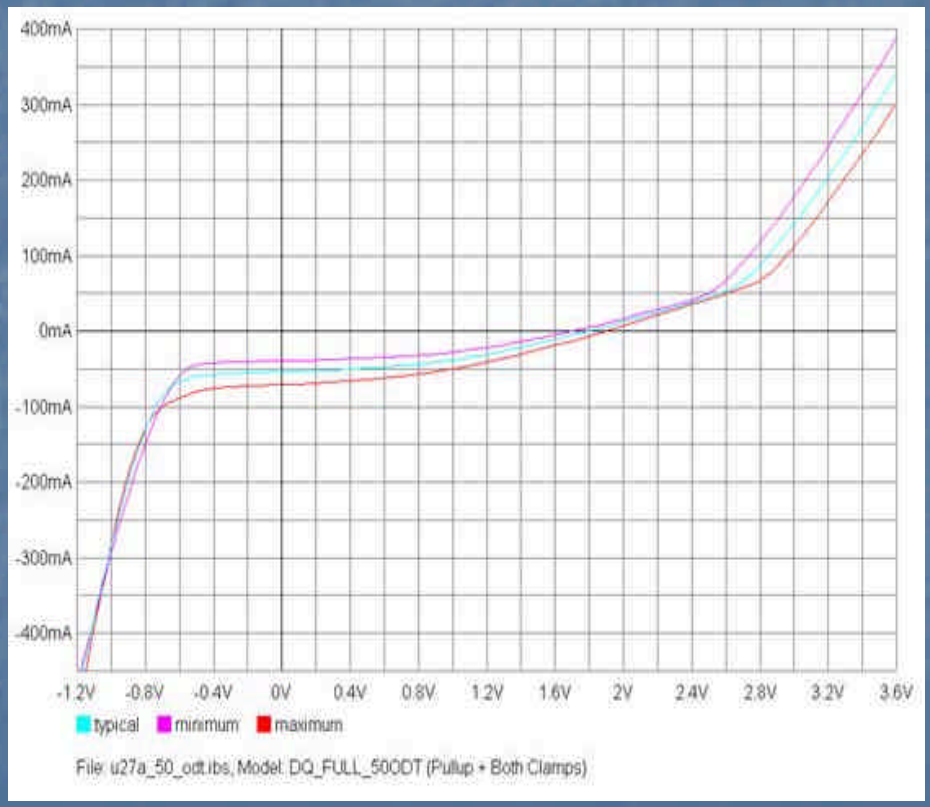
DDR2 I/O Buffer Modeling Challenges

ODT modeling in IBIS

[Pulldown] combined with [* Clamp] characteristics

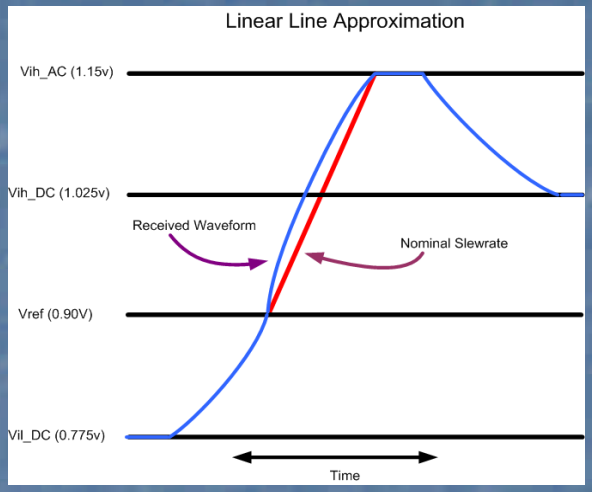


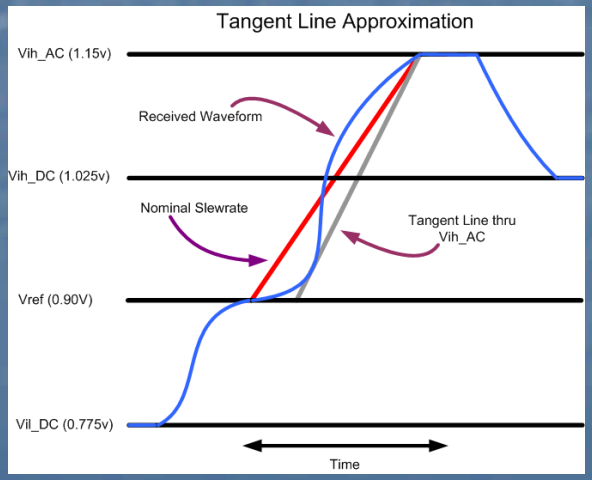
[Pullup] combined with [* Clamp] characteristics



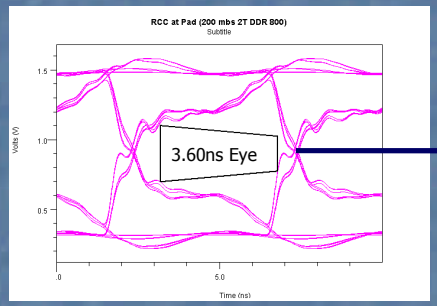
Future Considerations for IBIS

Slew-Rate De-Rating Tables



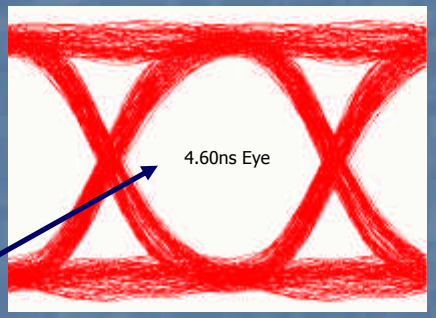


- EYE At Device PAD
  Simulated Result

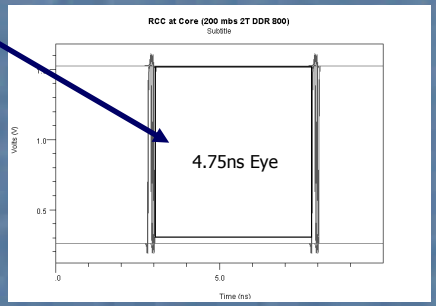


Receiver

- Virtual Eye at Receiver
  Computed Result



- Eye at Receiver Output
  Simulated Result



Thank You!