Power Delivery System, Signal Return Path, and Simultaneous Switching Output Analysis Guidelines

Asia IBIS Summit
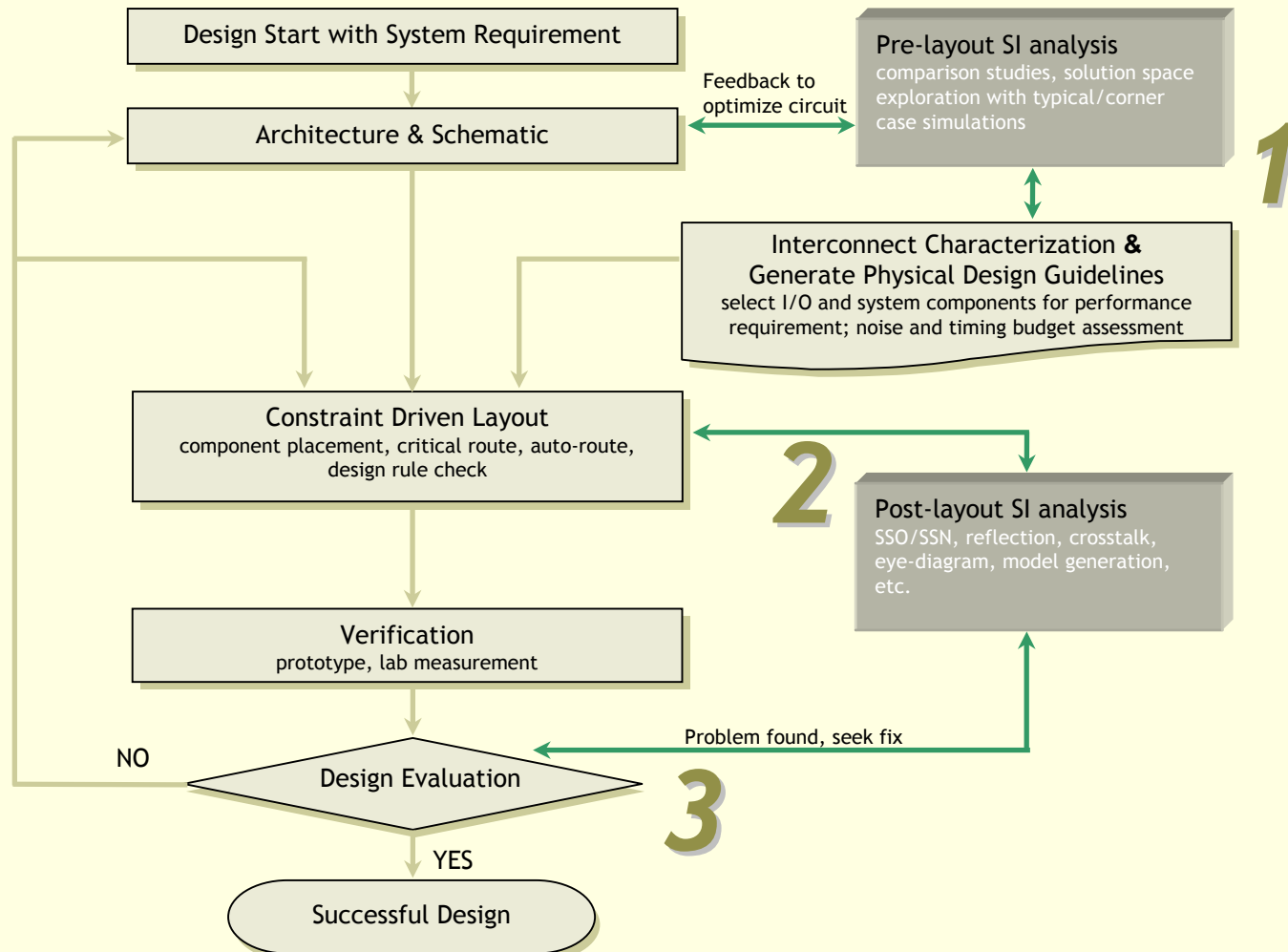
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Design Flow

Signal and Power Integrity Analysis is Performed in Each Stage

Design Start with System Requirement

Architecture & Schematic

Constraint Driven Layout
component placement, critical route, auto-route, design rule check

Verification
prototype, lab measurement

Design Evaluation

Successful Design

Feedback to optimize circuit

Pre-layout SI analysis
comparison studies, solution space exploration with typical/corner case simulations

1

Interconnect Characterization & Generate Physical Design Guidelines
select I/O and system components for performance requirement; noise and timing budget assessment

2

Post-layout SI analysis
SSO/SSN, reflection, crosstalk, eye-diagram, model generation, etc.

3

Problem found, seek fix

NO

YES

Enhanced Work Flow – Stage *1*

Pre-layout stage — generate high speed design guidelines

1. PDS design guidelines
   - Stackup what-if
   - Copper weight determination
   - Decap placement for P/G current
   - VRM sense line optimization

2. Signal return path guidelines
   - Via rules for layer transitions
   - Choose signal layer references
   - Crossing split-planes warning
   - Decap placement for enhancing signal return paths

3. SSO guidelines
   - Timing impact evaluation, SSO push-out timing budget
   - False switching prevention, victim nets (stuck-high, stuck-low), noise amplitude budget
   - Bus scheduling and driver slew rate control
   - Decap placement to reduce SSO noise

4. EMI early prevention guidelines
   - Via stitching rules
   - Stackup variations
   - Retreated plane rule
   - Power island/ring, mix-signal isolation guide
   - Radiation harmonics vs. P/G resonant frequencies correlation guide

Enhanced Work Flow – Stage 2

Post-layout stage — verification, design rule check, constraint management

1. PDS design check
   - Identify over- and under-voltage conditions for all devices on the distribution
   - Pinpoint insufficient routing (neckdowns) that causes excessive voltage drop
   - Locate current distribution "hot spots" that introduce unnecessary thermal stress
   - Identify via, bump, and ball currents above/below user-specified limits
   - Verify target impedance is met

2. SSO Simulation
   - Worst corner cases, even/odd mode switching, maximum delay, skew, over/under shoot, ringback
   - Eye-diagrams and pseudo-random bit streams (PRBS)

3. Decap Optimization
   - Decap number reduction - remove extra components to save routing space, cost and enhance product reliability
   - Decap value adjustment – address resonant frequencies

4. Model generation – deliver to other groups, or use in system-level simulations
   - Core power system model
   - I/O and return path modeling — using S-parameter models to capture signal distribution system and power distribution system interactions
   - IR drop DC circuit model

Enhanced Work Flow – Stage *3*

Problem resolution stage — evaluate design change options to reduce re-spin

1. PDS structure options
   - Add more decaps
   - Reduce pwr/gnd plane separation
   - Add more plane area (interplane capacitance)
   - Add more P/G shorting vias
   - Convert signal pin to P/G pin – e.g. FPGA footprint
2. Signal return path options
   - Reduce via transitions
   - Eliminate reference plane changes
   - Add decap across plane splits
   - Change signal vs. P/G ratio and distribution pattern, add more return vias or decaps
3. SSO options
   - Change driver slew rate and switching parameters
   - Add decaps to reduce SSO noise
4. EMI options
   - Add stitching vias near board edges
   - Adjust power island/ring
   - Add decaps to adjust radiation harmonics and P/G resonant frequencies

Delta-i Noise Simulation and Decoupling Capacitor Placement

Spatial Distribution of Power / Ground Noise on a PCB

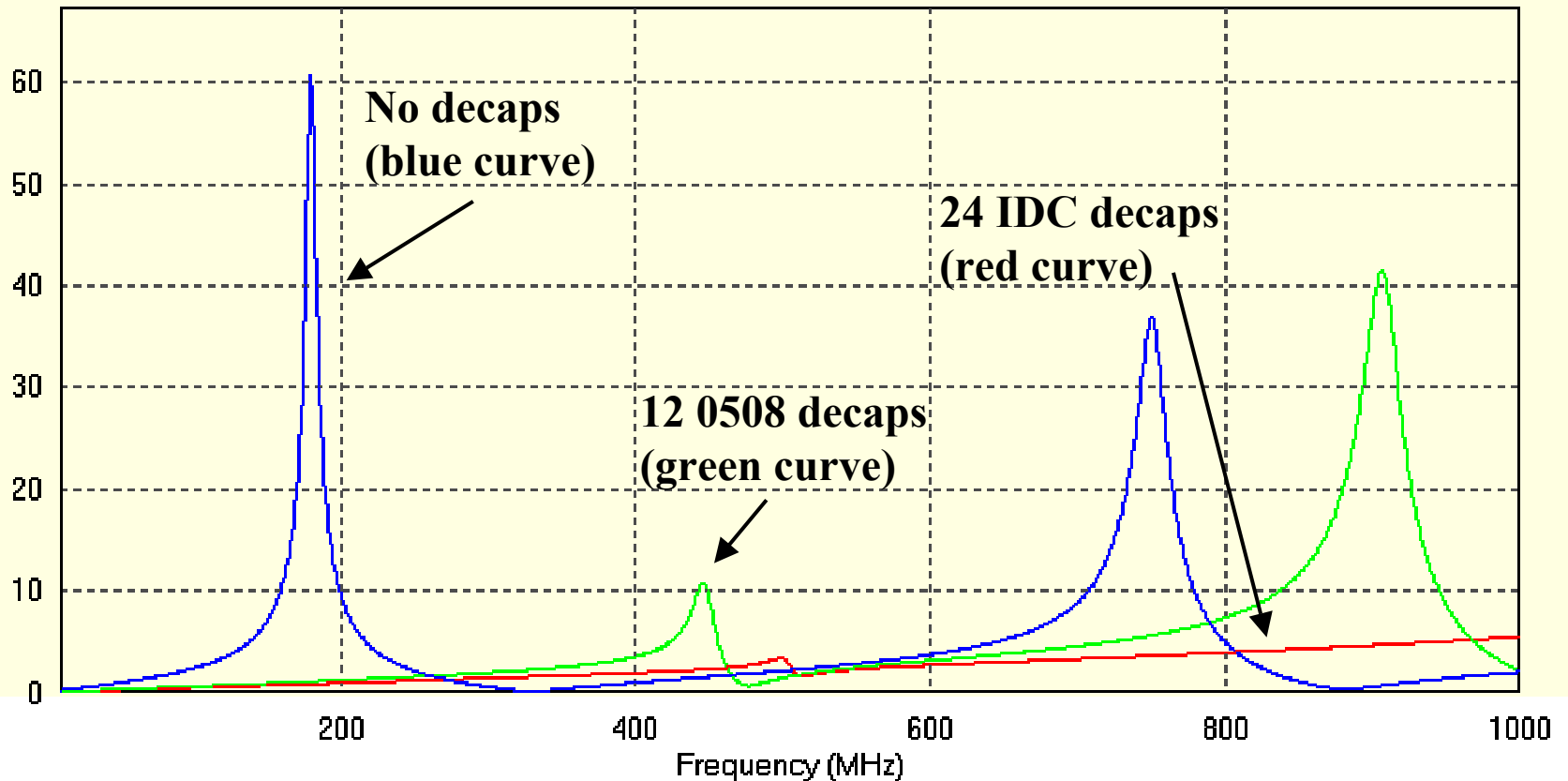No decaps

10 decaps placed

23 decaps placed
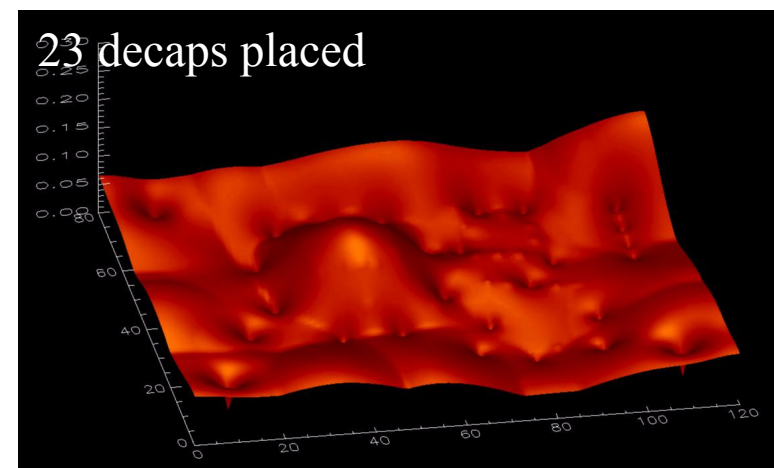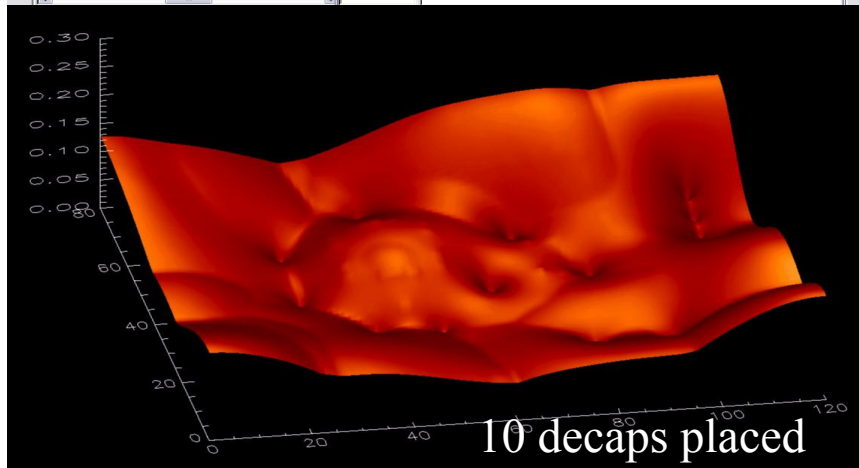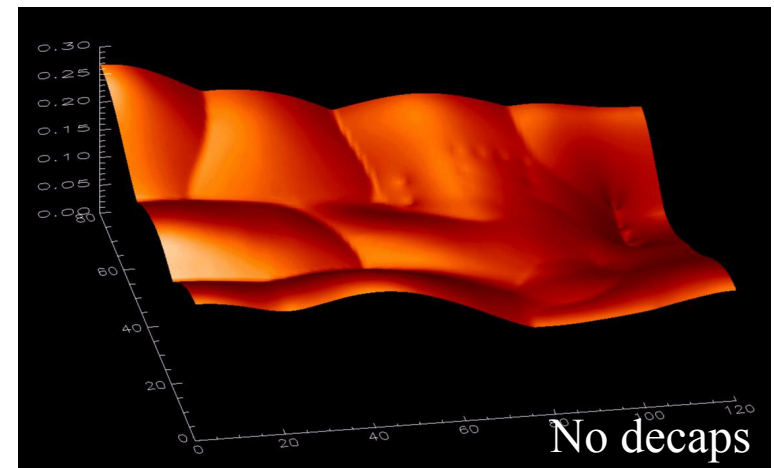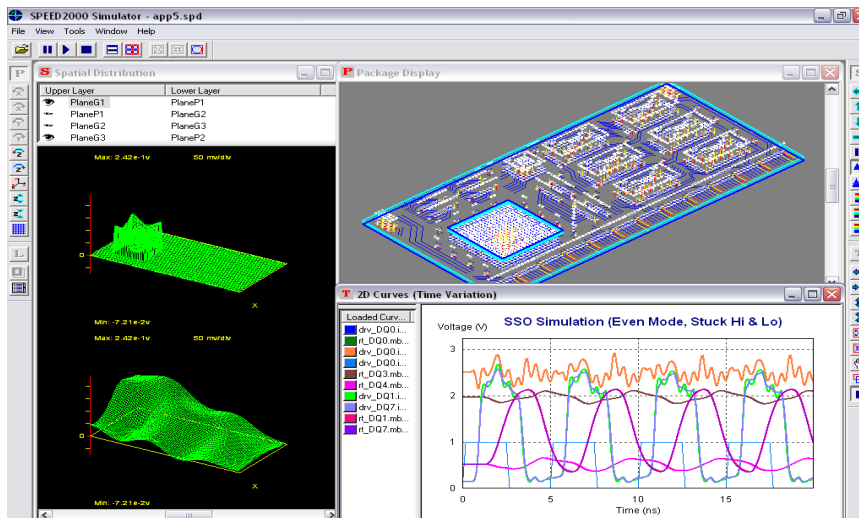
Power / Ground Impedance Extraction
PCB impedance at one location; number of decoupling caps is varied

Objective – eliminate/reduce impedance spikes within the frequency range of interest

Amplitude (Ohm)

No decaps (blue curve)

24 IDC decaps (red curve)

12 0508 decaps (green curve)

Frequency (MHz)

7

Optimize Decoupling Capacitor Selection and Placement for the Entire Distribution

- **Identify impedance "hot spots"**
    - Board location
    - Target frequency

- **Place decoupling capacitors in areas exceeding target impedance**

- **Select ideal component values**

- **Analyze power / ground resonance**

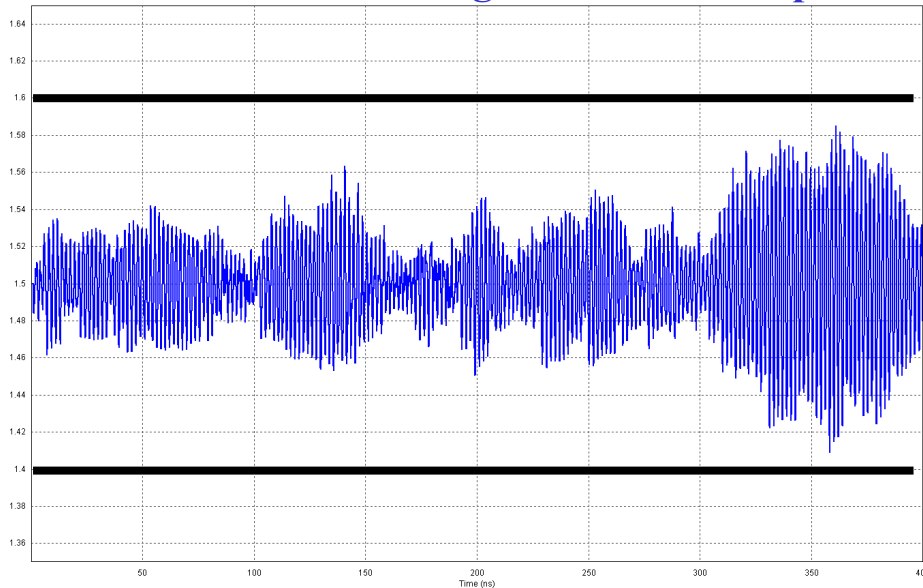- **Minimize component costs with optimized decoupling solutions**

Min value = 0.0000e+000, Max value = 2.7190e+000
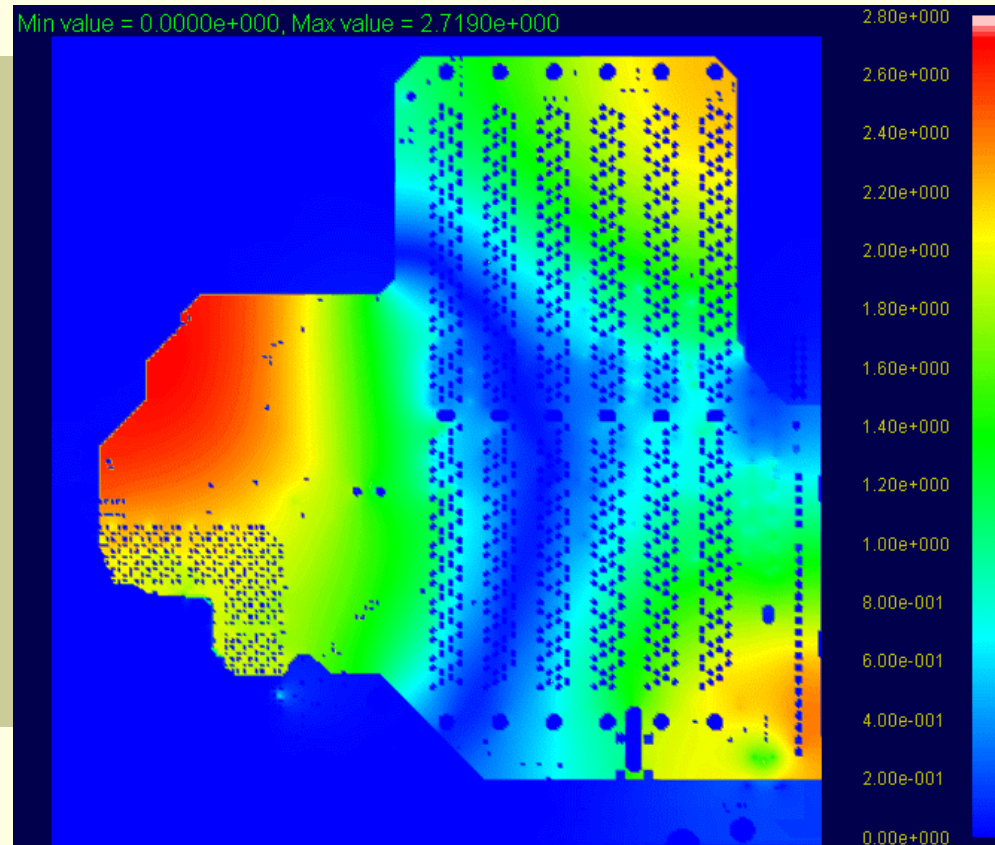
PDS Optimization – IR Drop Analysis

ASICs require a constant and stable voltage supply for proper operation

- The voltage supply is allowed to deviate by an amount specified by the vendor
- This deviation (or fluctuation) of the supply is composed of DC loss and AC noise
- The IR drop tolerance is commonly 5% (or less) of the nominal operating voltage
- If the tolerance is constant, then a reduction in DC loss yields a larger AC noise budget

Blue curve – PDS voltage with no IR drop   **Red curve – Same PDS voltage with 50mV drop**
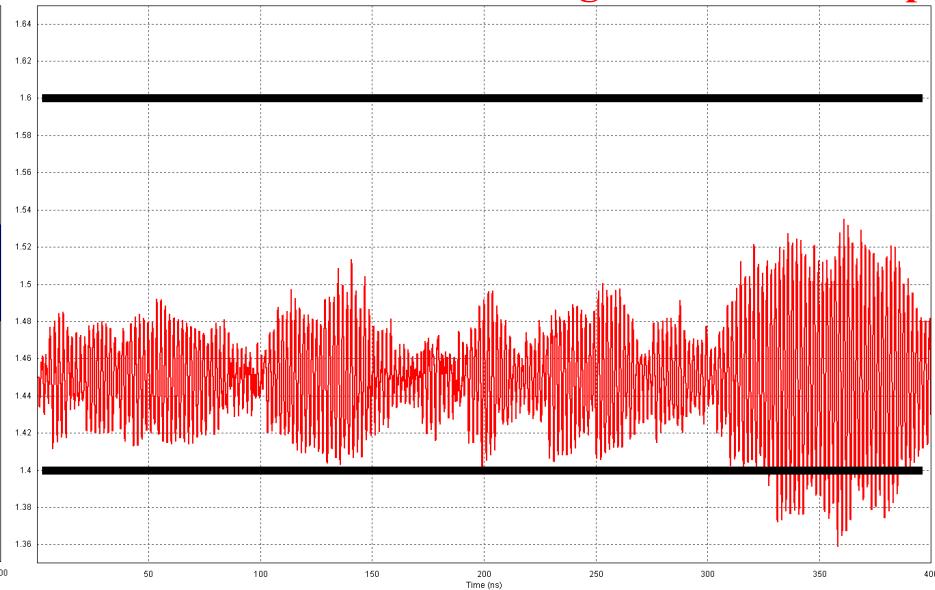
Why is DC Analysis Important?

- Numerous factors have combined to exacerbate the problem
  - Core voltage levels continue to drop: 1.2V and less are now common
  - As voltage is reduced, current requirements typically increase: IR drop = I * R
  - Less layers and higher densities have reduced the available area for power nets
  - Antipads around vias perforate the planes and can overlap – the "Swiss cheese" effect
  - Complex geometries make analysis with hand calculations difficult, if not impossible

Neck-down
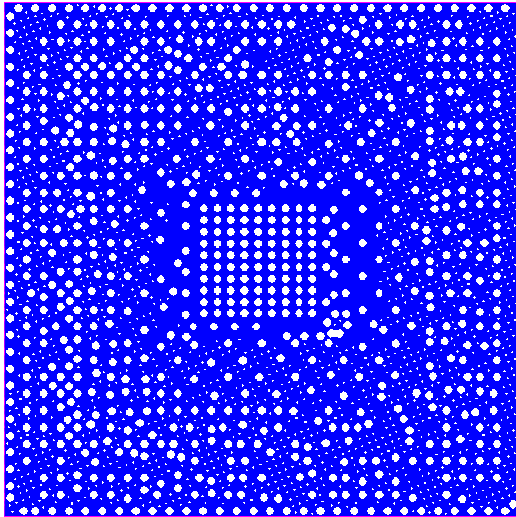
**Swiss Cheese on solid plane**

Dynamic trace routing can cut off the PDS

- IR Drop is a system level problem – analysis of the entire power distribution system (PDS) is necessary to optimize the end-to-end voltage margins for every device on the distribution

# PDS Optimization – IR Drop Analysis

Typical Objectives of DC Analysis:

- Pinpoint critical voltage distributions and IR drop issues at multiple component locations

- Optimize IR drop-sensitive Package and Board device locations

- Locate current distribution "hot spots" that may lead to current density and thermal issues

- Optimize crucial VRM (voltage regulator) sense line locations and nominal output voltage settings

- Quantify total path and loop resistances of the complex PDS

- Identify hard-to-find, high resistance areas

- Conduct conclusive IR drop analysis for the complete IC Package and Board PDS
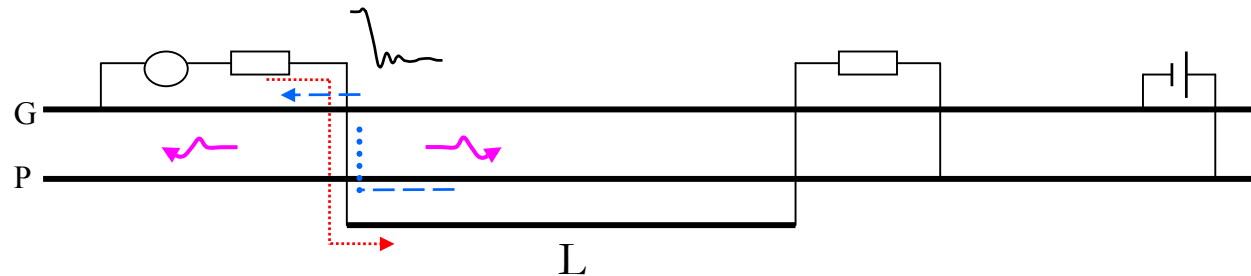

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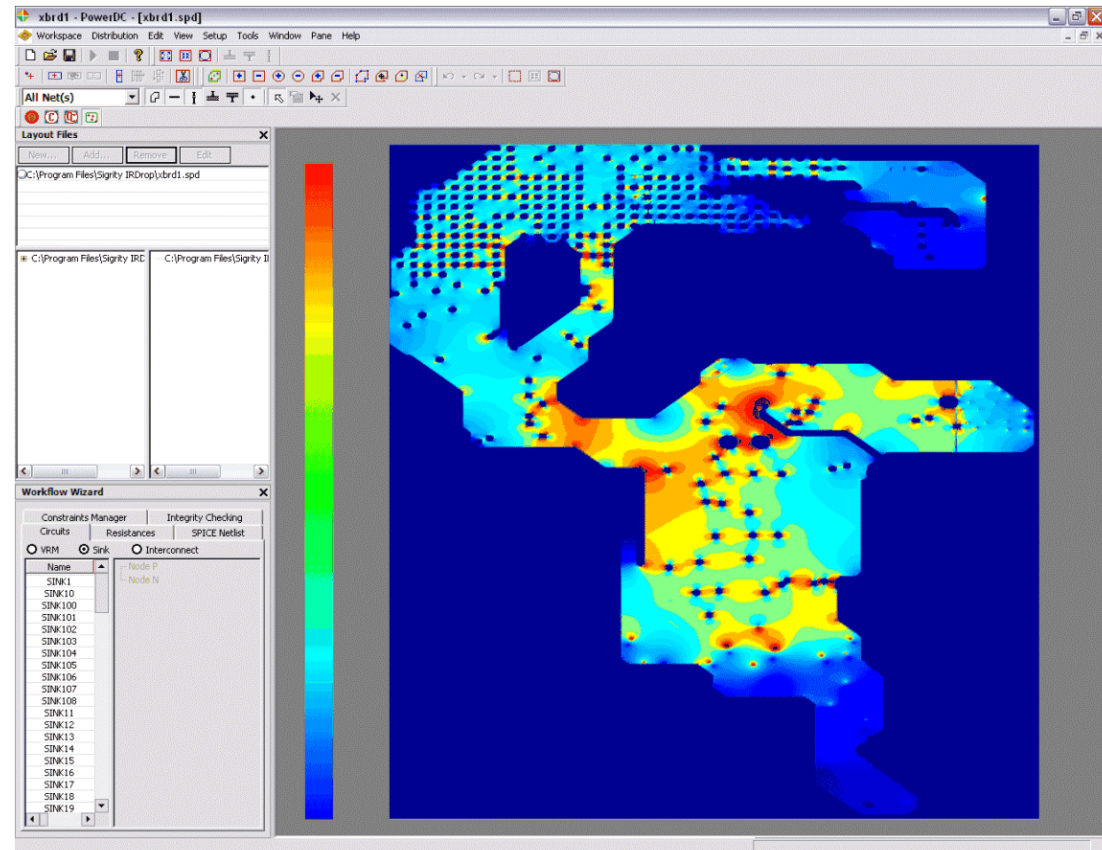
Signal Integrity Optimization – Effects of Signal Return Path Discontinuity (RPD) and SSN

One signal switching without reference plane change
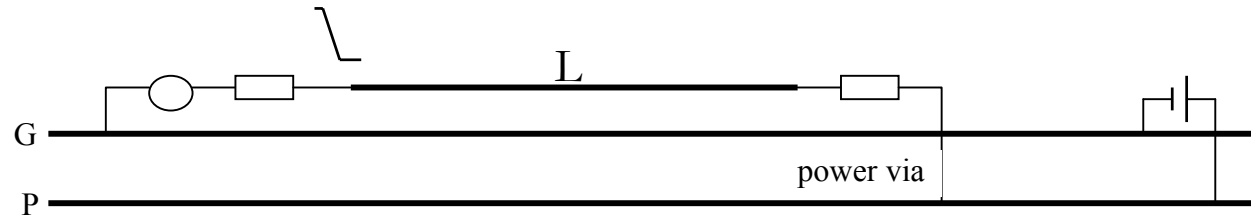
One signal switching with reference plane change,
Red:signal current   Blue:Displacement return current   Pink:power/ground voltage fluctuation due to EM waves between planes

Multiple signals switching with reference plane change,
Red: more signal currents

Pink: stronger power/ground voltage fluctuations due to EM wave between planes. More signal waveform distortion and skew.

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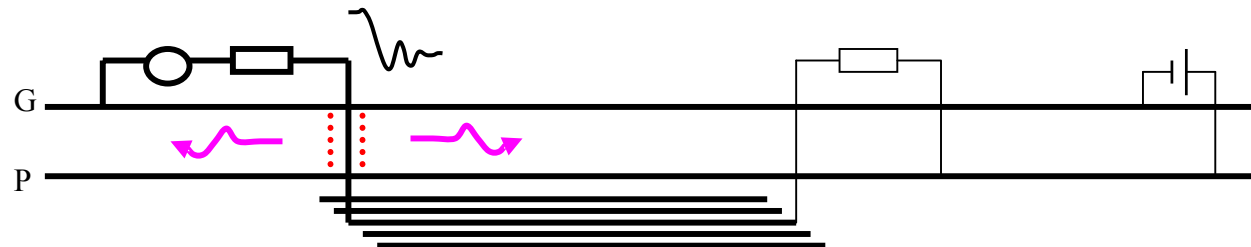
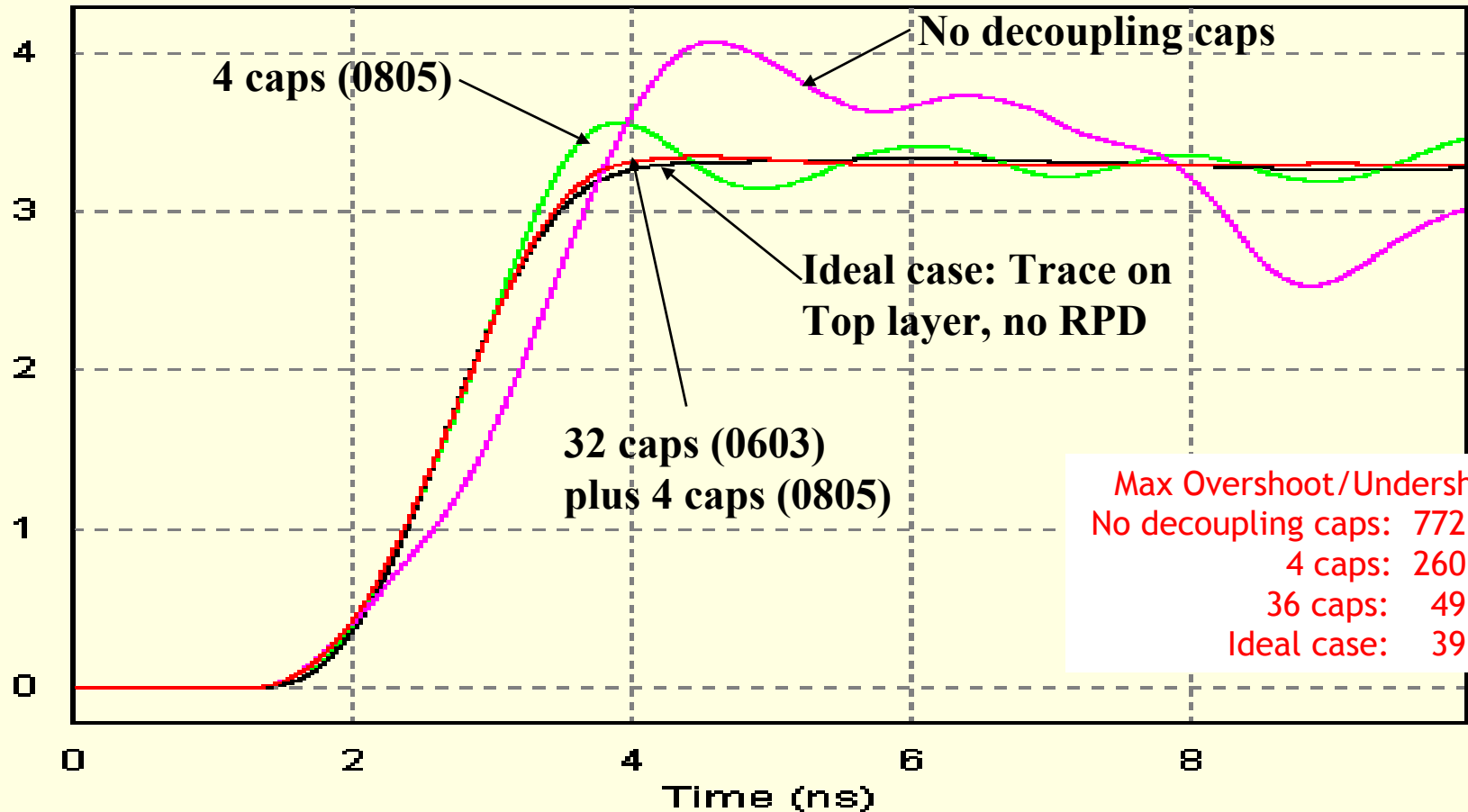# Receiver Waveforms under the Influence of Simultaneous Switching Noise (SSN)
(The number of simultaneous switched drivers was varied, no decoupling caps were used, results from *Speed2000*)
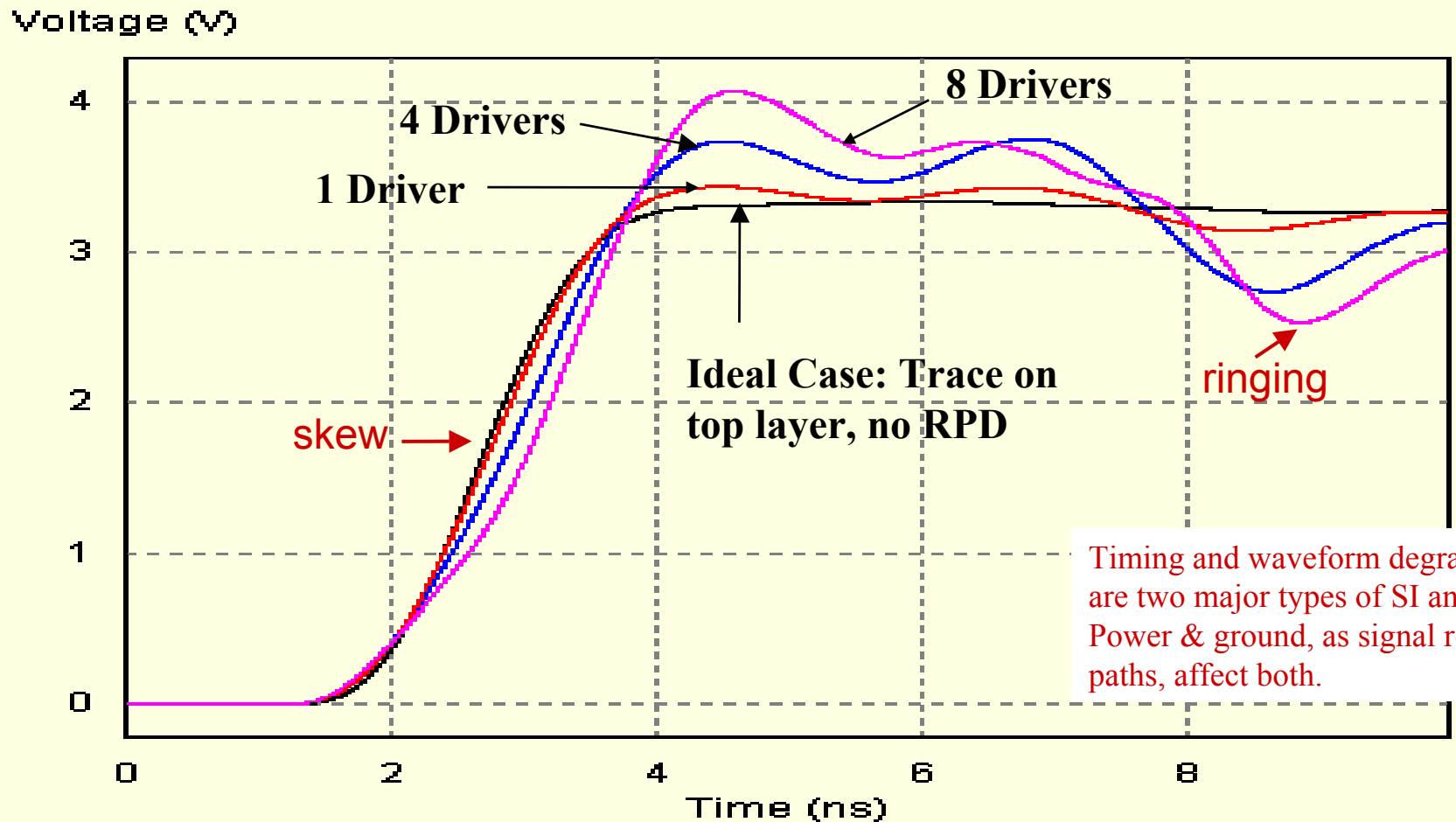
Effects of Decoupling Caps on Receiver Voltage with 8 Drivers Switching Simultaneously
(SSN reduction, results from *Speed2000*)

SIGRITY

www.sigrity.com

No decoupling caps

4 caps (0805)

Ideal case: Trace on Top layer, no RPD

32 caps (0603) plus 4 caps (0805)

Max Overshoot/Undershoot
No decoupling caps: 772 mV
4 caps: 260 mV
36 caps: 49 mV
Ideal case: 39 mV

Why use S-parameters for SSO analysis?

- Lumped RLC models are a low frequency approximation
  - A single RLC segment cannot accurately model propagation delay
  - Frequency-dependent, broadband coupling is mandatory at GHz switching frequencies
  - Power / ground impedance is highly frequency dependent – RLC cannot model this easily

- Power / ground structures affect the I/O signal's performance
  - Realistic power distribution systems (PDS) do not supply a constant, ideal voltage
  - Large, parallel busses create huge current transients (large dI/dt)
  - PDS noise degrades the signal quality of a driver's output (SSO pushout for example)
  - Resonance in the PDS significantly increases via crosstalk and impedance

- S-parameters capture the frequency dependent response and coupling of the power / ground structures and I/O signals

Broadband Package Model Extraction

34-port mixed PDS and I/O S-parameters, 100 Hz – 5 GHz
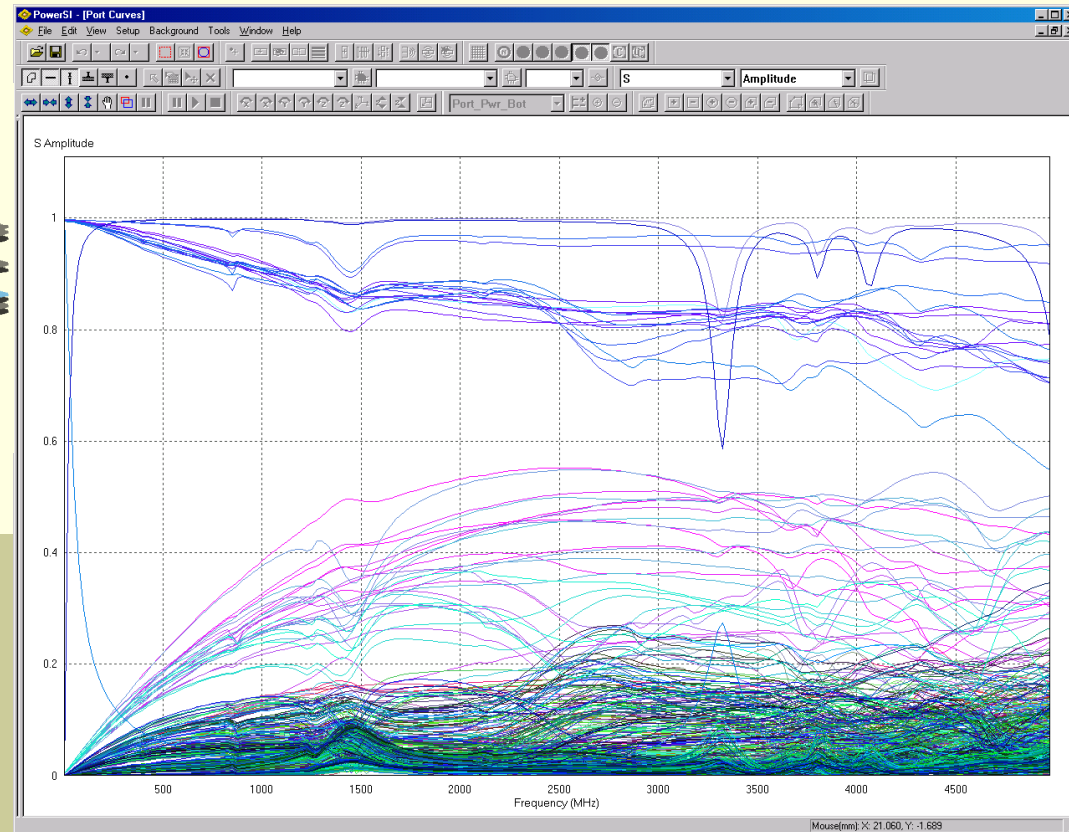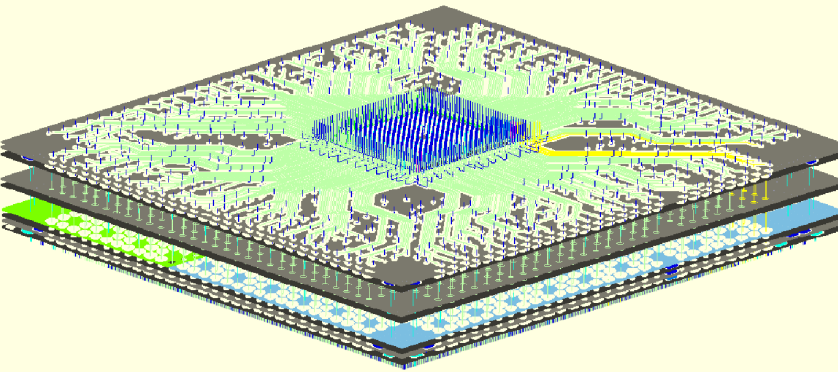
The 16 signal nets in the left corner of the package are of interest.

An equivalent circuit model is extracted for these 16 signal nets, together with the power and ground nets.

Suggestions for S-parameter Extraction

Only extract the nets of interest

- **Example: don't extract the PCI bus if you're only interested in DDR**

- **Typical extractions are 8 to 32 data nets; 64+ nets only when necessary**

- **Use current mirrors (multipliers) for large, parallel busses**
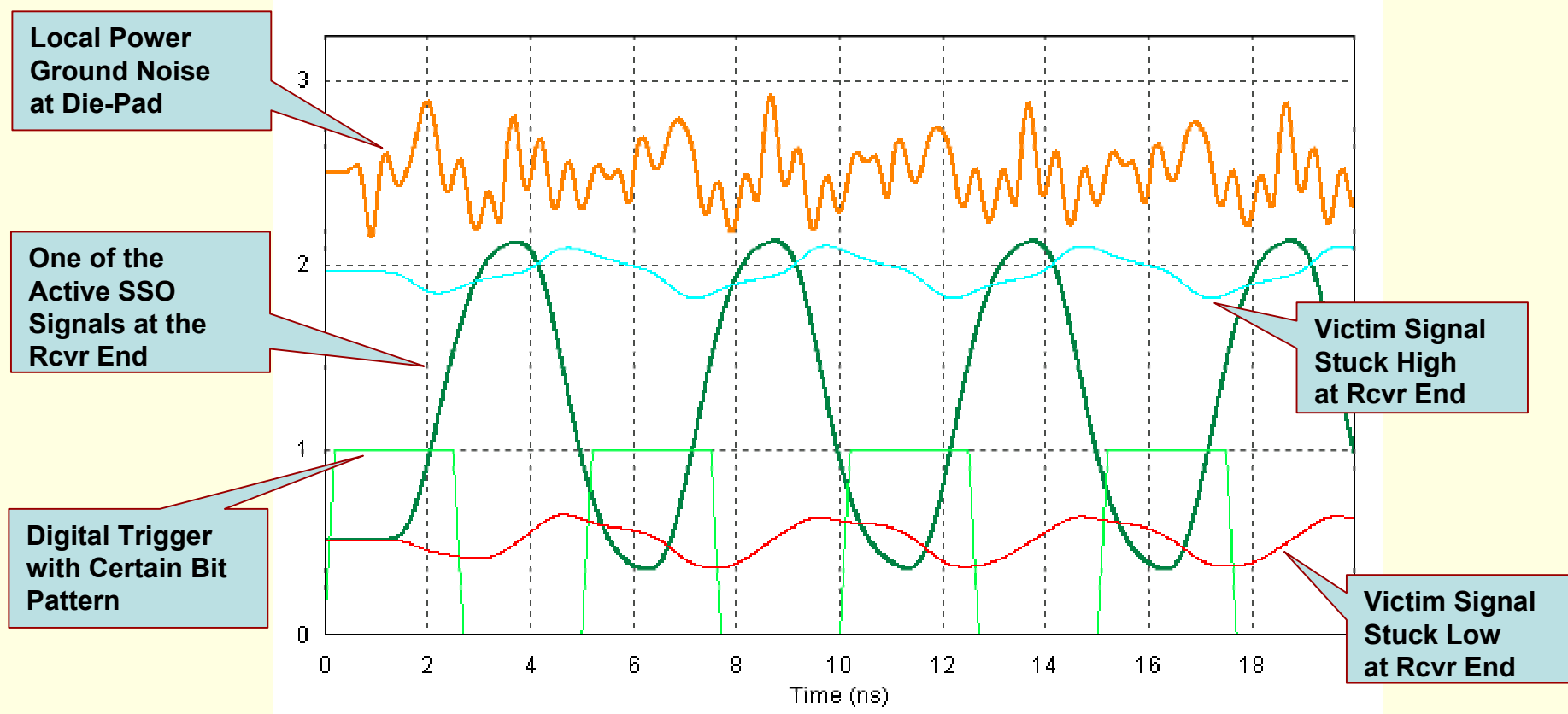
Set an appropriate frequency sweep

- **~100 Hz – 10 MHz: Log sweep with at least 5 points per decade**

- **10 MHz – 2+ GHz: Linear sweep with a 10 or 20 MHz increment**

- **The low frequency data is important!**

Typical PDN return-loss curve
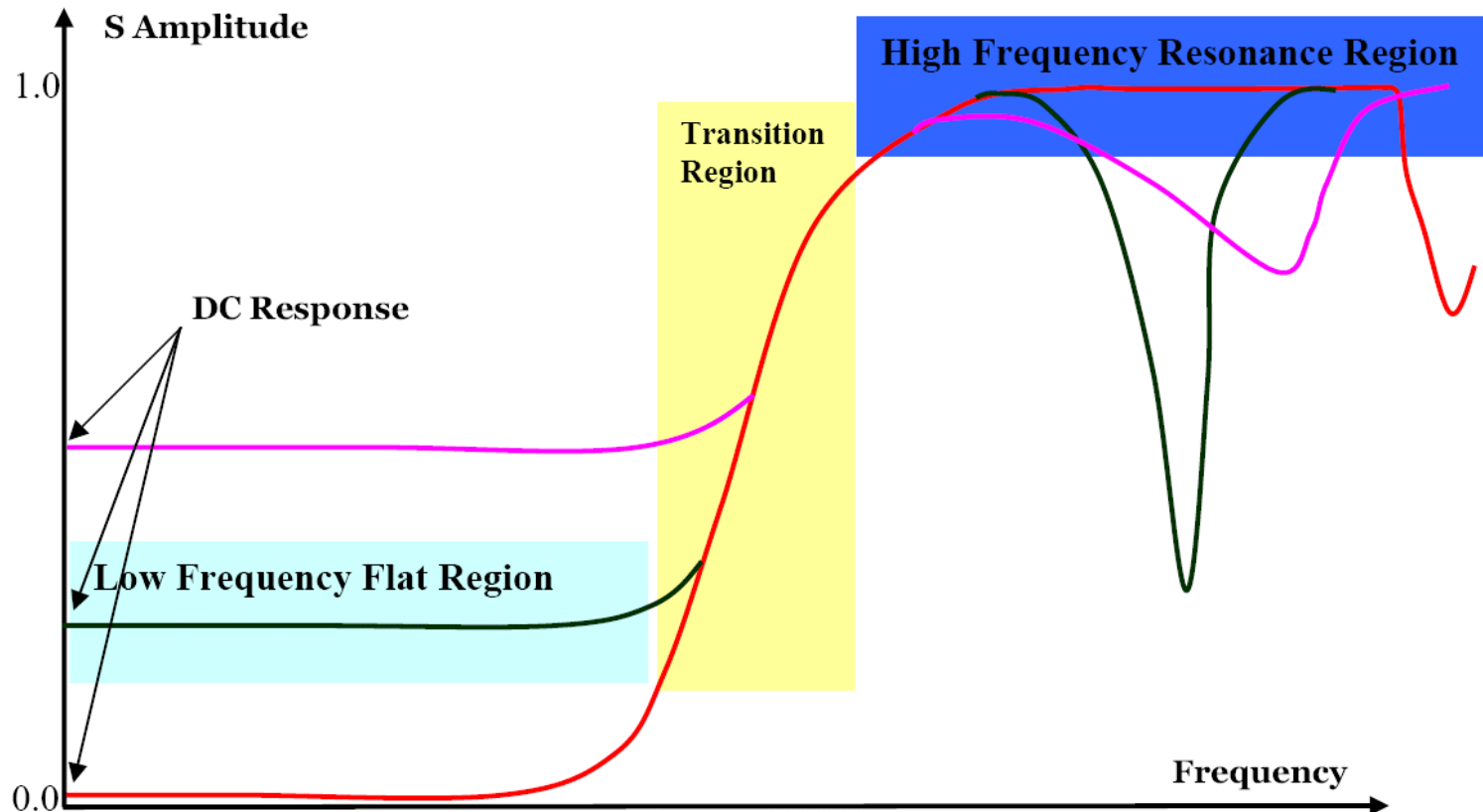
The low frequency flat region and the transition region must have a sufficient number of data points to enable the final simulator to accurately extrapolate the entire curve.

SSO Methodology – Stuck Bits

Local Power Ground Noise at Die-Pad

One of the Active SSO Signals at the Rcvr End

Victim Signal Stuck High at Rcvr End

Digital Trigger with Certain Bit Pattern

Victim Signal Stuck Low at Rcvr End

Set two of the data bits as stuck high and stuck low victims. These results can assist with a more in-depth analysis of the power and ground rail fluctuations.

SSO Methodology – PRBS
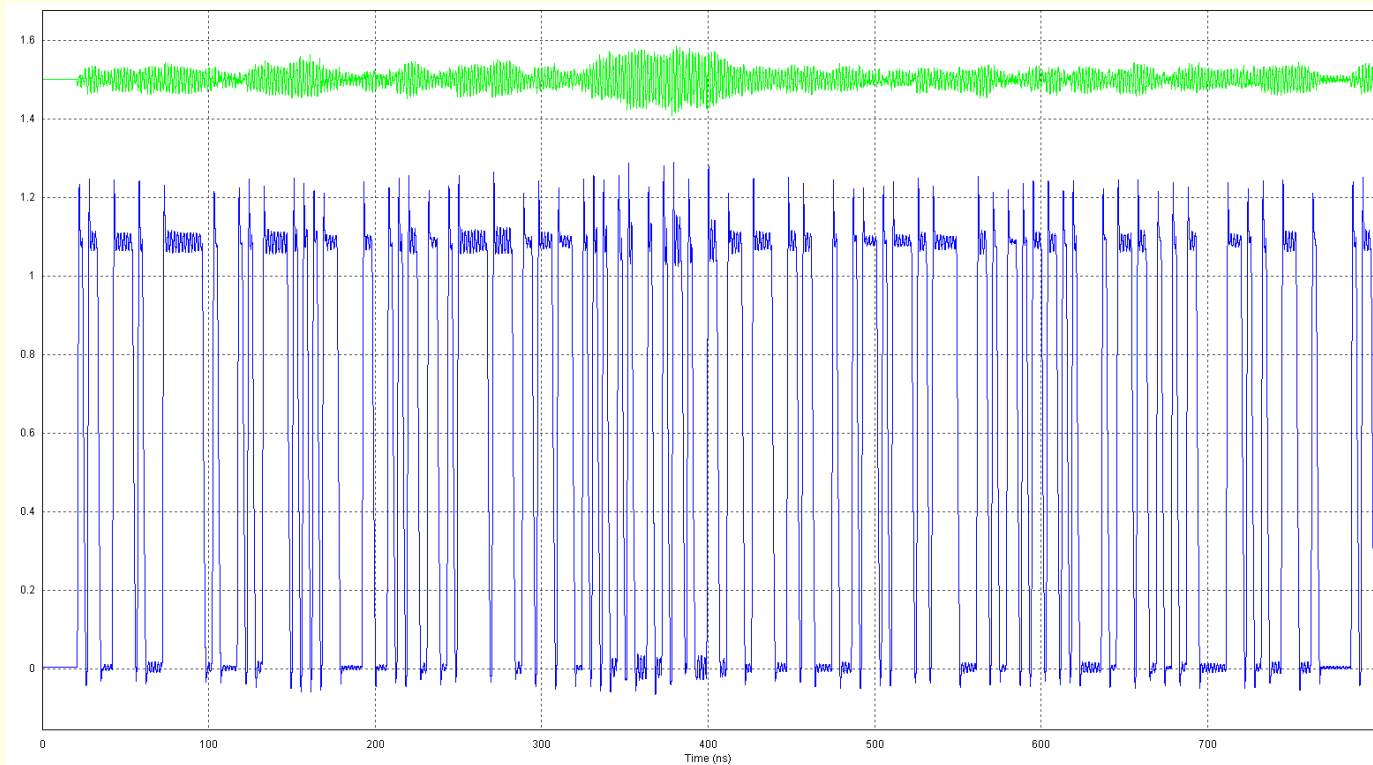
The worst case power/ground noise does not always occur with 1010… transitions. Random bit patterns will reveal the impact of PDS impedance problems that would otherwise be missed with repeating 1010... patterns.

Summary

- Optimizing the PDS impedance will reduce the supply noise, improve signal integrity, and generate less EMI

  - The PDS voltage noise has AC and DC components

  - Decoupling and IR drop analysis will maximize voltage margins of the complete system

- Capturing the interactions between the PDS and the I/Os is necessary for accurate signal integrity and SSO analysis

  - Ensure that signal return currents are accurately modeled, because unmanaged return currents can cause lots of PDS related noise phenomena

- Stuck bits and a PRBS stimulus are valuable techniques in identifying underlying problems for I/Os and the PDS

Thank You!

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