WELCOME FROM MICHAEL MIRMAK, INTEL CORPORATION

On behalf of the I/O Buffer Information Specification (IBIS) Committee, I would like to welcome you, our presenters and guests, to this first open IBIS Summit in Asia.

As you will see from the Summit discussions, behavioral modeling in general and IBIS in particular are needed more than ever in the electronics industry. Greater design complexity and demand for higher operating speeds have always presented challenges to our industries. These challenges are growing as our markets and the business and engineering resources that serve them expand to cover the entire globe. Our industries have an ever-present need for signal integrity data exchange methods that can support users with radically different design targets, procedures and tools with predictable performance. Yet, for optimum business efficiency and growth, those same methods must enable fast signal integrity analysis while maintaining information security. Fortunately, IBIS satisfies all these requirements, demonstrating throughout its 12-year history an increasing ability to support new technologies and industry needs. Through this Summit and future Summits, we hope to make the value of IBIS readily apparent.

We are very pleased that IBIS has been so enthusiastically received across Asia and are confident that IBIS Summits such as this one will continue in the years to come. We are especially grateful to our sponsors Huawei Technologies, Cadence Design Systems, Mentor Graphics Corporation, Signal Integrity Software and Sigrity, plus IBIS-supporting industry organizations such as the Japan Electronics and IT Industries Association (JEITA). Without them, this event would not have been possible.

We hope that you will find the presentations and discussions beneficial and enjoyable.

Sincerely,
Michael Mirmak
Chair, IBIS Committee

我代表 IBIS 委员会，欢迎各位演讲者和嘉宾参加在亚洲举办的第一次 IBIS 峰会。

大家将在这次峰会的讨论中看到，行为级模型越来越普遍，IBIS 模型在业界也得到更广泛的使用。高复杂度、高工作速度的设计需求给业界带来很多挑战。这些挑战从市场到业务到工程领域，覆盖了全球。业界要求信号完整性的数据交换方法可以支持用户快速地满足不同地设计目标，流程和适应不同的工具，并具有可接受的速度和精度，而且这些方法在满足快速的信号完整性分析下能保证信息安全。幸运的是，IBIS 满足了所有的需求，12 年来展示了满足新技术和业务需求的持续发展的能力。通过这次峰会和未来的峰会，我们希望能继续发扬 IBIS 的价值。

我们非常高兴地看到 IBIS 在亚洲被热情地接受，我们相信，IBIS 峰会将会继续下去。我们也特别感谢我们的赞助方：华为公司、Cadence Design Systems 公司、Mentor Graphics 公司、Signal Integrity Software 公司和 Sigrity 公司，还有支持 IBIS 的其他业界组织，比如日本 JEITA。没有他们，这次会议不可能顺利召开。

我们希望这是一个有意义的有价值的技术讨论会。

衷心的

迈克尔 莫马克
IBIS 委员会主席

WELCOME FROM JIANG, XIANGZHONG, HUAWEI TECHNOLOGIES

Dear All,

I was very excited when Mr. Bob Ross proposed that IBIS hold an IBIS meeting in China. Huawei has been designing and developing high-speed circuits for more than 8 years. This field is attracting more attention and focus in China with many talented people. Up to now, no purely neutral, technical public meeting has existed. We are now initiating the Asian IBIS Summit.

Huawei agreed to be a primary sponsor for this event in April, 2005. We also received a lot of logistical and financial support from our friends, Cadence Design Systems, Mentor Graphics, Signal Integrity Software, and Sigrity. After IBIS sent the first invitation in August, we received many registrations and paper submissions from major Chinese industries involved in high-speed design.

Here, I truly hope this IBIS Asian Summit will be successful. Welcome everyone.

Best regards,
Jiang, XiangZhong

大家好，

今年年初鲍伯若什先生给我提及希望在中国开办一届 IBIS 研讨会的时候，我非常高兴地表示赞成。高速电路设计领域在华为在中国已经开展了 8 年以上，这个领域也受到越来越多地关注，聚焦了越来越多的人才，但是始终还没有一个中立的公开的技术研讨的会议：IBIS 亚洲峰会是第一次。

自今年 4 月，华为承诺做主要赞助商以来，得到了 Cadence Design Systems 公司、Mentor Graphics 公司、Signal Integrity Software 公司和 Sigrity 公司等友商的积极相应，有力支持了会议费用和会务筹备。自今年 8 月 IBIS 发出第一封会议邀请以来，国内各主要公司的高速设计团队均积极响应，提出投稿申请。

衷心祝愿本次 IBIS 亚洲峰会成功召开。

姜向中

AGENDA AND ORDER OF THE PRESENTATIONS

(The actual agenda might be modified)

I B I S S U M M I T M E E T I N G A G E N D A

8:15 REFRESHMENTS & SIGN IN
- Vendor Tables Open

9:00 Introductions and Program Overview
- Welcome, Jiang, XiangZhong, (Huawei Technologies, China)
- Welcome to Summit, Mirmak, Michael (Intel Corporation, USA)
- Welcome Comments, Invited Chinese Leader (China)

9:30 **IBIS and Behavioral Modeling 5**
Mirmak, Michael (Intel Corporation, USA)

9:45 **Fiberhome Telecommunications Technology Experiences with IBIS Models 11**
Zheng, Qi (Fiberhome Telecommunications Technology, China)

10:15 BREAK (Refreshments)

10:30 **Three Facets of IBIS: Interface, Behavior and Measurement 17**
Dodd, Ian* and Li, Henry** (Mentor Graphics Corporation, *USA and **China)

11:00 **Simulation with IBIS in Tight Timing Budget Systems 31**
Sui, ShiJu, (ZTE Corporation, China)

9:45 **JEITA EDA - WG Activity and Study of Interconnect Model . . 45**
Watanabe, Takeshi (NEC Electronics Corporation, Japan)

12:00 FREE BUFFET LUNCH (Hosted by Sponsors)
- Vendor Tables

12:00 - 12:45 Press Conference for IBIS Officers and Sponsors

AGENDA AND ORDER OF THE PRESENTATIONS (Continued)

IBIS and Behavioral Modeling

Michael Mirmak
Intel Corporation
Chair, EIA IBIS Open Forum

IBIS Summit
Shenzhen, China
December 6, 2005

迈克尔.莫马克
英特尔公司
IBIS 委员会主席

亚洲 IBIS 技术研讨会
中国深圳
2005 年 12 月 6 日

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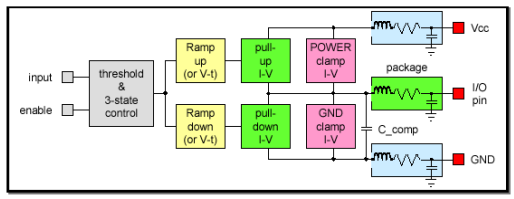
What is IBIS?

- **IBIS* (I/O Buffer Information Specification)**
  - A standard format for expressing I/O buffer electrical behavior plus component pin and package information
  - ANSI/EIA* 656-A, IEC* 62014

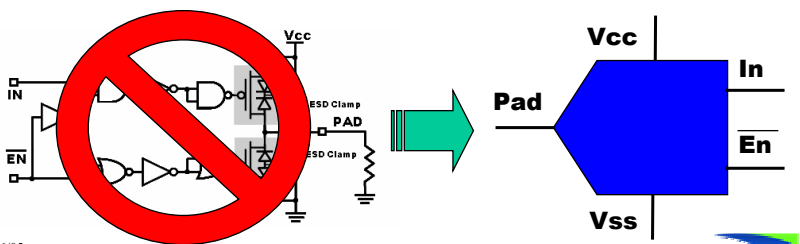
Most buffers expressed through
- Current vs. Voltage (I-V tables)
- Voltage vs. Time (V-T tables)
- Buffer capacitance (C_comp)

Components include
- Pin assignments and names
- Package information



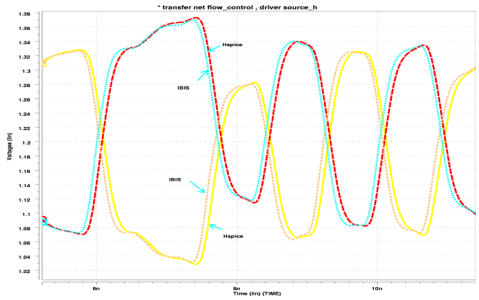
Behavioral Modeling

- **IBIS is only one type of behavioral model**
  - Others include:
    - ICM* (IBIS Interconnect Modeling Specification)
    - IMIC* (I/O Model for Integrated Circuits, JEITA* ED-5302)
    - ICEM* (Integrated Circuit Electrical Model, IEC 62014-3)
    - VHDL-AMS* (IEEE* 1076.1)
    - Verilog-AMS* (Accelera*)
- **Behavioral models replace internal design information with *observations of electrical ports or terminals***



An Example

- IBIS, as a behavioral modeling standard, offers
  - Protection of internal design information
  - Availability under multiple software tools
  - Increases in simulation speed over transistor-based models
- IBIS behavioral vs. transistor-based models
  - For a serial-differential design, IBIS can be 100 times faster!
  - Careful model creation preserves accuracy



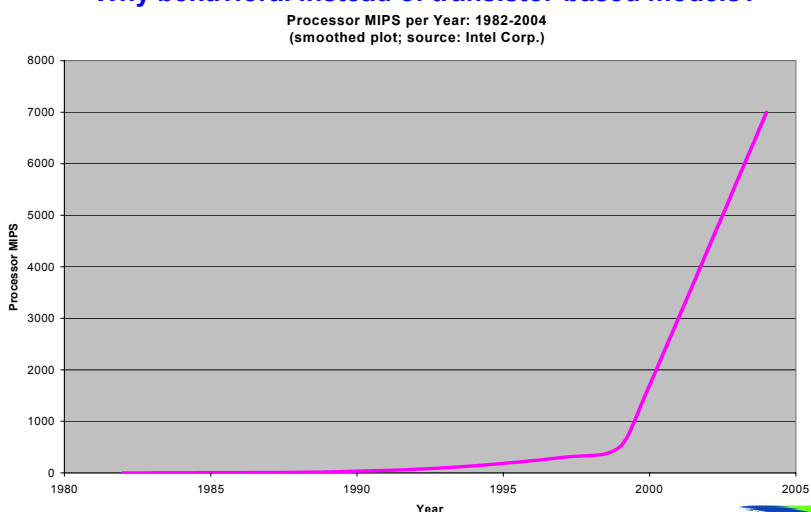
IBIS vs. SPICE*
(time-shifted to show correlation)

Image from SiSoft*:
IBIS Models at 2.5 GHz and Beyond; used with permission

Speed quotation from
Multi-Gigabit SerDes System Level Analysis...
by Huq/Dodd; used with permission

The Future of Modeling

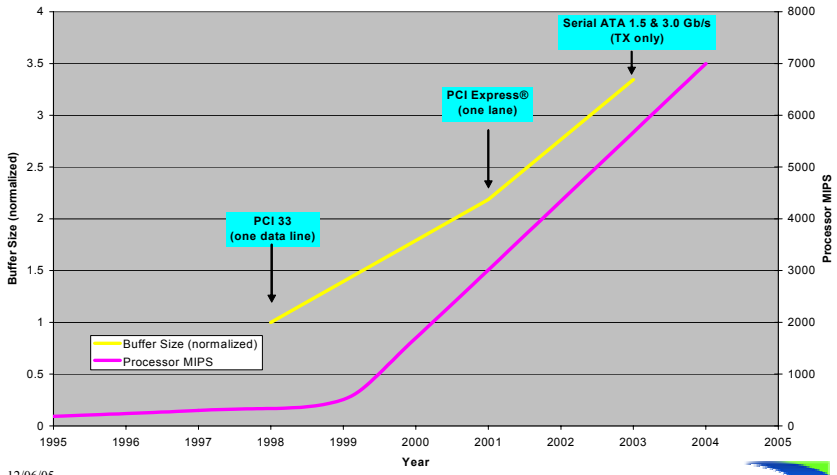
- Why behavioral instead of transistor-based models?



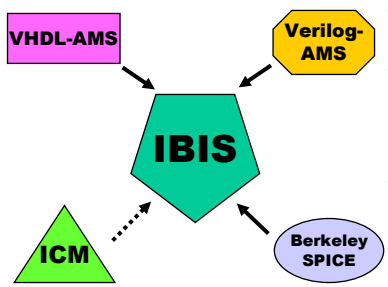
The Future of Modeling

- **Buffer complexity is keeping pace with processor power!**

I/O Buffer Size and Processor MIPS per Year: 1995-2004
(source: Intel Corp.)



Supporting Future Designs



- **Buffers becoming more complex**
  - Size is *tracking processing power*
- **New designs need more analysis**
  - Power delivery and switching noise
  - Pre-emphasis, active feedback and compensation
- **IBIS expanding to address needs**
  - New links to VHDL-AMS, Verilog-AMS, Berkeley SPICE*
  - Enable equations within IBIS
  - Links to ICM are in development

The industry needs behavioral modeling for today and tomorrow

IBIS provides a standard, unified solution for behavioral buffer modeling

You Are Invited!

- **IBIS Welcomes Worldwide Participation!**

Specifications
- **IBIS:** http://www.eda.org/ibis/ver4.1/
- **ICM:** http://www.eda.org/ibis/icm_ver1.1/

Training
- **Including IBIS history and tutorials**
- http://www.eda.org/ibis/training/

IBIS Cookbook
- **Features explained plainly**
- http://www.eda.org/ibis/cookbook/

Task Groups
- **Futures, Macromodel Library, Quality**
- **Free Model Review service!**

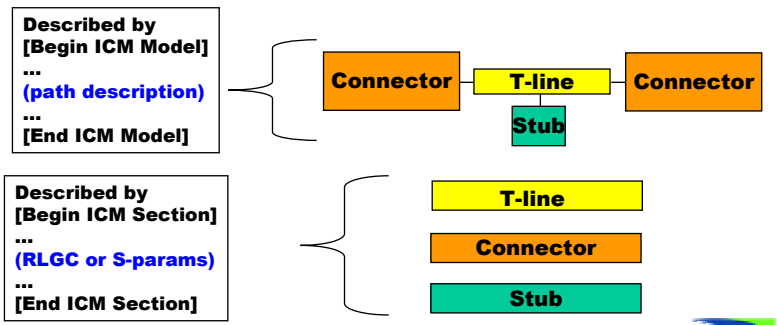
http://www.eigroup.org/ibis/
http://www.eda.org/ibis/

IBIS appreciates your input and support!

BACKUP

A Related Specification: ICM

- ICM = IBIS Interconnect Modeling Specification
  - Standard text format for interconnect modeling data
  - "Interconnect" can be connector, cable, PCB traces or even an IC package
    - *Defines structure as path between "sections"*
    - *Defines the electrical data for each section*



Fiberhome Telecommunications Technology Experiences with IBIS Models

Zheng Qi
Qzheng@fiberhome.com.cn

Overview

IBIS Models have played an important role in signal integrity analysis

- Access Buffer Characteristics
- Waveform Quality Check
- Timing Analysis

Buffer Characteristics

What Information can we get ?

- Use V-I Curves to calculate the driver output impedance
- V-t Curve provides the Buffer's transition time
- C_comp provides intuitional info of the load

Waveform Quality Check

Critical Net check

- Edge Trigged Signals
- Clocks

Check Contents

- Incident Voltage
- Edge Monotonic
- High /Low noise margin
- Source/sink currents

Timing Analysis

Flight Time Calculating

- Flight Time provides more reasonable descriptions than T.L Propagation Delay in Timing Budgets calculation
- T.L Delay ,loads and topology effects are taken into consideration

Mostly used model parameters

- IBIS 1.0 V-I Curves
- IBIS 1.0 C_comp
- IBIS 2.1 rise/fall waveforms
- IBIS 2.1 Pin mapping

- IBIS 3.2 seldom
- IBIS 4.0 seldom

Model check

Typical Problems

- Non-monotonic data in PU/PD table
- DC point does not match I-V load line
- V-t tables End slope not flat
- …

Always tools will filter these points,but good Understanding of these warning is necessary

Successful stories

- Multi-Drop bus Analysis

  When debugging we found data was improperly strobed .Post analysis shows there is non-Monotonic Clock Edge. Using high bandwidth probe check again and got it

- Timing Analysis

  Strong Driver results in Hold time conflict

Occurs at “Low Speed” situation

Behind these stories

IBIS models provides some clues in Waveform Quality check. But

- How Simulator processes the model is a black box
- Simulated result sometimes are tools relevant

Behind these stories

Timing Analysis

- Different Driver strength results in great different Delay
- Under low speed situation Timing analysis was proven and the IBIS model works well
- IBIS model can't describe the internal delay of the buffer . when doing timing analysis we always puzzle about the "Zero" reference point . especially when timing budgets is tight
- Closing the Timing loop requires Core-to-core timing

Problems

- High Speed Serial Interconnect have widely used . But effective analysis was lagged
- Find Bugs of Serial Interconnect is more difficult than old designs . Maybe it is an impossible task

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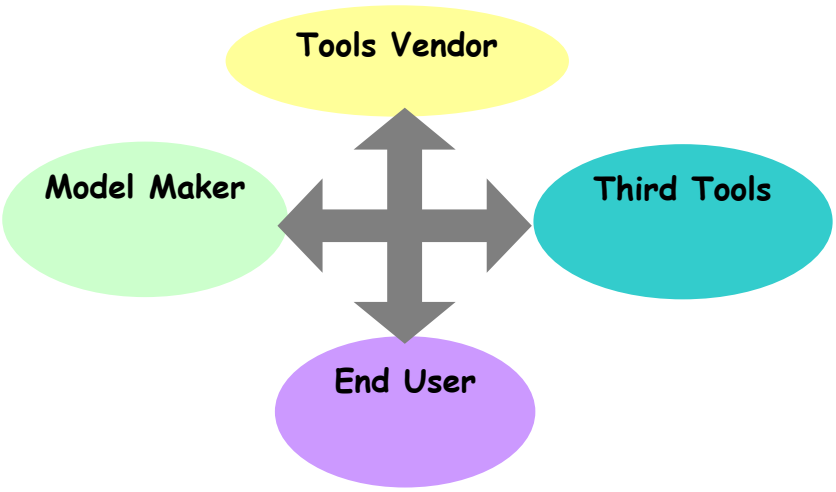
We are expecting



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Three Facets of IBIS: Interface, Behavior and Measurement

December 2005

Ian C Dodd
Architect, High Speed Tools
SDD Division
Henry Li
Technical Marketing Engineer
Mentor Graphics (Shanghai)
Electronic Technology Co Ltd

Mentor Graphics®

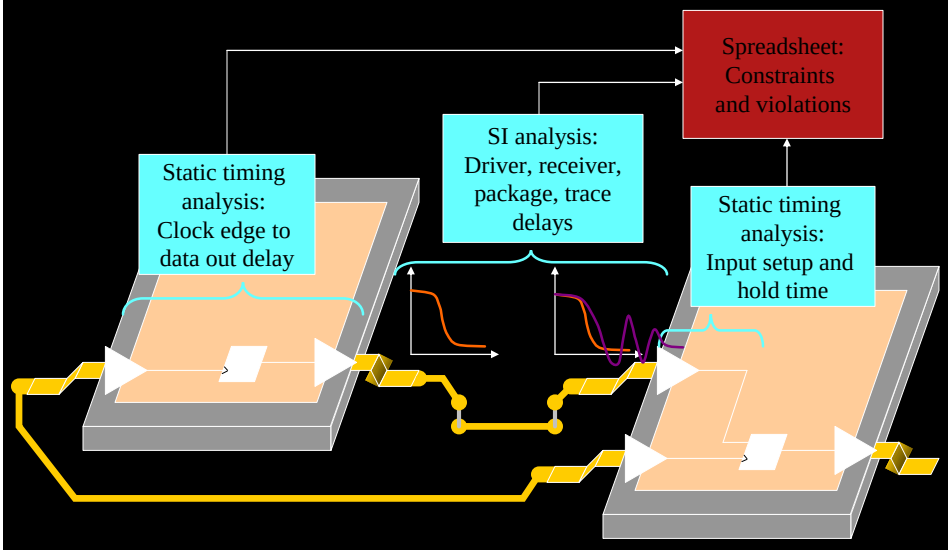
What are the Objectives of the SI Engineer?

- Maximize performance
  - Highest possible clock speed
- Ensure reliable operation
  - Meet timing constraints
  - Keep overshoot below levels that will cause device malfunction or destruction.
  - Maintain adequate switching margins
- Minimize per unit costs
  - Minimize the number of components (including terminators)
  - Use lowest cost PCB materials

How can these objectives be met?

- By investing in accurate timing and SI analysis so that safety margins can be controlled
  - Accurate static or dynamic timing models for the internal paths of active devices
  - Accurate SI models for drivers, loads and passive devices
  - Accurate models for the interconnect including the associated dielectrics
  - Using fully automated analysis tools so all vulnerable nets can be analyzed

Basic timing analysis



Part One:
Summary of IBIS to version 3.2

Highlights of IBIS 3.2 Behavior

- IBIS 3.2 assumes fixed topologies for drivers, inputs and terminators
- Support process range: Typ, Min & Max
- Drivers and Inputs
  - Two steady state Current versus Voltage (IV) tables representing power and/or ground clamps.
  - Capacitance
- Drivers
  - Nominal edge rates
  - Two additional steady state Current versus Voltage (IV) tables representing pull-up and pull-down transistors.
  - Optional Dynamic Voltage versus Time (VT) tables
    - Load conditions must be specified for each table

Highlights of IBIS 3.2 Behavior (continued)

- Series and Parallel Terminators
  - Resistance, Capacitance and Inductance
- Package Description
  - Assumes each external pin connects to one internal (die) pin
  - Default Package
    - Assumes no coupling: simple resistance, capacitance and inductance
  - Package Model
    - Allows multiple sections, each with coupled or uncoupled: resistance, capacitance and inductance

IBIS 3.2 Interconnect

- Provides mapping of the pins on a physical part to the models providing electrical behavior.
- Allows EDA tools to automatically build complete simulation models for nets on your PCB
  - Less error prone than creating simulation netlists manually
  - Allows for simulation coverage of the majority of nets on your PCB.

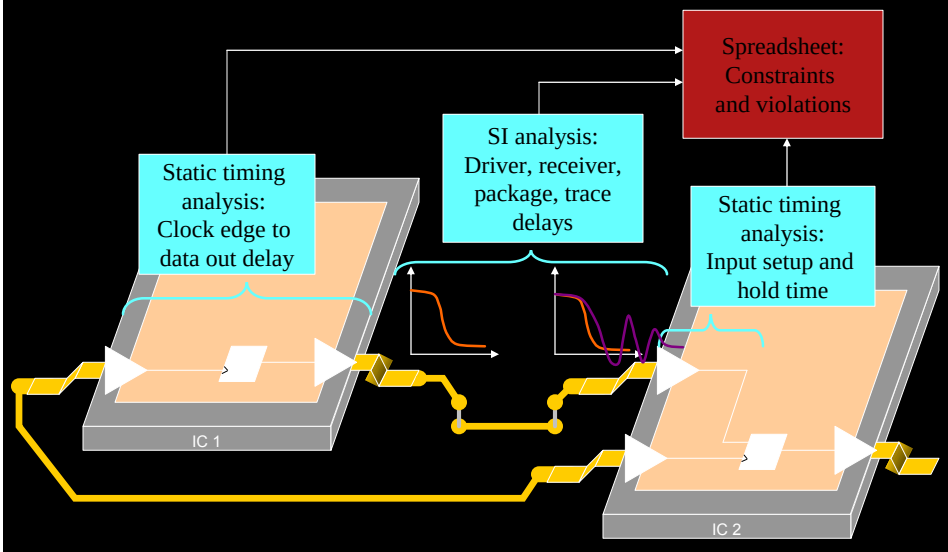
Highlights of IBIS 3.2 Interconnect

- IBIS Pin Section
  - Assigns driver, load and parallel terminator models to pins
- Series Pin Mapping Section
  - Assigns series terminators (and switches) to pins
- Diff Pin Section
  - Identifies differential pin pairs & adds differential delay info
- Electrical Board Description (EBD)
  - Limited description of a PCB containing IBIS components
  - Does not support modeling of trace to trace coupling.

Highlights of IBIS 3.2 Measurement

- Overshoot limits
  - If exceeded device may malfunction or be destroyed
  - Static and dynamic
- Input switching thresholds
  - Logic low
    - Vinl (or with hysteresis Vinl+ and Vinl-)
  - Logic high
    - Vinh (or with hysteresis Vinl+ and Vinl-)
- Timing Reference Voltage (Vmeas)
  - Transition voltage on driver pin used when measuring static timing delays e.g. “clock edge to data out”
  - Associated with a reference load
    - Vref, Rref and Cref

Basic timing analysis



Putting it all together with IBIS 3.2

- Simple synchronous example
  - First consider the data path
- Simulate the data path for the rising and the falling edges
  - Find the time at which the input pin on U2 leaves the initial logic state (raw minimum delay)
  - Find the time at which the input pin on U2 becomes stable at the final logic state (raw maximum delay)
- Simulate the driver connected to the timing reference load
  - Find the time to Vmeas
- Normalize the raw delays by subtracting the time to Vmeas
  - Removes any initial delay in VT table and partial edge time already included in the “clock edge to data out” delay.

Including Clock Skew

- Determine Clock Period
  - T_{clock}
- Simulate Data Path
  - Find Normalized Data Path Delays
    - TD_{data_min}, TD_{data_max} for rising and falling edges
- Simulate Clock Paths
  - Clock Driver to Clock Input on IC1
    - TD_{clock1_min}, TD_{clock1_max} for active edge
  - Clock Driver to Clock Input on IC2
    - TD_{clock2_min}, TD_{clock2_max} for active edge
- Get Internal Path Delay and Minimum Setup and Hold constraints from Databook
  - TD_{path}, T_{setup_min}, T_{hold_min}

Including Clock Skew (continued)

Worst Case Analysis

Calculate the actual setup and hold times for the rising edge

Compare the results to the timing constraints from the databook

Repeat for the falling edge

$$T_{setup} = T_{clock} - TD_{data\_max} + TD_{clock2\_min} - TD_{clock2\_max}$$

$$T_{hold} = T_{clock} - TD_{data\_min} + TD_{clock2\_max} - TD_{clock2\_min}$$

EDA tools that have integration between timing and SI analysis commonly have spreadsheets that automate these calculations and highlight timing violations

Part Two:
Beyond IBIS Version 3.2

Technology Changes

- Data rates on PCB have dramatically increased.
- PCB trace lengths have not shrunk in proportion
  - clock periods are often shorter than the interconnect delay
  - Source synchronous design must be used either with a separate clock signal or with an embedded clock
- Power budgets have decreased
  - Signaling voltages have been accordingly decreased
- PCB materials have not dramatically improved
  - Dielectric losses become the predominant circuit effect
  - Differential signaling is required to overcome attenuation
  - Pre-compensation or equalization is becoming common to compensate for wavefront distortion

Highlights of Post IBIS 3.2 Behavior

- ICM provides multi-stage coupled lossy transmission line or S-parameter modeling for connectors
  - Presently considering allowing ICM package descriptions so we can have consistent S-parameter support
- Multi-lingual extensions support behavior modeled in SPICE, VHDL-AMS and Verilog-AMS.
  - Almost no limit to the complexity of behavior that can be modeled
  - Depending on the simulator, model types can be mixed across the PCB and even on individual nets
- Power Integrity extensions

Highlights of Post IBIS 3.2 Interconnect

- Multi-lingual extensions provide flexible connectivity between SPICE, VHDL-AMS or Verilog-AMS models and the external component pins
  - Allows EDA tools to automatically build complete simulation models for nets on your PCB including the multi-lingual models

Existing Post IBIS 3.2 Measurement

- No enhancements to IBIS built in measurements since version 3.2
- Multi-lingual input models can determine when a transition has occurred
  - External models and circuits for inputs have a standard terminal which can be monitored by EDA tools
- Multi-lingual models can do extensive analysis and use (external circuit) terminals to present the results of analysis
  - No conventions as to how an EDA tool should interpret signals on these terminals
  - Cannot presently be used for automated analysis or to populate constraint spreadsheets

Recommendation for New IBIS Measurements

- We want to validate a high percentage of nets on PCBs
  - Requires automated measurement and constraint validation
  - IBIS is needed to provide the interface and measurement functions even when SPICE or AMS descriptions are used for behavior
- Measurement enhancements
  - Support measurements specified for any IBIS external pin or internal terminal
  - Provide voltage or current thresholds
  - Provide logic and equations that the EDA tool should use to determine values to be reported
  - Provide limits for reported values

Part Three:
IBIS 4.1 Multilingual Example

Typical IBIS 4.1Model

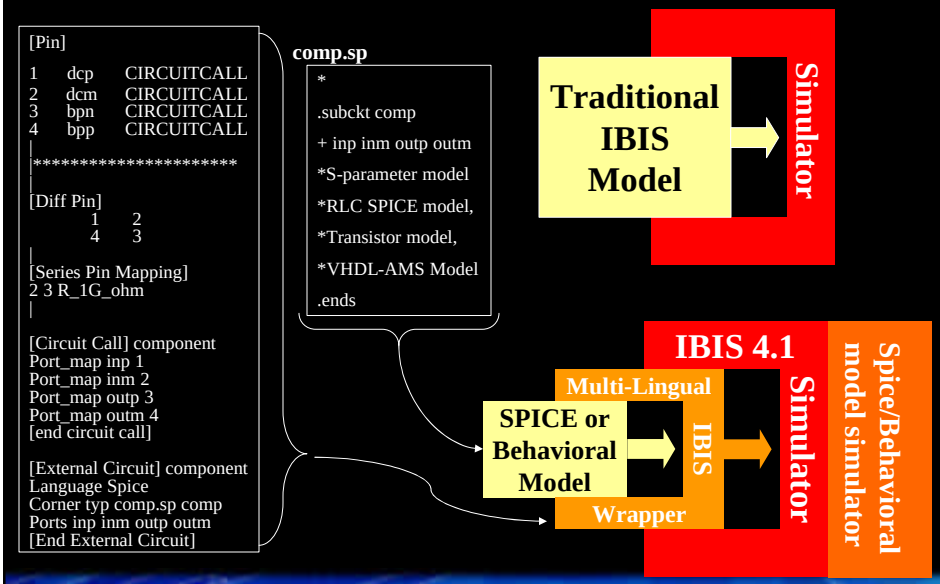
- **IBIS 4.1 adds four new keywords**
  - **[External Model] (new part of [Model])**
  - **[External Circuit]**
  - **[Circuit Call], [Node Declarations]**
- **Spice/Behavioral model is in external file**

Traditional IBIS

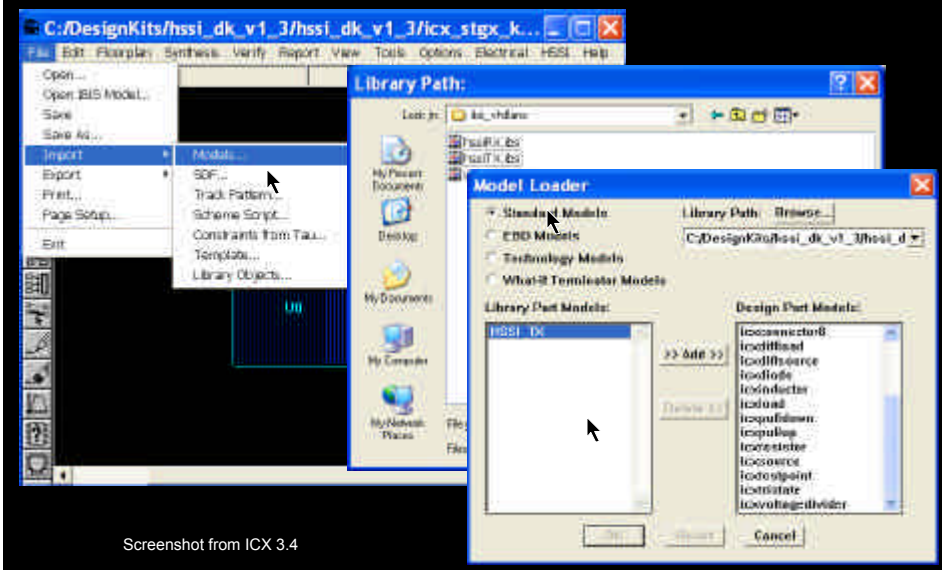
IBIS 4.1 Syntax

```
[Model] ExBufferVHDL
Model_type       Output_diff
Polarity         Non-Inverting
Vmeas = 0.75V
Rref  = 1Mohms
Vref  = 0V
|
[Voltage Range]   3.3     3.0     3.6
|
[External Model]
Language VHDL-AMS
|
| Corner corner_name file_name       circuit_name entity(architecture)
Corner    Typ          buffer_typ.vhd  buffer(buffer_io_typ)
Corner    Min          buffer_min.vhd  buffer(buffer_io_min)
Corner    Max          buffer_max.vhd  buffer(buffer_io_max)
|
| Parameters List of parameters
Parameters delay rate
Parameters preemphasis
|
| Ports List of port names (in same order as in VHDL-AMS)
Ports  D_control A_signal_neg A_signal_pos
|
[End External Model]
```

IBIS 4.1 Traditional and Multi-Lingual

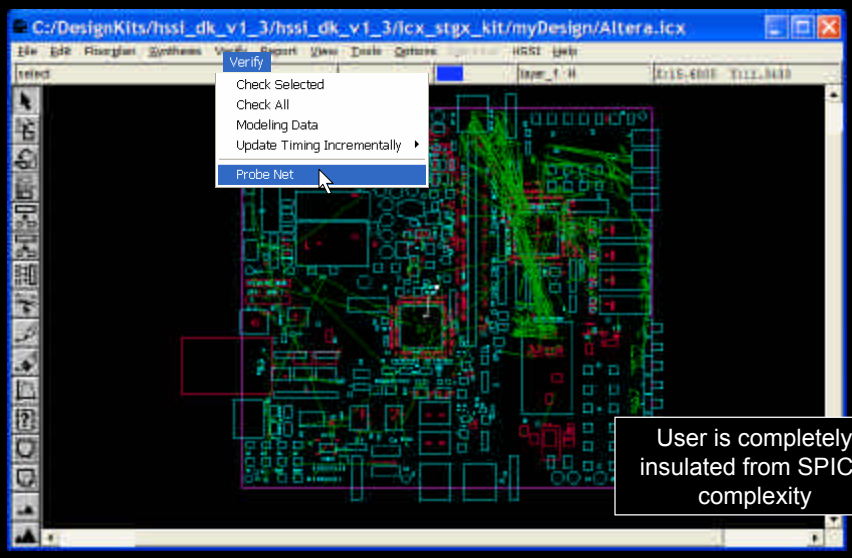


Import like any other IBIS model



Screenshot from ICX 3.4

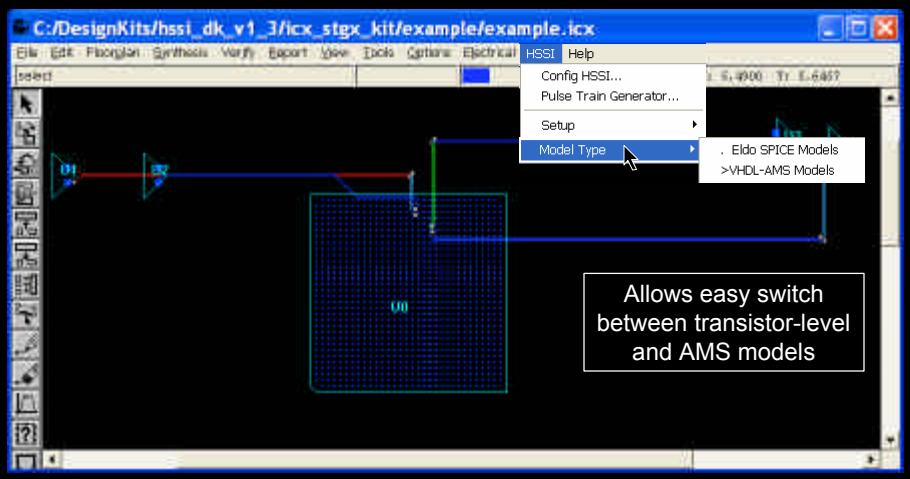
And PROBE, just like any IBIS model



User is completely insulated from SPICE complexity

Screenshot from ICX 3.4

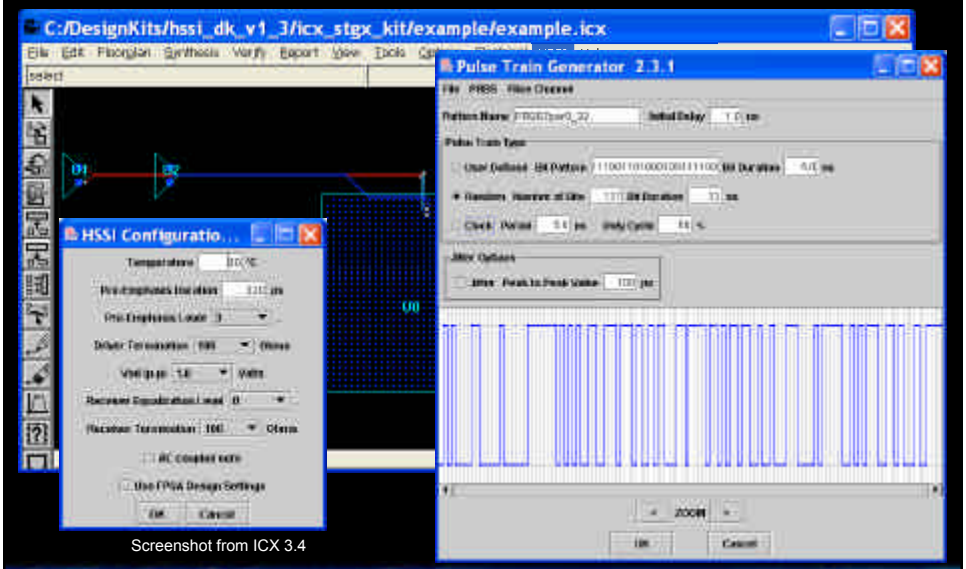
IBIS 4.1 Supports BOTH Transistor-level and AMS Models



Allows easy switch between transistor-level and AMS models

Screenshot from ICX 3.4

IBIS 4.1 “Parameters” Provide for Automation



Screenshot from ICX 3.4

Asian IBIS Summit 2005

Simulation with IBIS in Tight Timing Budget Systems

睦诗菊
SUI,SHIJU
sui.shiju@zte.com.cn
中兴通讯
ZTE CORPORATION

Agenda

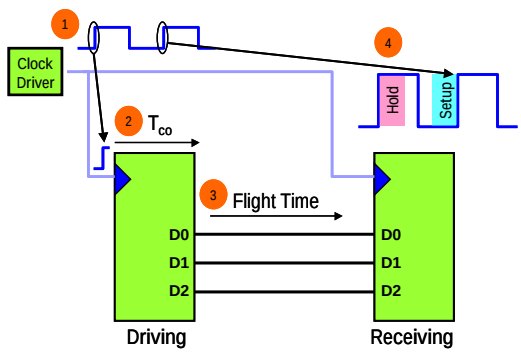
- Basis of system timing analysis
- Simulation with IBIS in tight timing budget systems
- Analysis methods

Timing Analysis Basis

- **Systematic timing analysis identifies**
  - Timing topology
  - Setup and hold time margins
  - The risk of timing violations

Common-Clock Synchronous System

- **Timing topology**



Timing Margins of CCS System

Setup_margin=Clock Period-Driver(Tcomax)-Tflightmax-Skew-Jitter-Tguard-Receiver(setup)

Hold_margin=Driver(Tcomin)+Tflightmin-Skew-Tguard-Receiver(hold)

Loose Timing Budget System Analysis

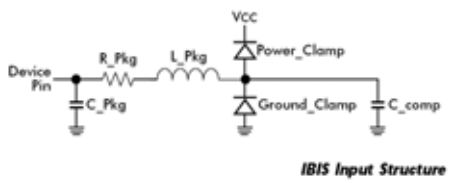
- **Definition**
- **Required inputs**
  - Timing topology
  - Component-level timing data
  - Operating clock frequency
  - Approximated flight time and guard band

Tight Timing Budget System Analysis

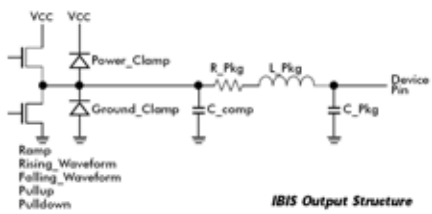
- **Definition**
- **Required inputs**
  - Timing topology
  - Component-level timing data
  - Operating clock frequency
  - *Simulation with component models is mandatory*
  - *More sophisticated numerical processing needed*

IBIS Models Do Good Job in Simulation

- **Available**
- **Effective**



IBIS Input Structure

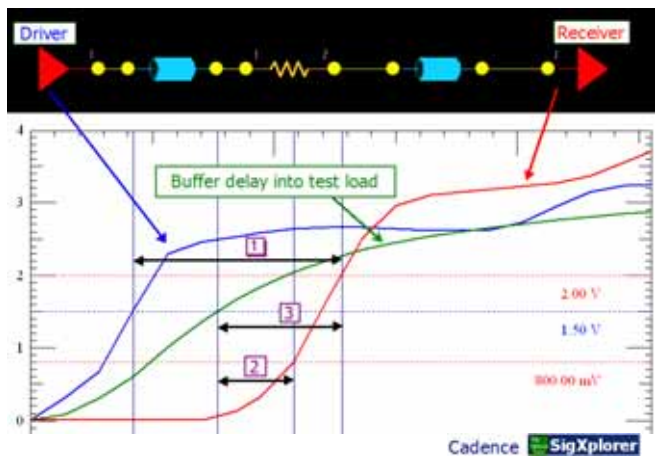


IBIS Output Structure

Flight Time

- **Flight time vs. propagation delay**
  - Propagation delay
    - The sum of T-line delays in the path
  - Flight time
    - The time it takes the data out from the driver to settle at the receiver's input
  - For tight budget designs the flight time should be simulated with cautions

Flight Time Simulation



- **Questions**
  - **Is delay1 flight time?**
  - **What are delay2 and delay3 ?**

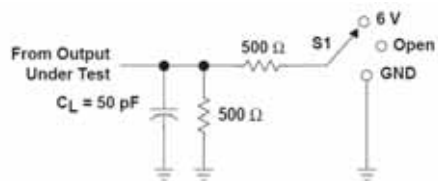
Flight Time Simulation with IBIS

- **Cautions**
  - Check component datasheet and IBIS model
  - Avoid double counting C_comp and load
  - Receiver thresholds

IBIS vs. Datasheet Consistency

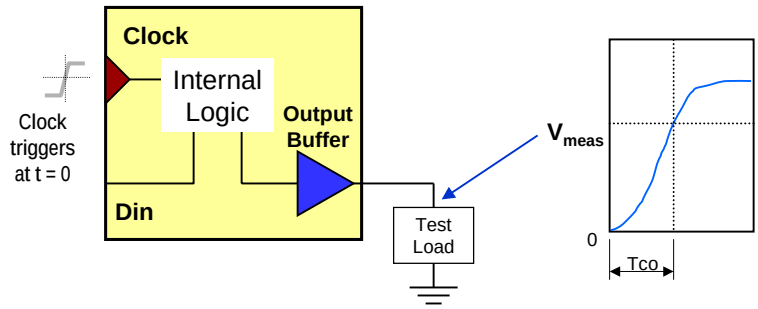
- **Test loads should match**

[Model] output
Model_type 3-state
Polarity Inverting
Enable Active-Low
Vmeas =1.5v
Cref =50pf
Rref = 500
Vref = 0.000



LOAD CIRCUIT In datasheet

Tco Measurement



Avoid Double Counting

- **Avoid double counting output C_comp**
- **Avoid counting both test load and load**
- **Method 1**
  - Compensate from simulated flight time
- **Method 2**
  - Subtract their effect from Tco

Negative Flight Time

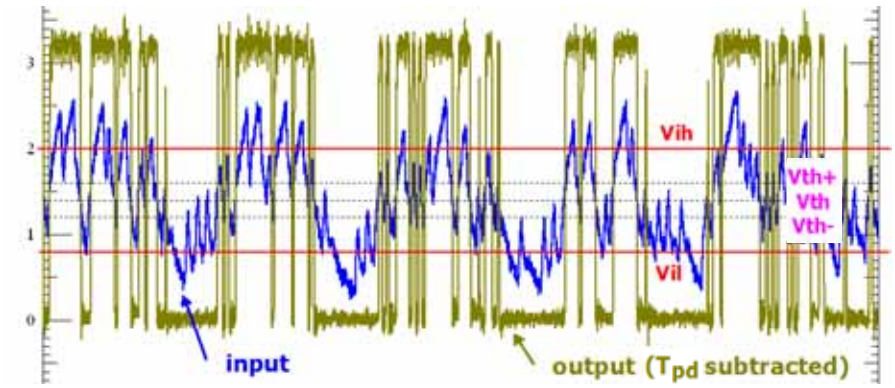
- **Negative flight time happens when**
  - Test load for Tco measurement is heavier than actual load
  - The interconnect is short

Include Corners in Simulation

- **Parts behave diversely**
- **Simulate including strong and weak buffers**

Receiver Thresholds

- **Test example**



Receiver Thresholds

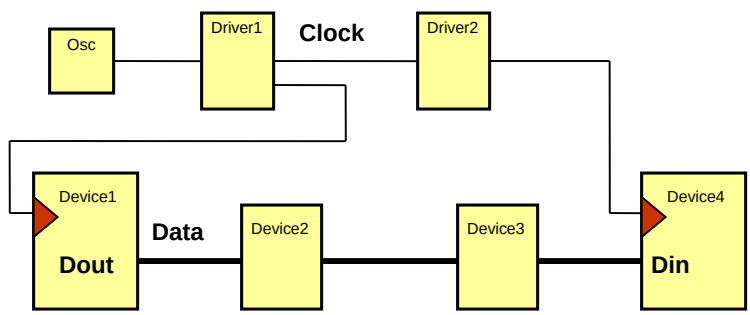
- **Use Vih and Vil as initial choice**
- **Use Vth when available**
- **IBIS Ver 4.0**
  - [Receiver Thresholds] sub-parameters
    - Vth,Vth_min,Vth_max
    - Vinh_ac,Vinl_ac, Vinh_dc,Vinl_dc
    - Tslew _ac

Guard Band Time

- **Effects likely not included in your simulation**
  - Simultaneous switching output
    - Ver4.0 and earlier models do not include SSO in data tables
  - Crosstalk
  - Inter-symbol interference
  - Power supply noise
- **Guard band time ensures margins existence**
- **Obtained from simulation or measurements**

Deal with Complex Topology

- **Example**



Deal with Complex Topology

- **Adding components in path**
  - Path delay deviations increase
  - Timing margins decrease
  - Alternative analysis methods are needed to put the simulated interconnection delays together

Timing Analysis Methods

- **Worst case timing analysis**
- **Statistical timing analysis**
  - Root Sum Square timing analysis
  - Monte Carlo timing analysis

Worst Case Timing

- **Path delay**
  - Maximum worst-case path delay

$$t_{path}\max\ \text{worst - case delay} = t_p\max(\text{device 1}) + t_p\max(\text{device 2}) + t_p\max(\text{device 3}) + \cdots + t_p\max(\text{device N}) + t_p\max(\text{interconnect1}) + t_p\max(\text{interconnect2}) + t_p\max(\text{interconnect3}) + \cdots + t_p\max(\text{interconnectN})$$

  - Minimum worst-case path delay

$$t_{path}\min\ \text{worst - case delay} = t_p\min(\text{device 1}) + t_p\min(\text{device 2}) + t_p\min(\text{device 3}) + \cdots + t_p\min(\text{device N}) + t_p\min(\text{interconnect1}) + t_p\min(\text{interconnect2}) + t_p\min(\text{interconnect3}) + \cdots + t_p\min(\text{interconnectN})$$

Statistical Timing Analysis(1)

- **Root sum square timing analysis**
  - Maximum RSS path delay

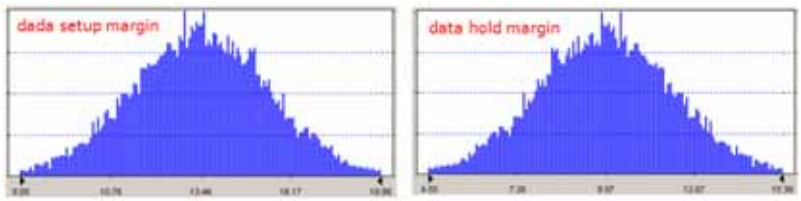
$$t_{path}\max \text{RSS delay} = t_{path}\text{typ} + \sqrt{(t_p\max 1 - t_p\text{typ}1)^2 + \cdots + (t_p\max N - t_p\text{typ}N)^2}$$

  - Minimum RSS path delay

$$t_{path}\min \text{RSS delay} = t_{path}\text{typ} - \sqrt{(t_p\text{typ}1 - t_p\min 1)^2 + \cdots + (t_p\text{typ}N - t_p\min N)^2}$$

Statistical Timing Analysis(2)

- **Monte Carlo timing analysis**
  - By random sampling delay values determines the timing attribute probability distribution



Conclusion

- **Cautions with simulation in tight timing budget system**
  - Check component test load
  - Avoid double counting
  - Receiver thresholds
- **Simulated results analysis methods**
  - Worst case
  - RSS
  - Monte Carlo

References:

James E. Buchanan ,"***Signal and Power Integrity in Digital Systems (TTL, CMOS, & BiCMOS)***", McGraw-Hill Inc., ISBN 0-07-008734-2

Stephen H. Hall, "***High speed Digital Systems Design***", McGraw-Hill Inc., ISBN: 0-471-36090-2

Todd Westerhoff ,"***Closing the loop between timing analysis and signal integrity***" Cadence Design System

JEITA EDA -WG Activity and Study of Interconnect Model

Dec 6, 2005
Asian IBIS SUMMIT in Shenzhen, China

JEITA EDA-WG
Takeshi Watanabe (NEC Electronics)

JEITA ; Japan Electronics and Information Technology Industries Association

Outlines

1. JEITA EDA-WG Activities
2. Short Term Direction of JEITA EDA WG
3. Study of Interconnect Model
4. JEITA IBIS Model Portal site

1. JEITA EDA-WG Activities

Objectives of JEITA EDA

EDA Model for

Digital Consumer Electronics

Cellular Phone, LCD /PDP TV,
Digital Camera/Video, DVD Recorder

(Digital , RF, and Analog circuits)

Auto Mobile Electronics ?

(Motor Drive, EMC)

< Applicability of IBIS V4.1 >

3

EMI, SI and PI for Digital Consumer Electronics

<Background>

EMI **High-speed Clock Frequency**

SI **DDR, PCI, PCI-Express**

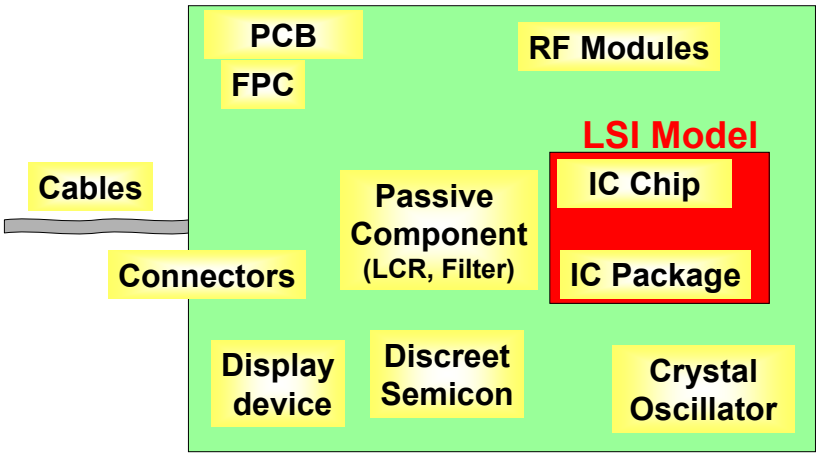
PI **High density and Large scale IC**

SiP and Module, PCB level

EMI, SI and PI Simulation Technology

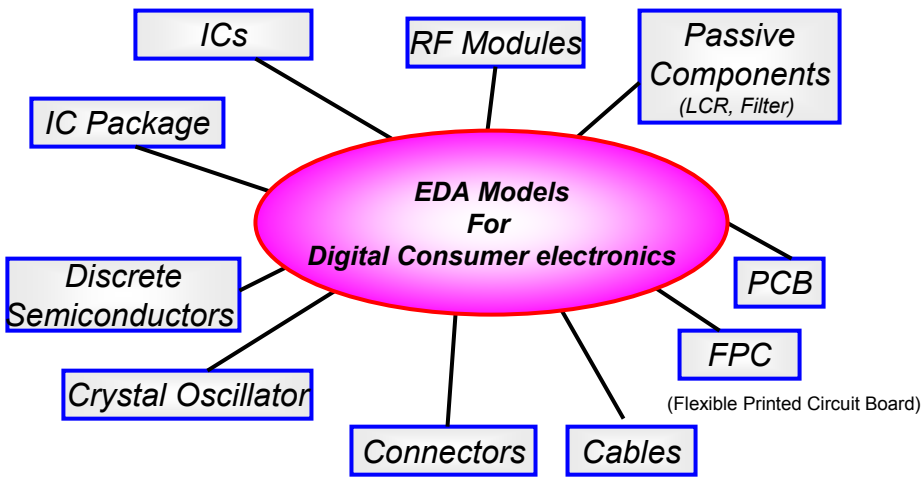
4

EDA Model for EMI, SI and PI Simulation



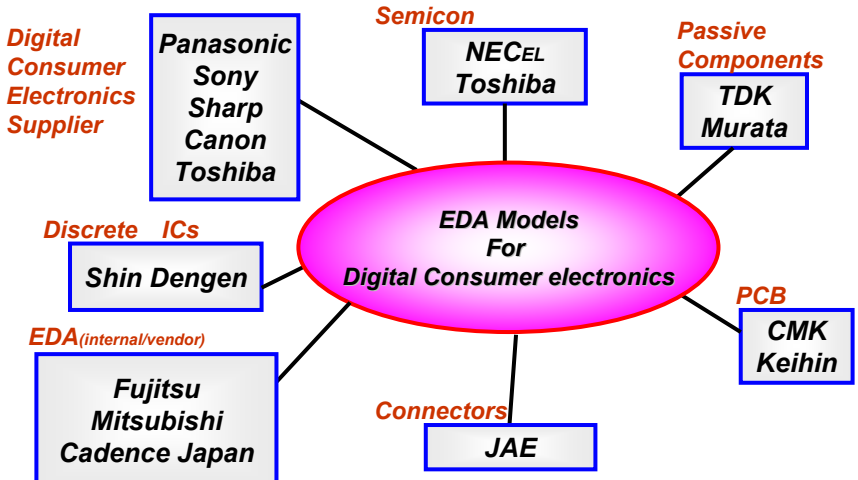
Focus of EDA Model for Simulation

10 components



JEITA EDA-WG Member

16 Major Companies

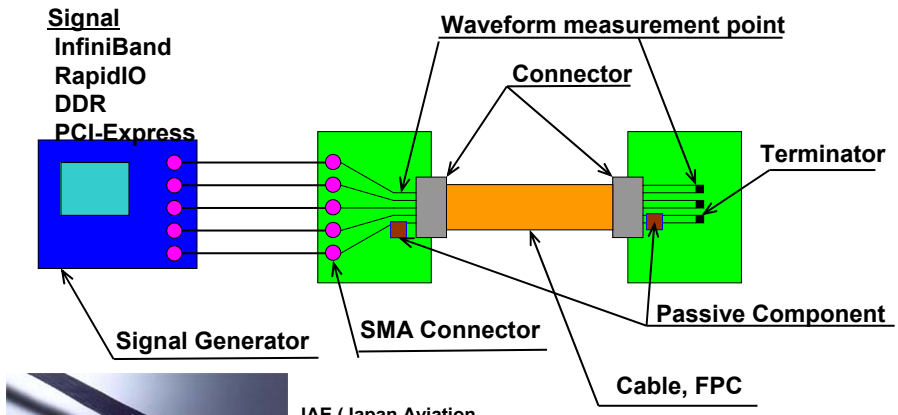


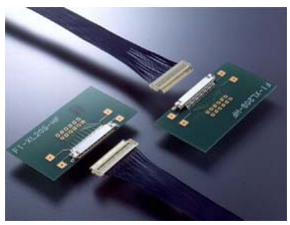
2. Short Term Direction of JEITA EDA WG

- Study of Interconnect Model
- IBIS Models of Passive Components and Connector and other Components
- JEITA IBIS Model HP
- Discussion about Case study of Simulation for Digital Consumer Electronics and JEITA-IBIS Joint meeting periodically

3. Study of Interconnect Model

SI Model （Connector, PCB, Cable）





JAE (Japan Aviation Electronics Industry)
FI-X Series

Study of Interconnect Model for Signal Integrity

◆Target Application; DDR, PCI-Express etc.

◆EDA Model; Connectors,

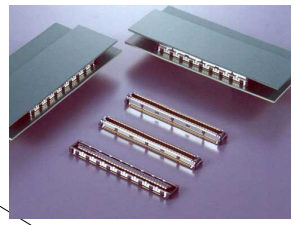
Passive Components,

PCB (Via, Pattern),

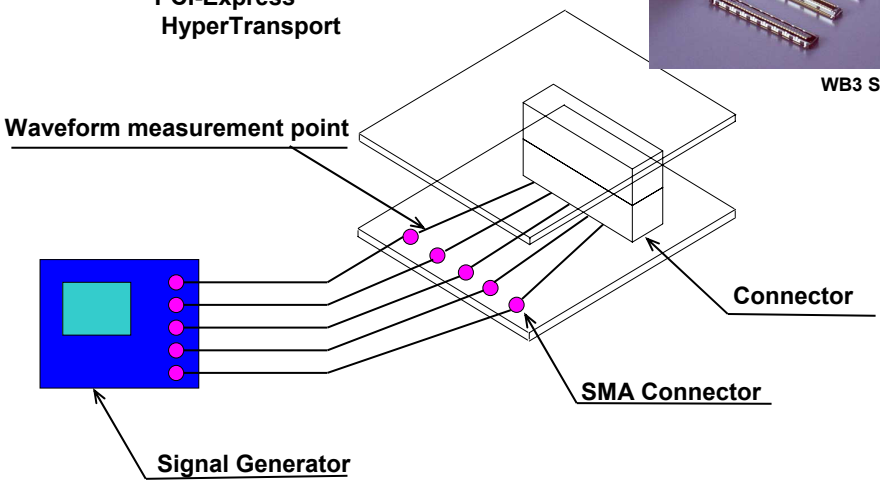
(LSI)

◆Simulation Tool; Cadence etc.

SI Model （Connector- Type B; stacked module, PCB, Cable）

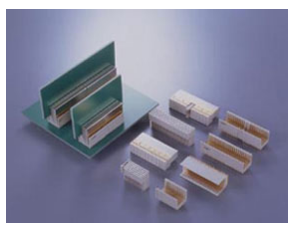


WB3 Series



11

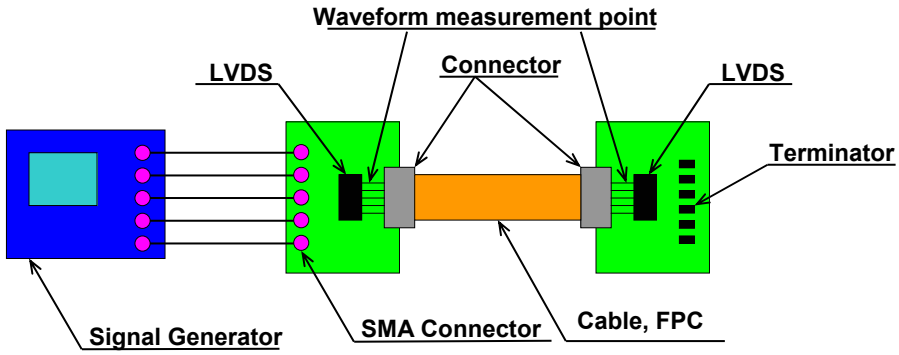
SI Model （Connector- Type C, PCB, Cable）



MJ04 Series

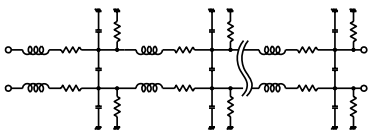
12

SI Model （Connector, PCB, Cable, LVDS）

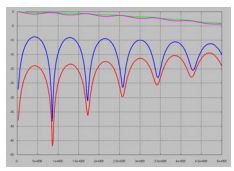


Simulation Model

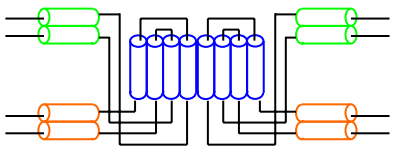
Equivalent circuit



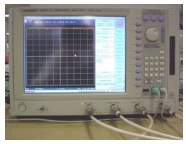
Simulation



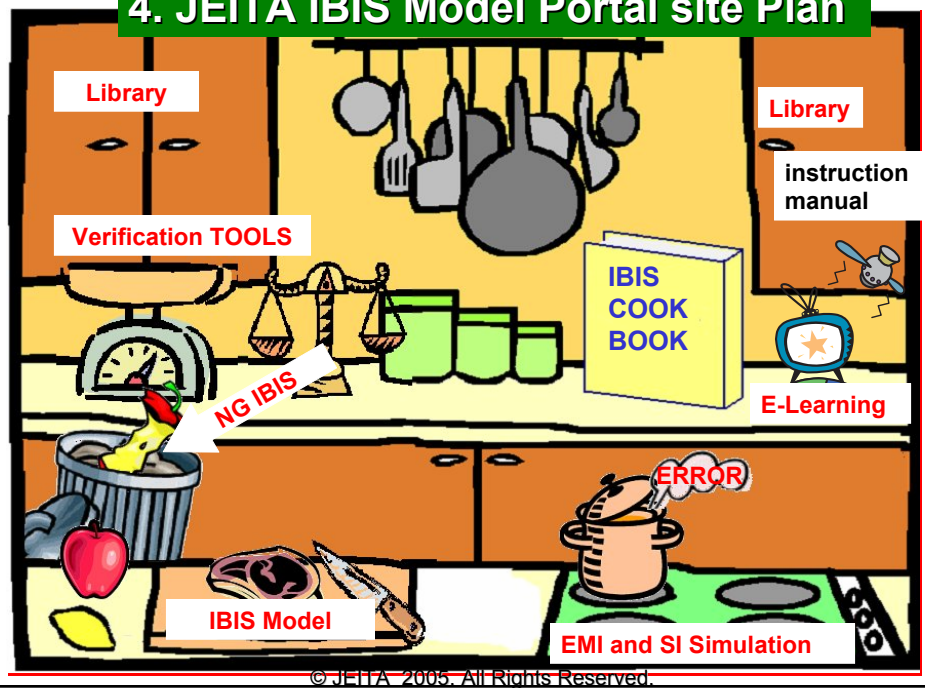
TML



Measurement



4. JEITA IBIS Model Portal site Plan

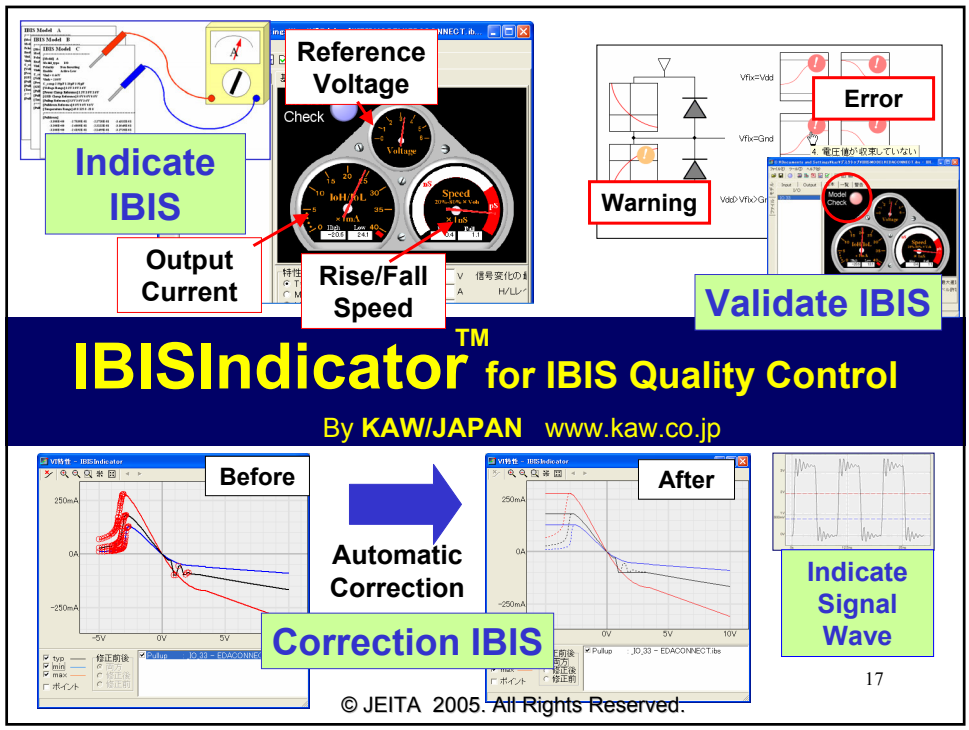


JEITA IBIS Model Portal Site Contents

- **IBIS Documentations**
  - **COOK BOOK**
- **IBIS Library**
  - **Instruction manual**
  - **IBIS Model Storage rack**
- **IBIS Training / IBIS E-Learning**
- **IBIS Free Tool**

Support for IBIS Users

16



17

Thank you for all the help

EIA/IBIS Committee!

18

IBIS and Power Delivery Systems

Jiang, Xiangzhong
Li, Jinjun
Zhang, Shengli

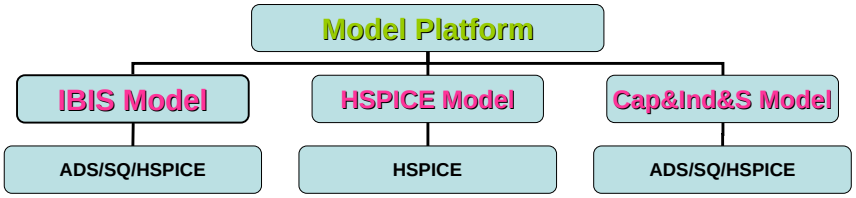
Huawei Technologies, China

- IBIS history in Huawei

- A accurate Simulate Model is first element of successful SI , and the difficult step.
  - 1999 SI dept. founded
  - 2000 Test board
  - simulate arithmetic study
  - 2001 Mr. Bob Ross visit Huawei and lecture
  - IBIS Membership
  - 2001 Modeling Group founded
  - Track Industry Model development
  - 2003 ibischk4 fund
  - Now Asian IBIS Summit 2005

•2 Model Platform in Huawei

•Total simulation Model solution



•3 IBIS Validation

•Ibischk3

•Syntax Errors and Warnings

•Common Errors and Warnings

•Structural Errors and Warnings

•Non-monotonicity Warnings

•Extraction Errors and Warnings

•3 IBIS Validation

- •IBIS file check(correct&Completeness,Databook)
- •IBIS Properties
- •Component Properties
- •[pin]list
- •Package&pin Properties
- •C_pin L_pin R_pin
- •Model_type
- •C_comp
- •[Voltage Range]
- •Vinh,Vinl
- •Vmeas Vref Rref Cref
- •Max/Min Data condition
- •VI Properties
- •VT Properties

•3 IBIS Validation

- •Simulate
- •Spice Correlation
- •Voltage Swings[high/low,over]
- •Timing Test Load Response
- •Measure

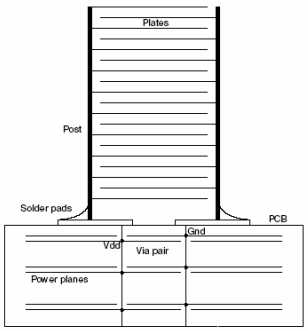
Simulation Platform of Power Integrity Based on Distributed Spice Circuit Models of Components

- Huawei spice circuit model library of capacitor
- Huawei simulation platform of power integrity

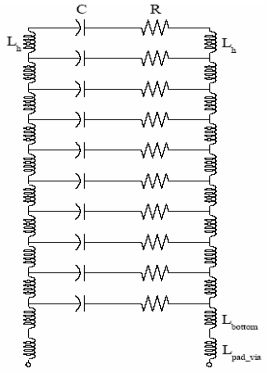
Background

- It is a great challenge to design a power distribution system capable of delivering large amounts of current at low voltage, and decoupling capacitors must be chosen and placed to optimize its performance .
- Simulation of power integrity can improve the capability of design and analysis for complex power distribution system efficiently.
- Modeling passive component is still the emphases of simulation of power integrity because of the bottle-neck of noise model of IC.
- The distributed circuit model of component is appropriate for SPICE simulation and analysis programs that optimize the use of discrete capacitors in PDS.

Distributed circuit model of ceramic capacitor



Cross section of discrete capacitor mounted on PCB power planes



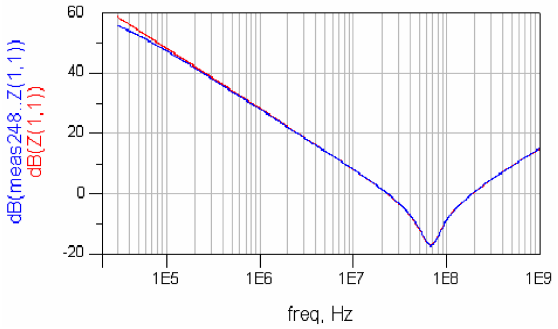
Distributed circuit model for SPICE derived from construction of ceramic capacitor

The spice netlist of 0.01uF ceramic capacitor

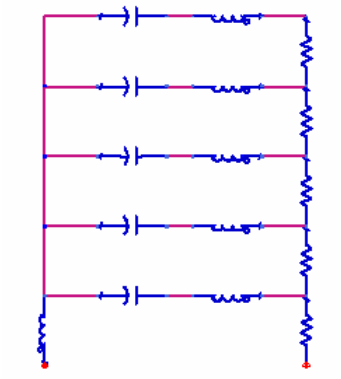
```
.subckt C_08070247 1 5
+ esr=1m loopInductance=1n
lloop 1 2 loopInductance
Ll1   2          3a       4.241181e-010 h
C11   3a         32a      8.785720e-010 f
Rl1   32a           4a              7.684703e-001 ohm
Lr1   4a         3        4.241181e-010 h
Ll2   3a         5a        1.439540e-011 h
C2    5a              31a          8.785720e-010 f
R2    31a        6a        7.684703e-001 ohm
Lr2   6a         4a        1.439540e-011 h
Ll3   5a         7a        1.439540e-011 h
C3    7a         30a      8.785720e-010 f
R3    30a        8a        7.684703e-001 ohm
Lr3   8a         6a        1.439540e-011 h
Ll4   7a         9a              1.439540e-011 h
C4    9a         29a      8.785720e-010 f
R4    29a        10a       7.684703e-001 ohm
Lr4   10a        8a        1.439540e-011 h
Ll5   9a         11a       1.439540e-011 h
C5    11a        28a      8.785720e-010 f
R5    28a        12a       7.684703e-001 ohm
Lr5   12a        10a       1.439540e-011 h
Ll6   11a        13a       1.439540e-011 h
C6    13a        27a      8.785720e-010 f
R6    27a        14a       7.684703e-001 ohm
Lr6   14a        12a       1.439540e-011 h
Ll7   13a        15a       1.439540e-011 h
C7    15a        26a      8.785720e-010 f
R7    26a        16a       7.684703e-001 ohm
Lr7   16a        14a       1.439540e-011 h
Ll8   15a        17a       1.439540e-011 h
C8    17a        25a      8.785720e-010 f
R8    25a        18a       7.684703e-001 ohm
Lr8   18a        16a       1.439540e-011 h
Ll9   17a        19a       1.439540e-011 h
C9    19a        24a      8.785720e-010 f
R9    24a        20a       7.684703e-001 ohm
Lr9   20a        18a       1.439540e-011 h
Ll10  19a        21a       1.439540e-011 h
C10   21a        23a      8.785720e-010 f
R10   23a        22a       7.684703e-001 ohm
Lr10  22a        20a       1.439540e-011 h
rl 3 4 esr //  esr in ohms
rdum 2 3 10Meg //  resistor to make dc path
vsense 4 5 0 ac=0
.ends C_08070247
```

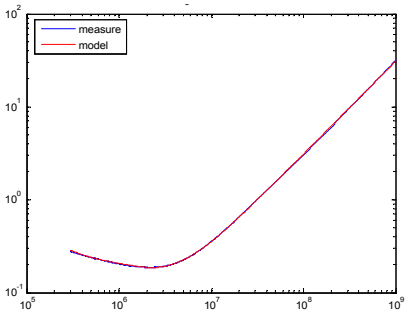
Element values model was extracted from measured s-parameter based on Monte Carlo method

Distributed circuit model simulation compared to measured 0.01uF capacitor



Spice circuit model of 10uF Tantalum capacitor





The spice netlist of 10uF Tantalum capacitor

```
.subckt C_08020059 1 5
+ esr=1m loopInductance=1n
lloop 1 2 loopInductance //  loop or mounted inductance in henries c1 2 1a capacitance
L0   2          3a       1.328655e-009 h
C1   3a         32a     2.090239e-006 f
L1   32a        4a       4.893012e-010 h
R1   4a         3        2.133079e-001 ohm
C2   3a         31a       3.609295e-006 f
L2   31a        6a       1.015527e-009 h
R2   6a         4a       3.549960e-001 ohm
C3   3a         30a      1.426664e-007 f
L3   30a        8a       1.952736e-009 h
R3   8a         6a       8.641232e-001 ohm
C4   3a         29a      5.113291e-007 f
L4   29a        10a      8.165504e-010 h
R4   10a        8a       7.889731e-001 ohm
C5   3a         28a      1.839965e-007 f
L5   28a        12a      6.076517e-010 h
R5   12a        10a      1.088326e+000 ohm
r1 3 4 esr //  esr in ohms
rdum 2 3 10Meg //  resistor to make dc path
vsense 4 5 0 ac=0
.ends C_08020059
```

Element values model was extracted from measured s-parameter based on Monte Carlo method

HUAWEI Simulation platform of power integrity

- Cadence SQPI based two-dimension transmission line theory

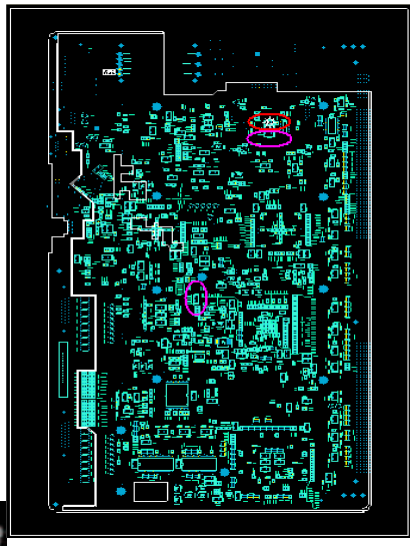
  S-parameter:

  Spice model: high-efficiently

- Ansoft Siwave Based electromagnetic theory

  S-parameter

Simulation of Power integrity for one product

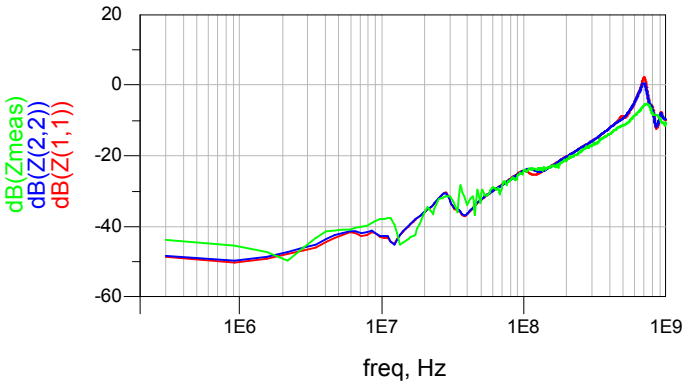


Total pins: 13022 pins

Stackup: 12 layers

Power consumption: 3.3VX20A

Simulated and measured impedance of power network for the product



Red: s-parameter; Blue: spice mode; Green: measurement

Conclusion

•HUAWEI hold completed and accurate spice model library of passive component;

•Simulation platform of power integrity based on spice model library has been founded;

•The simulated impedance proved to be consistent with measurement and can be used to solve the power noise problem of product.

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Power Delivery System, Signal Return Path, and Simultaneous Switching Output Analysis Guidelines

Asia IBIS Summit

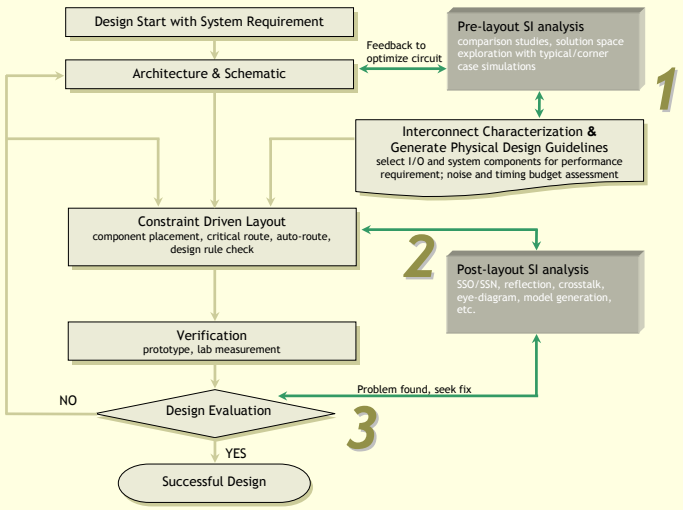
Raymond Y. Chen
Sam Chitwood
Sigrity, Inc.

December 2005

SIGRITY

Design Flow

Signal and Power Integrity Analysis is Performed in Each Stage



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Enhanced Work Flow – Stage 1

Pre-layout stage — generate high speed design guidelines

1. PDS design guidelines
   - Stackup what-if
   - Copper weight determination
   - Decap placement for P/G current
   - VRM sense line optimization
2. Signal return path guidelines
   - Via rules for layer transitions
   - Choose signal layer references
   - Crossing split-planes warning
   - Decap placement for enhancing signal return paths
3. SSO guidelines
   - Timing impact evaluation, SSO push-out timing budget
   - False switching prevention, victim nets (stuck-high, stuck-low), noise amplitude budget
   - Bus scheduling and driver slew rate control
   - Decap placement to reduce SSO noise
4. EMI early prevention guidelines
   - Via stitching rules
   - Stackup variations
   - Retreated plane rule
   - Power island/ring, mix-signal isolation guide
   - Radiation harmonics vs. P/G resonant frequencies correlation guide

3

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Enhanced Work Flow – Stage 2

Post-layout stage — verification, design rule check, constraint management

1. PDS design check
   - Identify over- and under-voltage conditions for all devices on the distribution
   - Pinpoint insufficient routing (neckdowns) that causes excessive voltage drop
   - Locate current distribution "hot spots" that introduce unnecessary thermal stress
   - Identify via, bump, and ball currents above/below user-specified limits
   - Verify target impedance is met
2. SSO Simulation
   - Worst corner cases, even/odd mode switching, maximum delay, skew, over/under shoot, ringback
   - Eye-diagrams and pseudo-random bit streams (PRBS)
3. Decap Optimization
   - Decap number reduction - remove extra components to save routing space, cost and enhance product reliability
   - Decap value adjustment – address resonant frequencies
4. Model generation – deliver to other groups, or use in system-level simulations
   - Core power system model
   - I/O and return path modeling — using S-parameter models to capture signal distribution system and power distribution system interactions
   - IR drop DC circuit model

4

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Enhanced Work Flow – Stage 3

Problem resolution stage — evaluate design change options to reduce re-spin

1. PDS structure options
   - Add more decaps
   - Reduce pwr/gnd plane separation
   - Add more plane area (interplane capacitance)
   - Add more P/G shorting vias
   - Convert signal pin to P/G pin – e.g. FPGA footprint
2. Signal return path options
   - Reduce via transitions
   - Eliminate reference plane changes
   - Add decap across plane splits
   - Change signal vs. P/G ratio and distribution pattern, add more return vias or decaps
3. SSO options
   - Change driver slew rate and switching parameters
   - Add decaps to reduce SSO noise
4. EMI options
   - Add stitching vias near board edges
   - Adjust power island/ring
   - Add decaps to adjust radiation harmonics and P/G resonant frequencies

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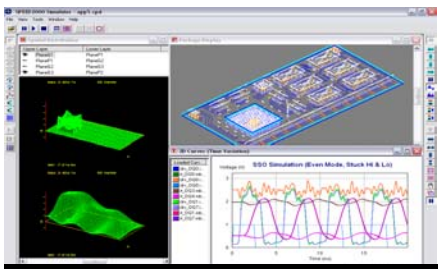
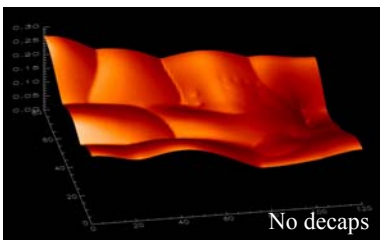
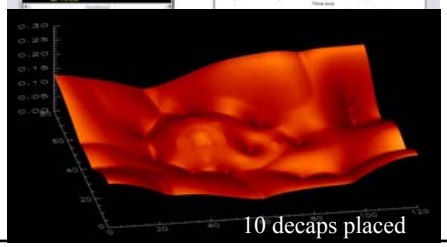
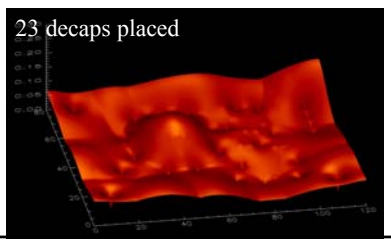
Delta-i Noise Simulation and Decoupling Capacitor Placement

Spatial Distribution of Power / Ground Noise on a PCB









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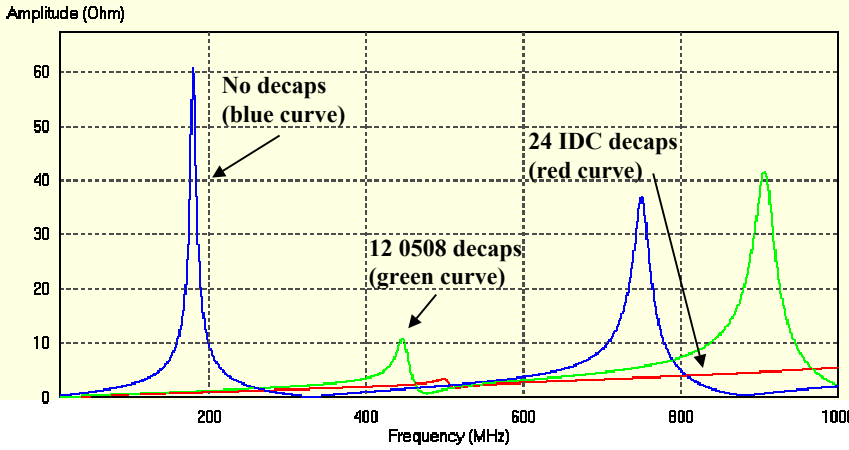
Power / Ground Impedance Extraction

PCB impedance at one location; number of decoupling caps is varied

Objective – eliminate/reduce impedance spikes within the frequency range of interest



7

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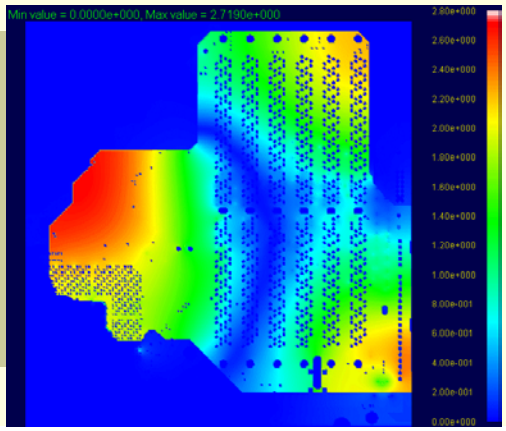
Optimize Decoupling Capacitor Selection and Placement for the Entire Distribution

- Identify impedance "hot spots"
  - Board location
  - Target frequency
- Place decoupling capacitors in areas exceeding target impedance
- Select ideal component values
- Analyze power / ground resonance
- Minimize component costs with optimized decoupling solutions



8

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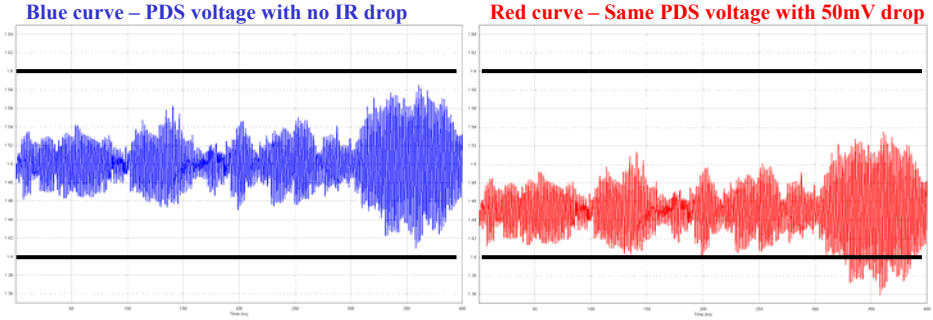
PDS Optimization – IR Drop Analysis

ASICs require a constant and stable voltage supply for proper operation

- The voltage supply is allowed to deviate by an amount specified by the vendor
- This deviation (or fluctuation) of the supply is composed of DC loss and AC noise
- The IR drop tolerance is commonly 5% (or less) of the nominal operating voltage
- If the tolerance is constant, then a reduction in DC loss yields a larger AC noise budget

Blue curve – PDS voltage with no IR drop

Red curve – Same PDS voltage with 50mV drop



9

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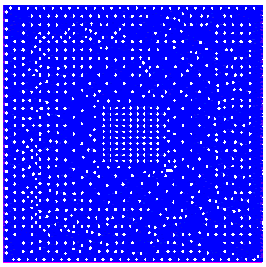
Why is DC Analysis Important?

- Numerous factors have combined to exacerbate the problem
  - Core voltage levels continue to drop: 1.2V and less are now common
  - As voltage is reduced, current requirements typically increase: IR drop = I * R
  - Less layers and higher densities have reduced the available area for power nets
  - Antipads around vias perforate the planes and can overlap – the "Swiss cheese" effect
  - Complex geometries make analysis with hand calculations difficult, if not impossible

Neck-down



Swiss Cheese on solid plane

Dynamic trace routing can cut off the PDS

- IR Drop is a system level problem – analysis of the entire power distribution system (PDS) is necessary to optimize the end-to-end voltage margins for every device on the distribution

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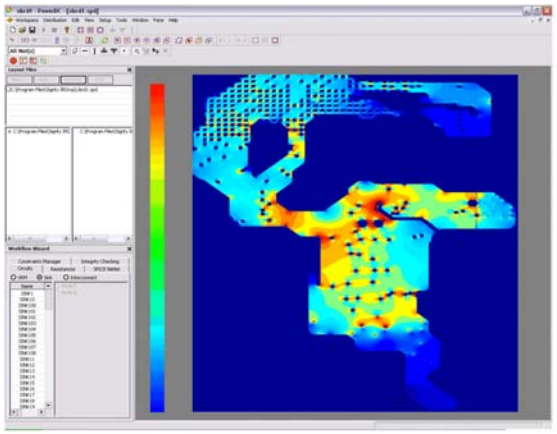
PDS Optimization – IR Drop Analysis

Typical Objectives of DC Analysis:

- Pinpoint critical voltage distributions and IR drop issues at multiple component locations
- Optimize IR drop-sensitive Package and Board device locations
- Locate current distribution "hot spots" that may lead to current density and thermal issues
- Optimize crucial VRM (voltage regulator) sense line locations and nominal output voltage settings
- Quantify total path and loop resistances of the complex PDS
- Identify hard-to-find, high resistance areas
- Conduct conclusive IR drop analysis for the complete IC Package and Board PDS



11

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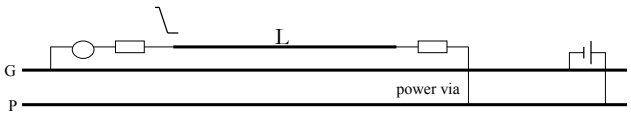
Signal Integrity Optimization – Effects of Signal Return Path Discontinuity (RPD) and SSN

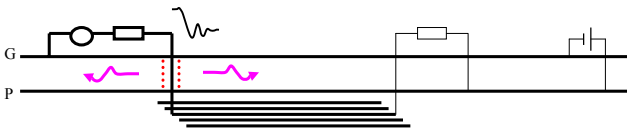
One signal switching without reference plane change



One signal switching with reference plane change,
Red:signal current Blue:Displacement return current Pink:power/ground voltage fluctuation due to EM waves between planes

Multiple signals switching with reference plane change,
Red: more signal currents

Pink: stronger power/ground voltage fluctuations due to EM wave between planes. More signal waveform distortion and skew.



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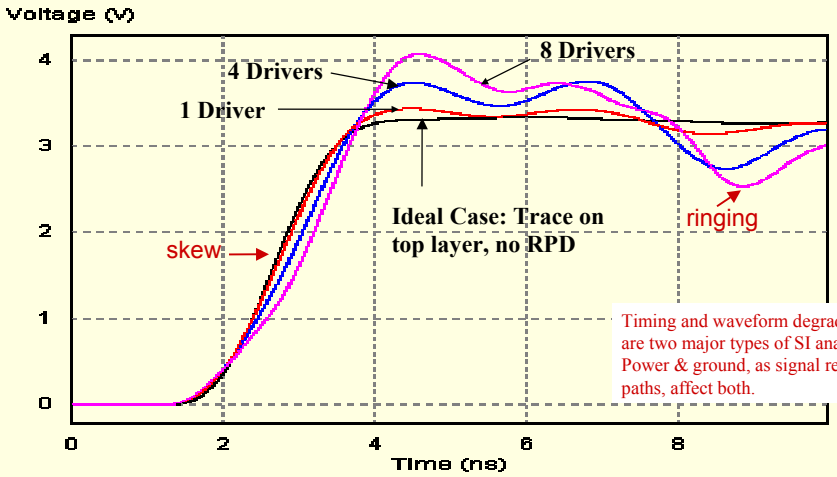
Receiver Waveforms under the Influence of Simultaneous Switching Noise (SSN)

(The number of simultaneous switched drivers was varied, no decoupling caps were used, results from *Speed2000*)



Timing and waveform degradation are two major types of SI analysis. Power & ground, as signal return paths, affect both.

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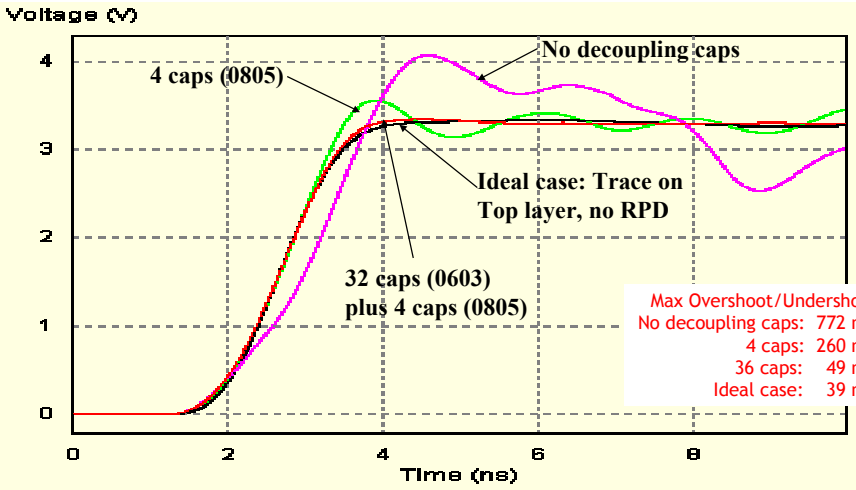
Effects of Decoupling Caps on Receiver Voltage with 8 Drivers Switching Simultaneously

(SSN reduction, results from *Speed2000*)



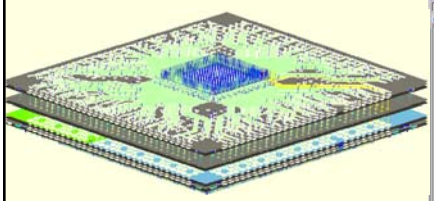
Max Overshoot/Undershoot
No decoupling caps: 772 mV
4 caps: 260 mV
36 caps: 49 mV
Ideal case: 39 mV

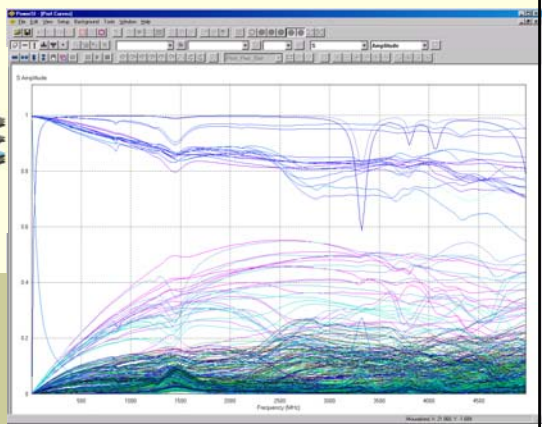
Why use S-parameters for SSO analysis?

- Lumped RLC models are a low frequency approximation
  - A single RLC segment cannot accurately model propagation delay
  - Frequency-dependent, broadband coupling is mandatory at GHz switching frequencies
  - Power / ground impedance is highly frequency dependent – RLC cannot model this easily
- Power / ground structures affect the I/O signal's performance
  - Realistic power distribution systems (PDS) do not supply a constant, ideal voltage
  - Large, parallel busses create huge current transients (large dI/dt)
  - PDS noise degrades the signal quality of a driver's output (SSO pushout for example)
  - Resonance in the PDS significantly increases via crosstalk and impedance
- S-parameters capture the frequency dependent response and coupling of the power / ground structures and I/O signals

Broadband Package Model Extraction

34-port mixed PDS and I/O S-parameters, 100 Hz - 5 GHz





The 16 signal nets in the left corner of the package are of interest.

An equivalent circuit model is extracted for these 16 signal nets, together with the power and ground nets.

Suggestions for S-parameter Extraction

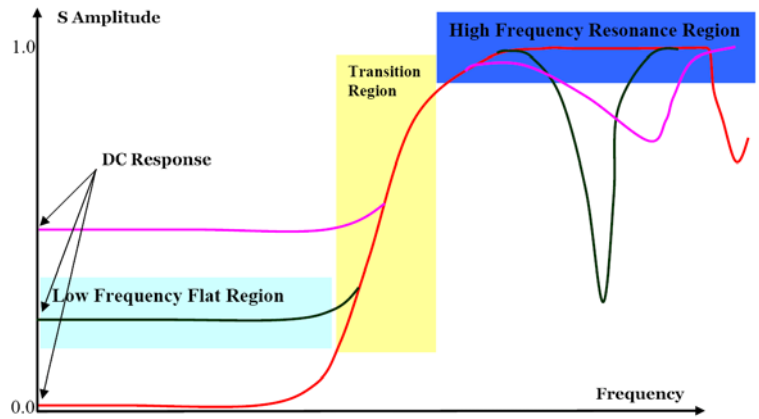
Only extract the nets of interest

- Example: don't extract the PCI bus if you're only interested in DDR
- Typical extractions are 8 to 32 data nets; 64+ nets only when necessary
- Use current mirrors (multipliers) for large, parallel busses

Set an appropriate frequency sweep

- ~100 Hz - 10 MHz: Log sweep with at least 5 points per decade
- 10 MHz - 2+ GHz: Linear sweep with a 10 or 20 MHz increment
- The low frequency data is important!

Typical PDN return-loss curve



The low frequency flat region and the transition region must have a sufficient number of data points to enable the final simulator to accurately extrapolate the entire curve.

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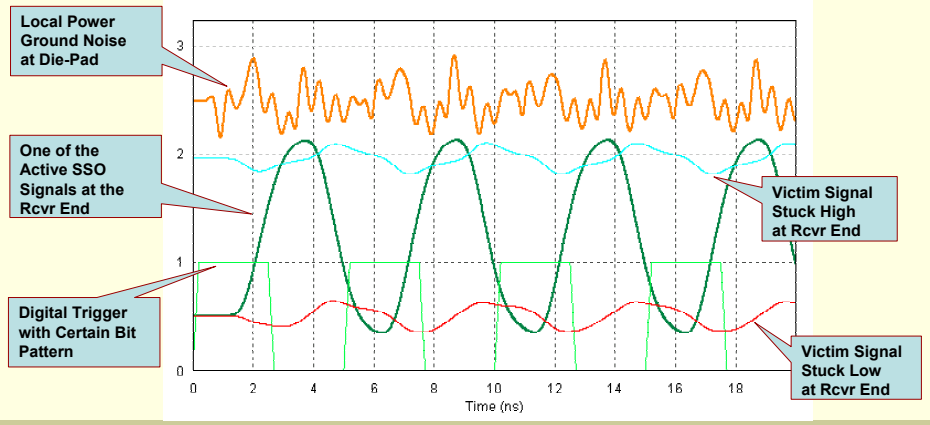
SSO Methodology - Stuck Bits



Set two of the data bits as stuck high and stuck low victims. These results can assist with a more in-depth analysis of the power and ground rail fluctuations.

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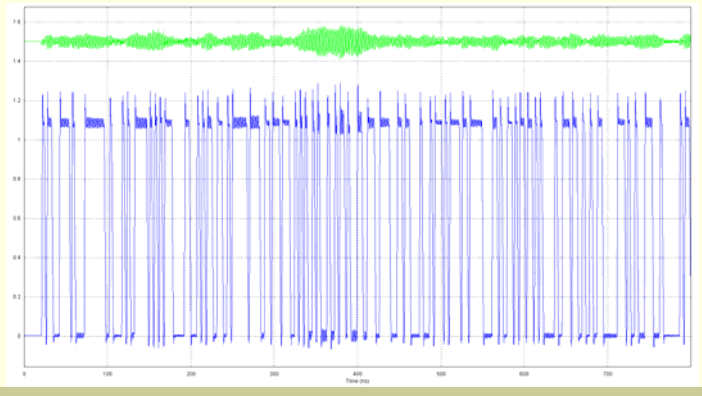
SSO Methodology - PRBS



The worst case power/ground noise does not always occur with 1010… transitions. Random bit patterns will reveal the impact of PDS impedance problems that would otherwise be missed with repeating 1010... patterns.

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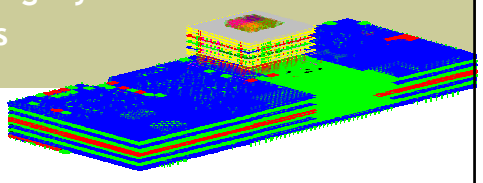
Summary

- Optimizing the PDS impedance will reduce the supply noise, improve signal integrity, and generate less EMI
  - The PDS voltage noise has AC and DC components
  - Decoupling and IR drop analysis will maximize voltage margins of the complete system
- Capturing the interactions between the PDS and the I/Os is necessary for accurate signal integrity and SSO analysis
  - Ensure that signal return currents are accurately modeled, because unmanaged return currents can cause lots of PDS related noise phenomena
- Stuck bits and a PRBS stimulus are valuable techniques in identifying underlying problems for I/Os and the PDS

Thank You!

Advanced Power and Signal Integrity Solutions
for Chips, Packages and Boards



Splitting C_comp for Power Integrity Simulations

Zhiping Yang, Ph.D.
Cisco Systems, Inc.
(Now with Apple Computer, Inc.)

Asian IBIS Summit in ShenZhen, China
12/6/2005

Acknowledgment

- The author would like to thank Cisco Systems, Inc. for the support and approval of this presentation material
- The author would like to thank Apple Computer, Inc. for providing travel arrangements to make this presentation happen
- The author would like to thank Randy Wolf from Micron for his support and help on HSPICE buffer model

Content

- Why C_comp and its split ratio are important for power integrity simulations?
- The procedures to extract the C_comp and C_decap values from HSPICE simulations
- Simulation results for Micron U27_a_dq buffer

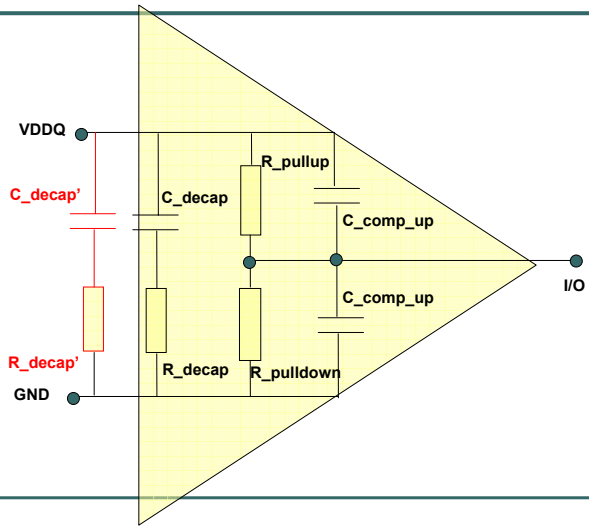
Why C_comp and its split ratio are important for power integrity simulations?

C_comp could impact the power integrity simulations in following ways:

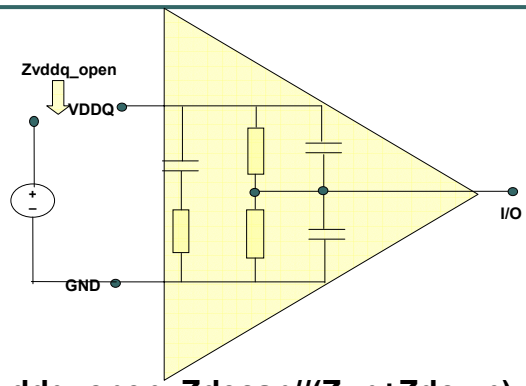
- C_comp at non-switching I/O could act as effective local decoupling caps. The ratio has a big impact.
- C_comp split ratio heavily impacts the noise level coupled from power supply to quite I/O pins, especially at high frequency.
- C_comp split ratio will have direct impact on dynamic current distribution for switching I/O buffers

Note: C_comp split ratio has no impact on SI simulations when voltage supply is ideal.

Simplified I/O model for IBIS specification



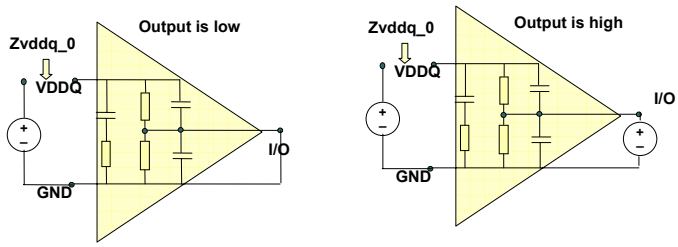
Zvddq_open



Zvddq_open=Zdecap//(Zup+Zdown) (1-1)

Yvddq_open=Ydecap+(Yup*Ydown)/(Yup+Ydown) (1-2)

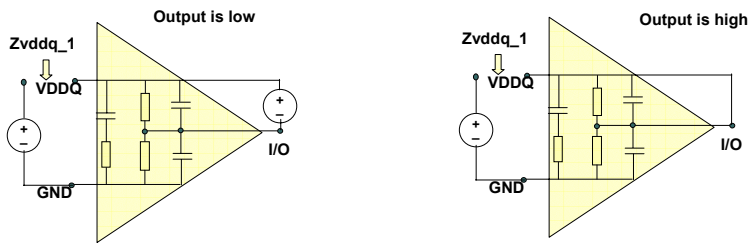
Z_vddq_short_to_gnd



Zvddq_0=Zdecap//Zup (2-1)

Yvddq_0=Ydecap+Yup (2-2)

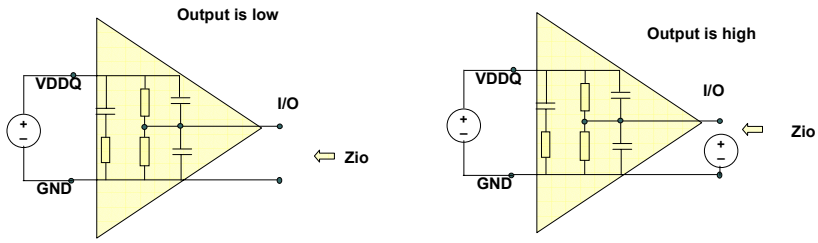
Z_vddq_short_to_pwr



Zvddq_1=Zdecap//Zdown (3-1)

Yvddq_1=Ydecap+Ydown (3-2)

Z_io



Zio=Zdown//Zup (4-1)

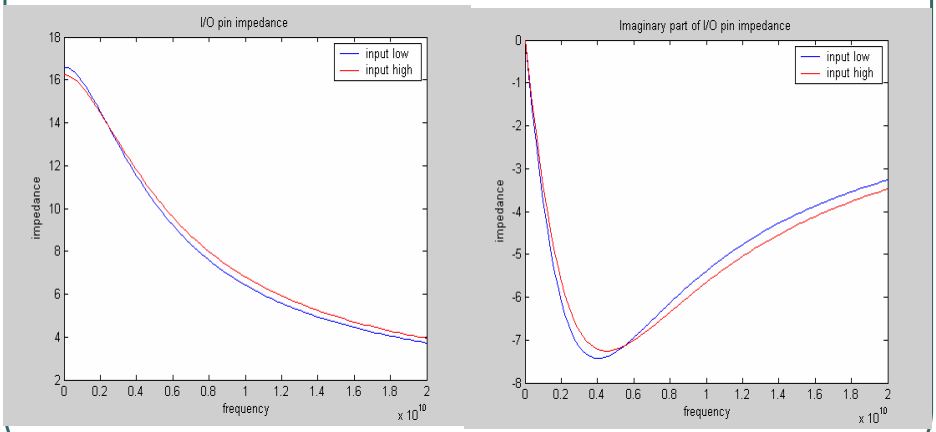
Yio=Ydown+Yup (4-2)

Extraction of Yup, Ydown and Ydecap

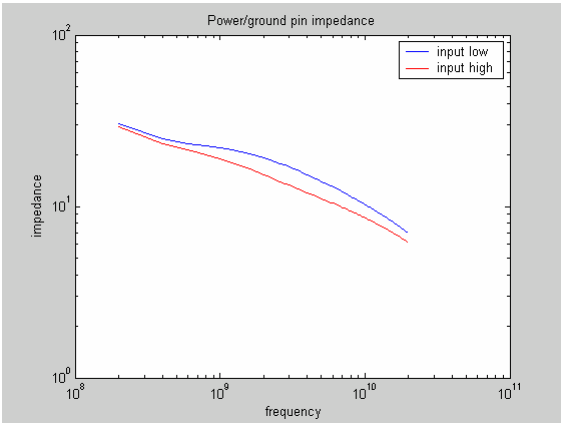
- Yvddq_0=Ydecap+Yup (2-2)
- Yvddq_1=Ydecap+Ydown (3-2)
- Yio=Yup+Ydown (4-2)

- Yup=(Yvddq_0+Yvddq_1+Yio)/2-Yvddq_1 (5-1)
- Ydown=(Yvddq_0+Yvddq_1+Yio)/2-Yvddq_0 (5-2)
- Ydecap=(Yvddq_0+Yvddq_1+Yio)/2-Yio (5-3)

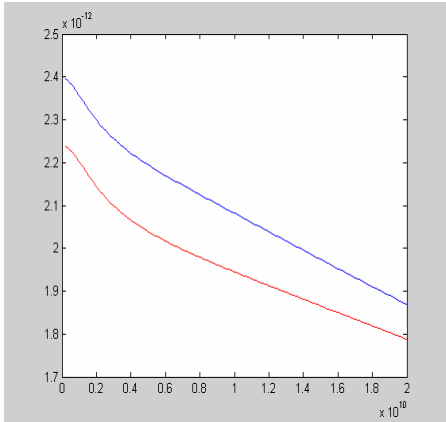
I/O pin impedance



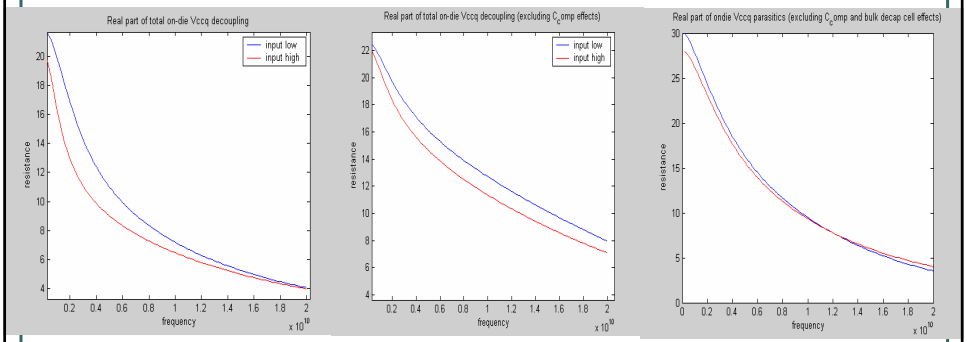
Power/ground impedance when I/O pin is open



I/O pin capacitance



Vccq parasitic resistance

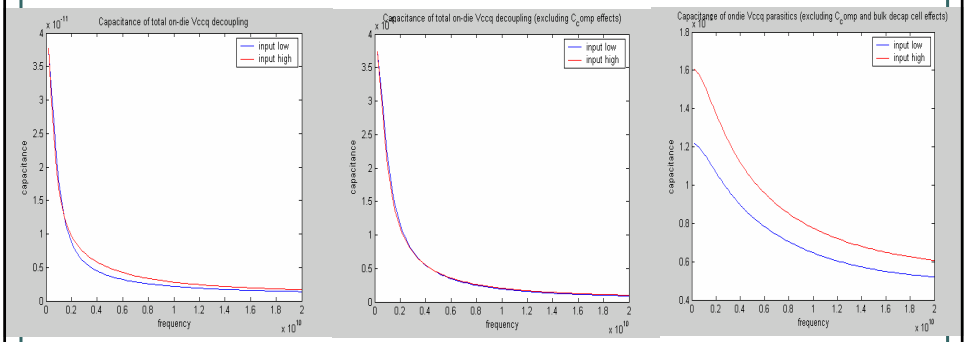


Everything included

C_comp effect excluded

C_comp and lumped decap cell effect excluded

Vccq parasitic capacitance

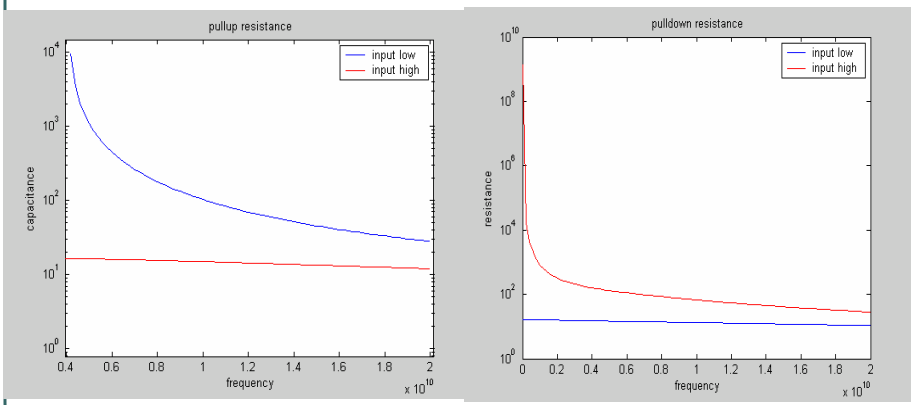


Everything included

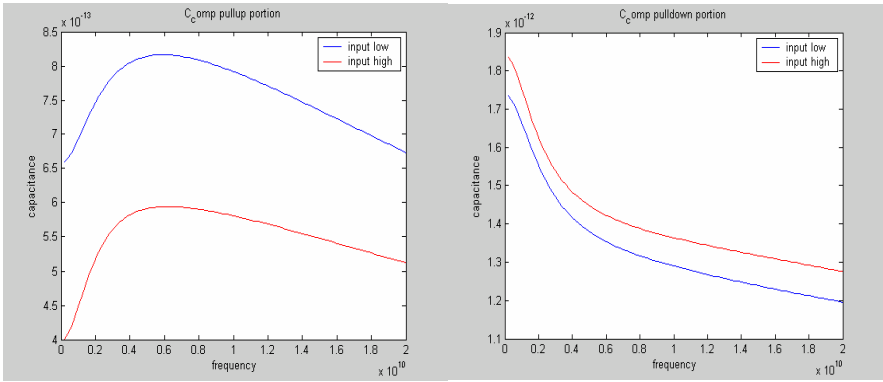
C_comp effect excluded

C_comp and lumped decap cell effect excluded

Pull_up and Pull_down resistance



Pull_up and Pull_down capacitance



Conclusions

- C_comp is frequency and state dependent
- C_comp split ratio is also frequency and state dependent
- C_comp and its split ratio are very important factors for correct power integrity simulations
- Existing C_comp and I/V table may not completely model the frequency dependent property of I/O buffer, even at steady state.

Q&A

?

IBIS在信号完整性分析中的应用
Using IBIS for SI Analysis

Lance Wang, ZhangMin Zhong
Cadence Design Systems, Inc.
Asian IBIS Summit, Shen Zhen, P.R. China
December 6, 2005

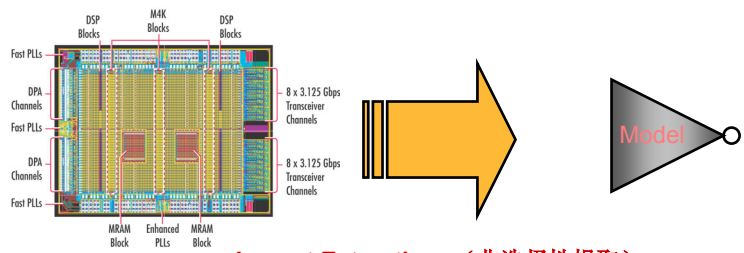
Outline

- What happened on IBIS （IBIS历史）
- Why IBIS （IBIS的好处）
  - Speed and Accuracy （速度和精度）
  - Industrial Examples （工业化例子）
- Advanced IBIS Technologies （加强型IBIS技术）
  - Complex-IO Devices （复杂I/O器件）
  - Macromodeling is a solution （宏模型解决方案）
  - Experiences and Industrial Examples （经验和工业化例子）

Outline

- **What happened on IBIS** （IBIS历史）
- Why IBIS
  - Speed and Accuracy
  - Industrial Examples
- Advanced IBIS Technologies
  - Complex-IO Devices
  - Macromodeling is a solution
  - Experiences and Industrial Examples

What happened on IBIS
- Spice Transistor Level Models（晶体管级模型建模流程）

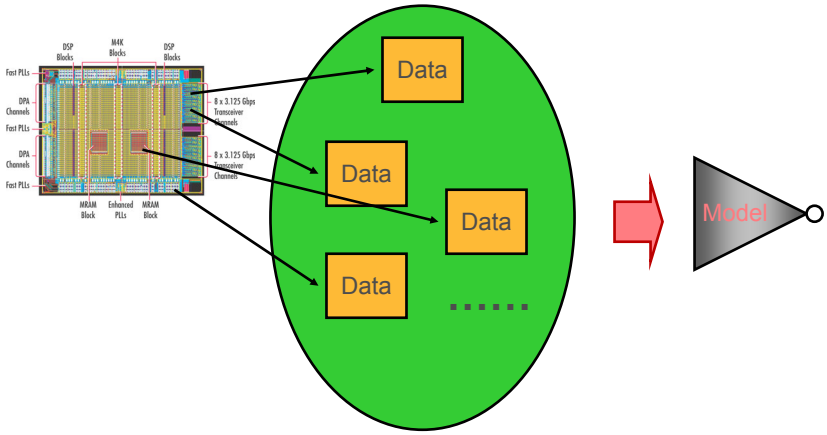


Layout Extractions（非选择性提取）

-Very Complicated
-A lots of unusable stuff
-Too slow in the simulations

What happened on IBIS

- Behavioral Models （行为级模型建模流程）

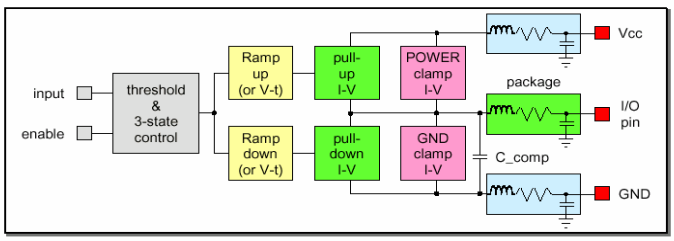


Behavioral Extractions 选择性提取

What happened on IBIS

- IBIS is behavioral Model （IBIS是行为级模型）

IBIS model



Block diagram of CMOS buffer

A basic IBIS model consists of:

four I-V curves: - pullup & POWER clamp
- pulldown & GND clamp

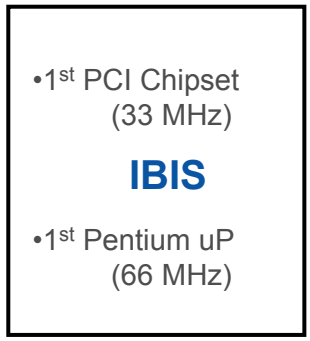
two ramps: - dV/dt_rise
- dV/dt_fall

die capacitance: - C_comp

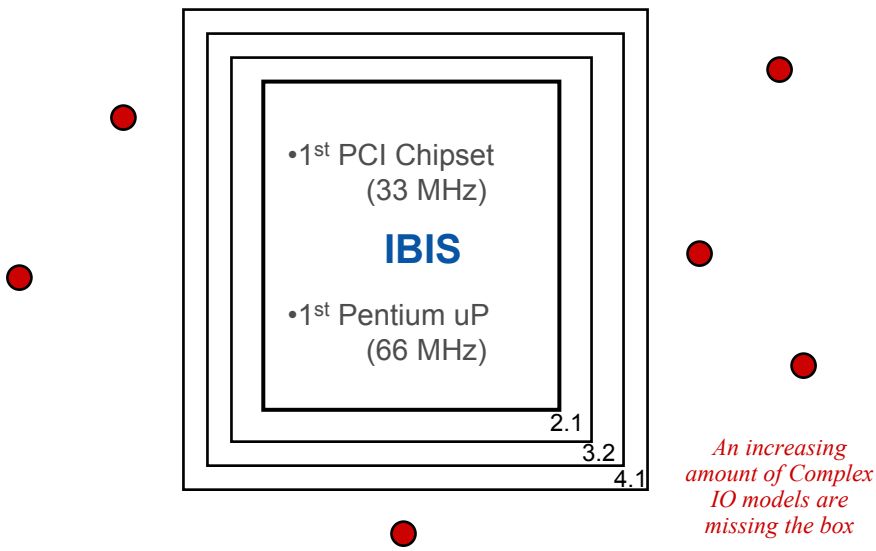
packaging: - RLC values

for each buffer on a chip

What happened on IBIS - The Original "Box"

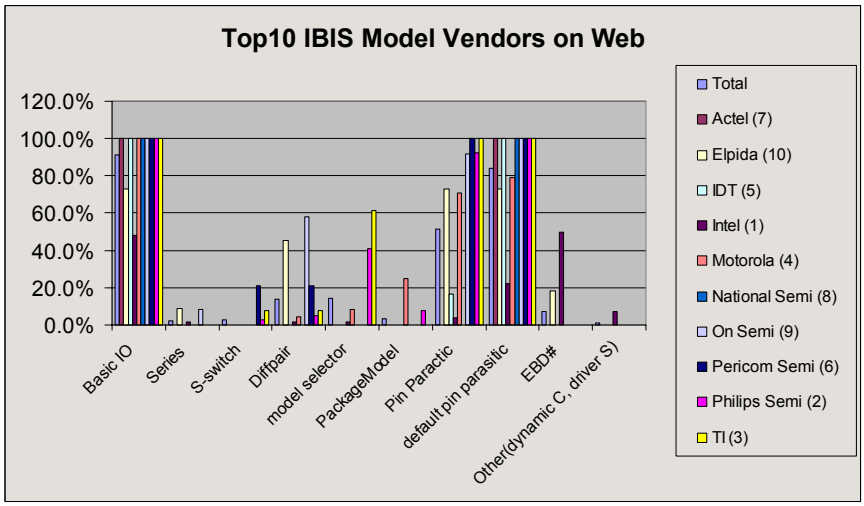


…and the "Box" did grow



An increasing amount of Complex IO models are missing the box

What happened on IBIS
- IBIS Model Vendors（IBIS模型提供者）



What happened on IBIS
- IBIS in EDA Tools（IBIS在EDA工具中的应用）

- Major EDA Simulators are supporting IBIS now
  - Cadence
  - Mentor
  - [illegible]
  - Agilent

SPICE Simulators are taking IBIS now !!!

And many, many more……

Outline

- What happened on IBIS
- **Why IBIS （IBIS的好处）**
  - **–Speed and Accuracy （速度和精度）**
  - **–Industrial Examples （工业化例子）**
- Advanced IBIS Technologies
  - – Complex-IO Devices
  - – Macromodeling is a solution
  - – Experiences and Industrial Examples

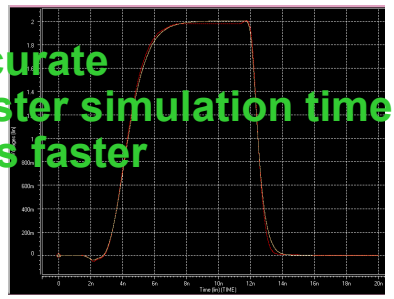
  cadence

Why IBIS （IBIS的好处）
-Speed and Accuracy （速度和精度）

- Behavioral data in Spice simulators

I(pad) = Ipd(V(pad)-V(gnd))*Wd(t) + Icd(V(pad)-V(gnd_c))
+ Ipu(V(pad)-V(pwr))*Wu(t) + Icu(V(pad)-V(pwr_c))

- **Results are accurate**
- **Much, much faster simulation time**
  - **20-1000 times faster**
- **IP Protected**



HSpice Transistor Model vs. IBIS Model

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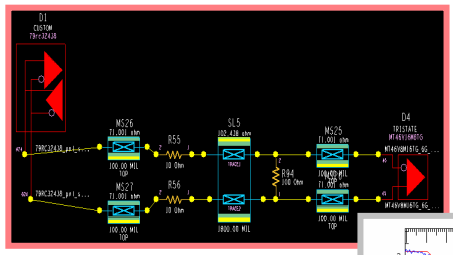
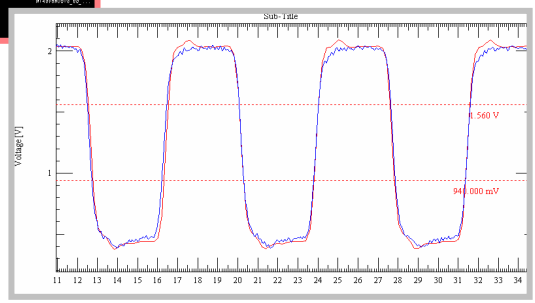
Why IBIS （IBIS的好处）
- Industrial Examples（工业化例子） (133MHz)



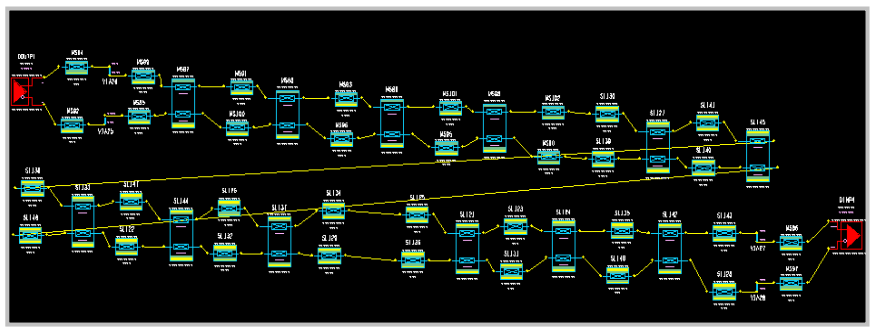
Driver: IDT 79RC32438

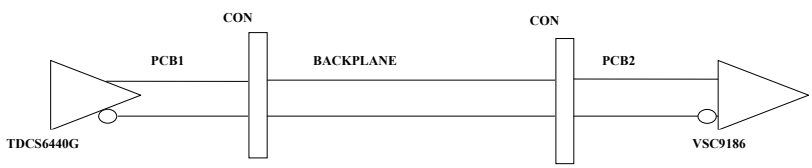
Receiver: Micron MT46V16M8TG



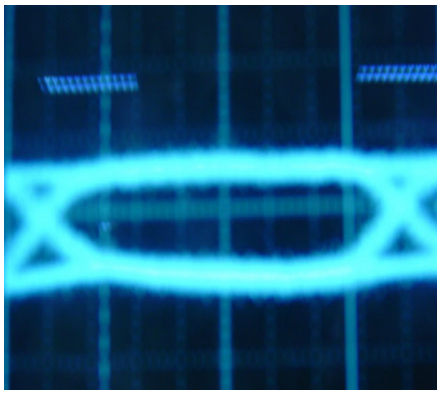
Blue: Measured result　　Red: Simulated result

Why IBIS （IBIS的好处）
- Industrial Examples（工业化例子）(622Mbps)



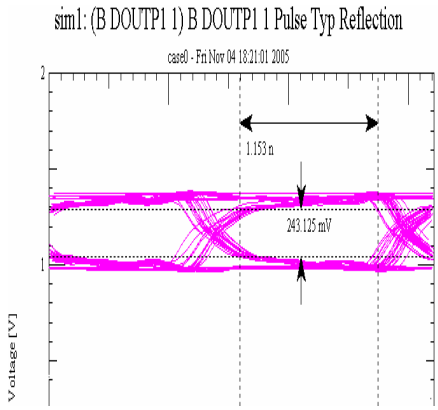


Why IBIS （IBIS的好处）
- Industrial Examples（工业化例子）(622Mbps)



Eye Height: 210mv

Eye Width: 1.1ns



Eye Height: about 240mv

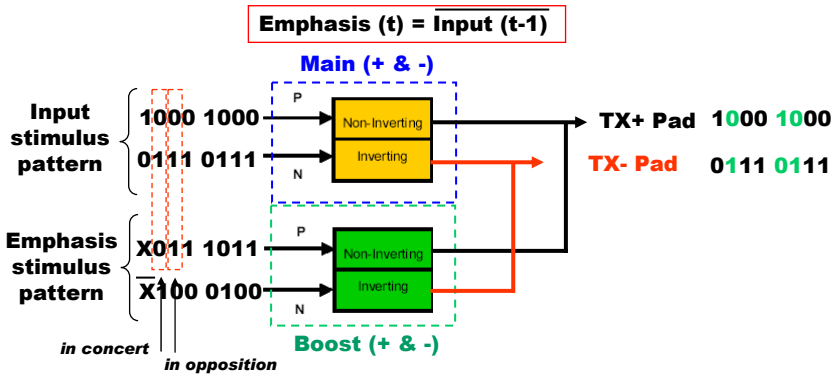
Eye Width: about 1.15ns

Outline

- What happened on IBIS
- Why IBIS
  - Speed and Accuracy
  - Industrial Examples
- **Advanced IBIS Technologies（加强型IBIS技术）**
  - **Complex-IO Devices （复杂I/O器件）**
  - **Macromodeling is a solution （宏模型解决方案）**
  - **Experiences and Industrial Examples （经验和工业化例子）**

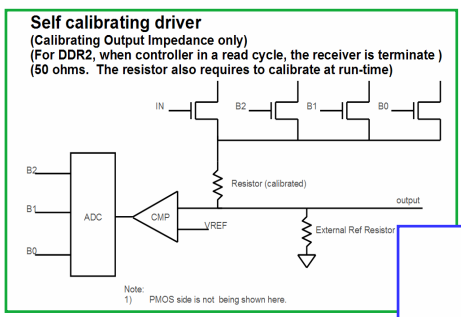
Complex-IO Devices（复杂I/O器件）

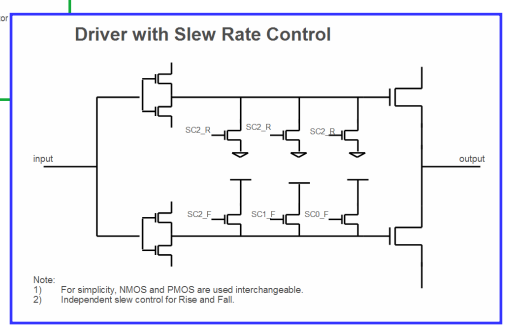
Pre-emphasis预加重/De-emphasis去加重



Picture from Michael Mirmak's presentation in DesignCon East IBIS Summit 2004

Complex-IO Devices（复杂I/O器件）





What is MacroModeling and Why?

KEY Conclusions

Equation-based macromodeling of LVDS drivers

- ❖ Flexible methodology
  - no specific assumption on device internal structure **(preserve IP)**
  - handle drivers with enhanced features (*e.g.*, **control ckts**)
- ❖ **Accurate** and **efficient** macromodel **(5÷10x speed-up)**
- ❖ Ready for advanced **SPICE, VHDL-AMS** implementations
- ❖ Ready **available also for EDA tools** via the **IBIS** multilingual extension

宏模型是一个解决方法

Methodology only

In progress: mapping to LVDS drivers with enhanced analysis

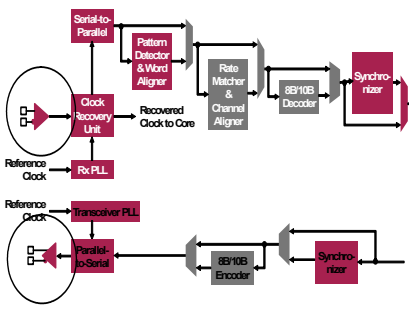
Macromodeling is a Methodology !!!

SPI 2004 SPI 2004 17 EMC group

  cadence

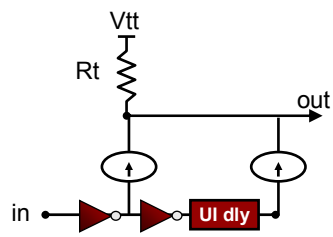
Macromodel from architecture templates
从器件结构中得出宏模型

- Most modern devices are based on known DSP circuit architectures



Known circuit architecture

Match template parameters to Layout model to get an accurate macromodel



Macromodel template with parameters

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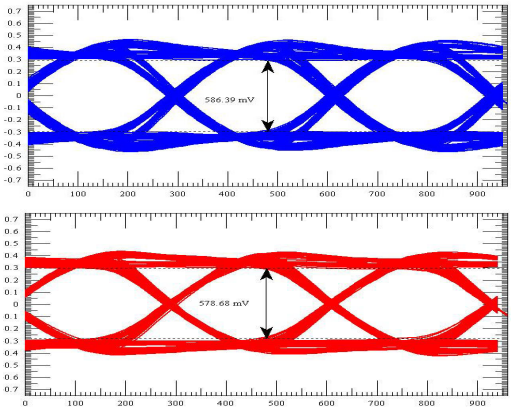
Industry example- Altera Stratix GX

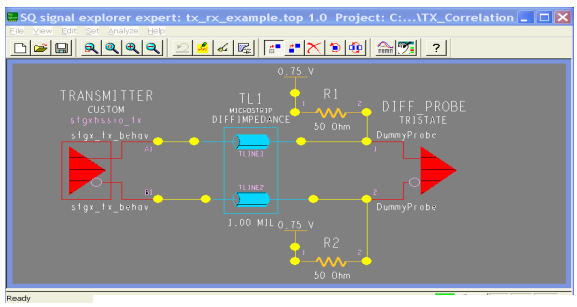
"Altera successfully adapted the MacroModel templates to produce fast and accurate models of our multi-gigabit transceivers. Not only did the resulting model correlate well, it also simulates between 20 to 400 times faster than its transistor-level counterpart. And the model can be easily adjusted to match the behaviors of actual silicon measured in the lab."

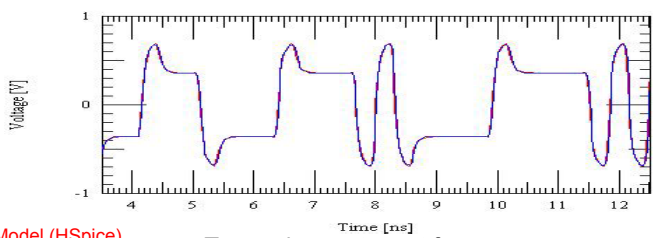


Correlation: MacroModel vs TransistorModel

"Overall, the templates were simple to work with and very valuable amidst the challenges of multi-gigahertz design."

Correlation - Altera Stratix GX

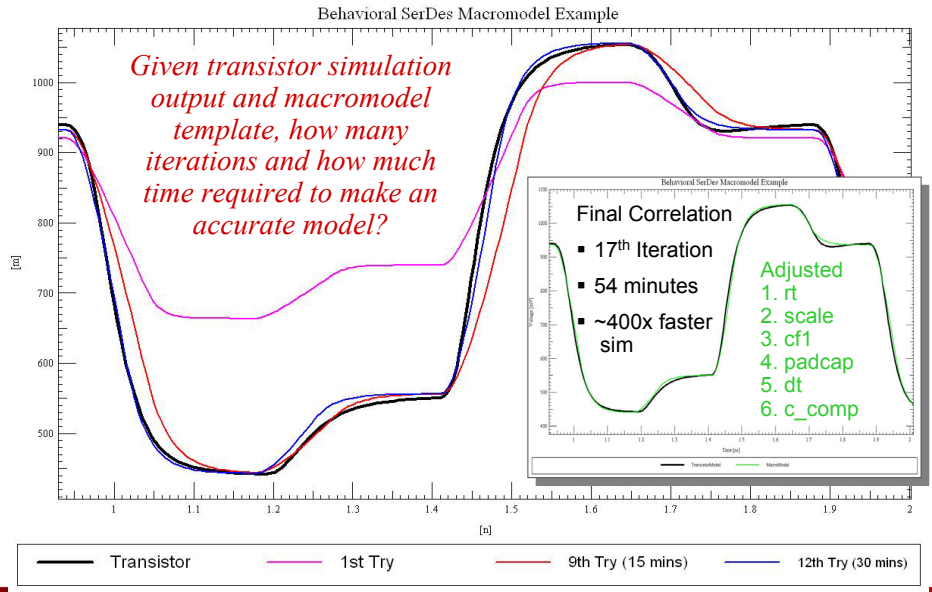




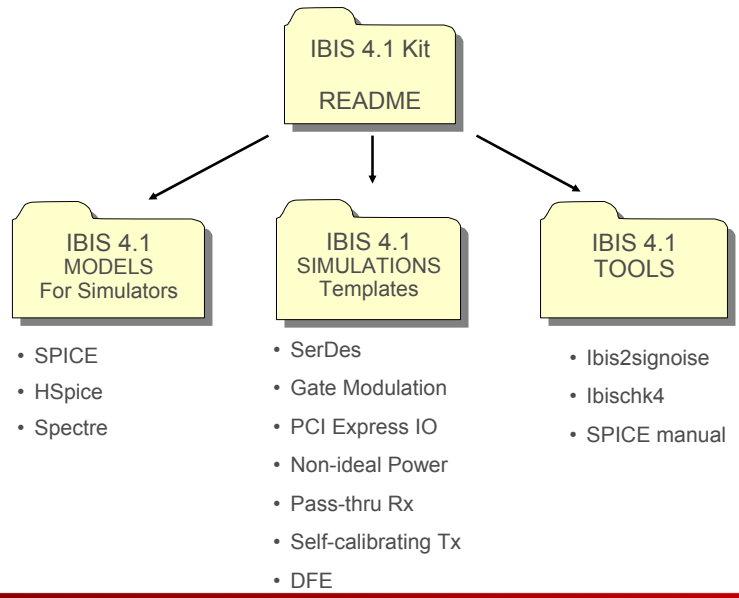
- Transistor Level Model (HSpice)
- Spice Macromodel (Cadence DML)

Transmitter output at factor=5

Case Study: Agere Systems 4 Gbps SerDes



Cadence IBIS 4.1 Kit

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Thank You
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Macromodeling and Multi-GHz Interconnection Simulation

Asian IBIS Summit

Zhu ShunLin

High-Speed System Lab， ZTE Corporation
Zhu.shunlin@zte.com.cn

December 2005

ZTE中兴

Agenda

- Transistor-Level Model versus Behavior-level Model
- Macromodeling of Complex IOs
- Lab Correlation for Macromodels
- Multi-GHz System Interconnect Simulation
- Conclusions

Transistor-level model and Behavior-level model

- SPICE Model
  - Good accuracy
  - models are derived from transistor-level netlist and layout
  - Relatively long simulation time and sometimes convergence problems
  - Intellectual property protection concerns
- IBIS Model
  - Models are derived from measurements and/or full SPICE model simulations
  - Fast simulation run time
  - Model must be verified, sometimes be converted and modified before usage
  - Difficult in Modeling complex transceiver buffers
- MacroModel
  - Fast simulation run time
  - A simply modeling solution for complex IOs ,such as pre-emphasis buffers
  - Macromodel is based on IBIS model

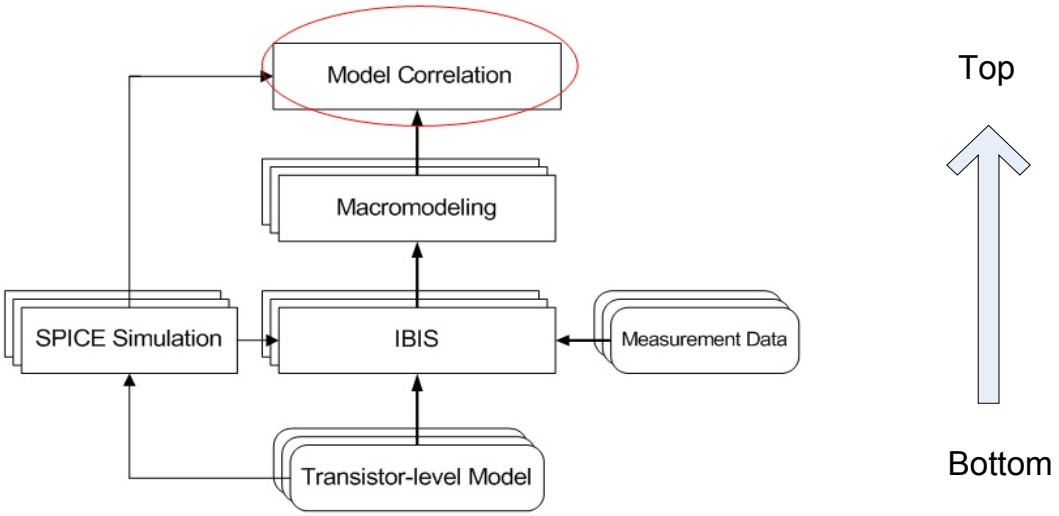
Modeling methodology

- Modeling is quite involved, it covers active devices as well as passive devices, such as package, transmission line, connector, via, and plane etc..
- Not all modeling methods are the same. They have tradeoffs and are suitable for different applications.
- There are behavioral IBIS and structural Spice modeling for active devices. Spice model is appropriate for demanding situations, while IBIS model is often used in system and board level simulation.
- Circuit simulators can run both IBIS and Spice. Different simulators have different characteristics.

Modeling of complex IOs

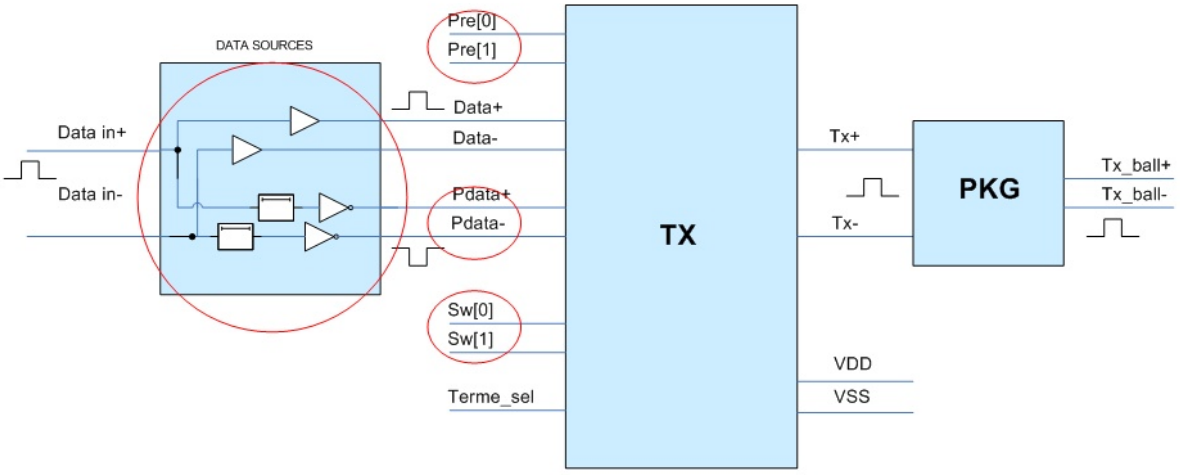
- IBIS Multi-lingual Modeling
  - VHDL-AMS
  - Verilog-AMS
  - Incorporating SPICE Subcircuits
  - Incorporating External Model
  - Incorporating S-Parameter Model
- Macromodeling based on IBIS
  - A simply solution for complex buffers
  - Combining spice subcircuits and behavioral models

Macromodeling and its correlation flow



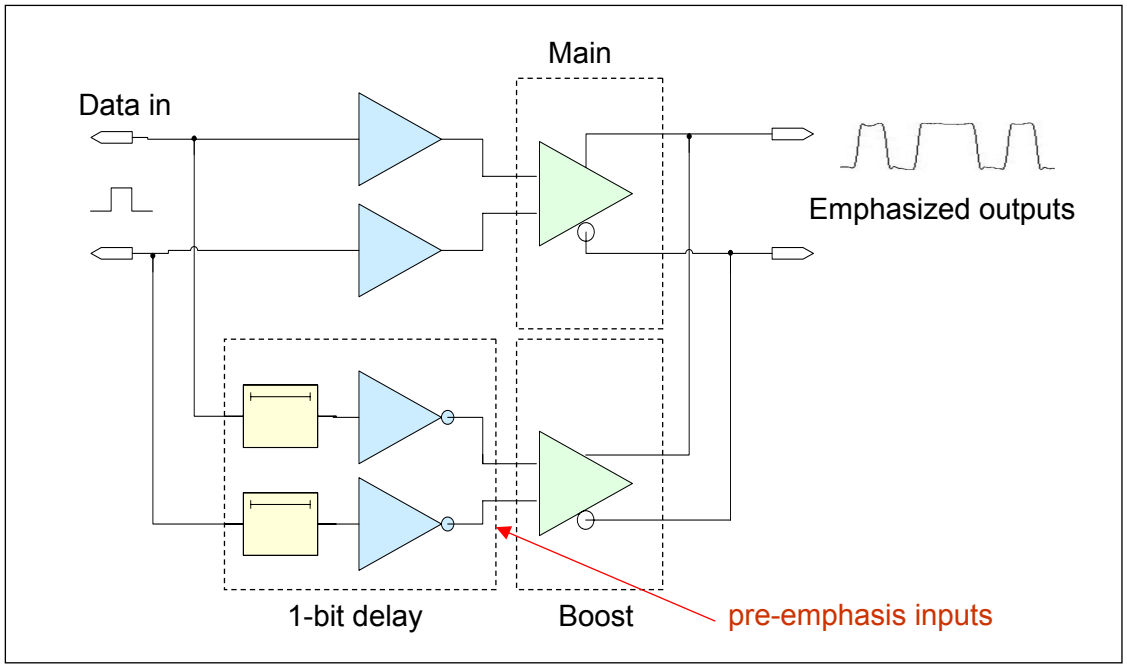
For behavior-level modeling , correlation is necessary.

Macromodeling of SERDES



The structure of transmitter device

Pre-emphasis



Example Macromodel for Pre-emphasis

- Normal IBIS data

```
[Model]        TX_sample
Model_type     Output

C_comp                  0.26pF   0.18pF   0.30pF
[Voltage Range]         1.2V     1.14V    1.26V
|
[Pulldown]
| Voltage      I(typ)        I(min)        I(max)
|
[Pullup]
| Voltage      I(typ)        I(min)        I(max)
|
[Ramp]
|              typ           min           max
dV/dt_r    0.36/0.10n     0.35/0.11n     0.37/98.79p
dV/dt_f    0.33/99.12p    0.33/96.04p    0.33/0.10n
R_load = 5k
```

- Place in macromodel template
  - (Pullup (ReferenceVoltage
  - rt
  - (Pulldown (VICurve
  - (Ramp (dt
  - (C_comp and/or padcap
- Additional data
  - Bitp ----- Unit interval
  - eqdb ----- Pre-emphasis db
  - Scale ----- Vp-p

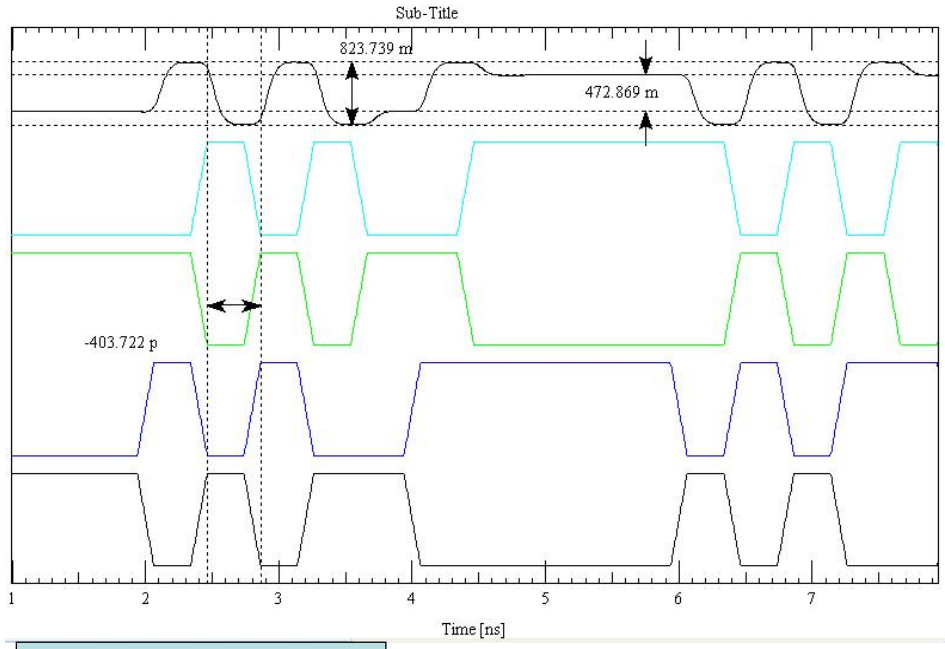
MGH MacroModel templates can be downloaded from

http://www.allegrosi.com

http://www.specctraquest.com

http://register.cadence.com/register.nsf/macromodeling?openform

Simulation of Pre-emphasis using marcormodel



Pre-emphasis output

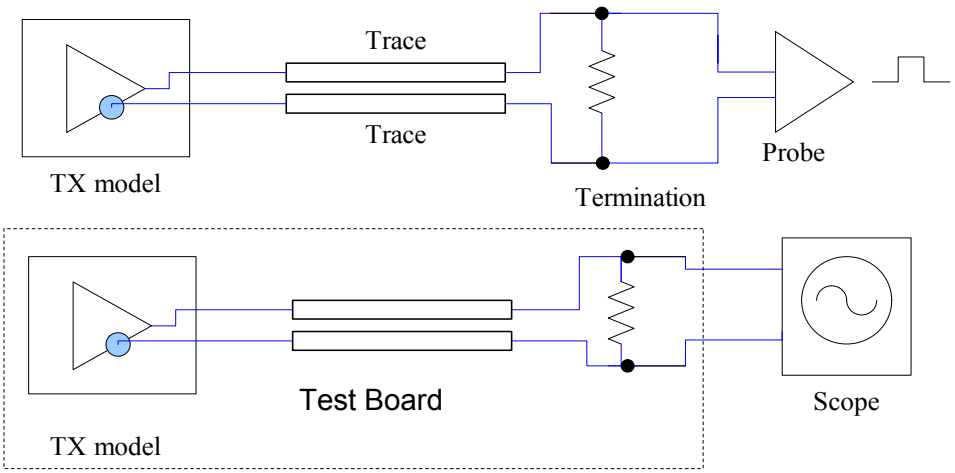
delay_1bit

data in-

data in+

UI=400ps PRBS K28.5

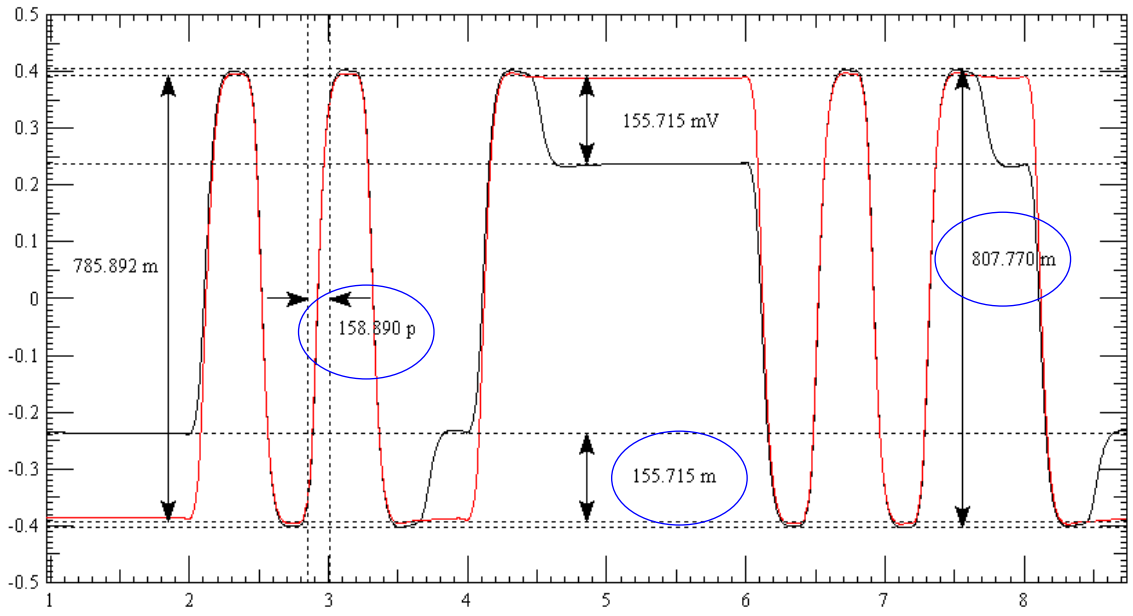
Macromodel Validation setup



Correlations with lab measurements and HSPICE simulations

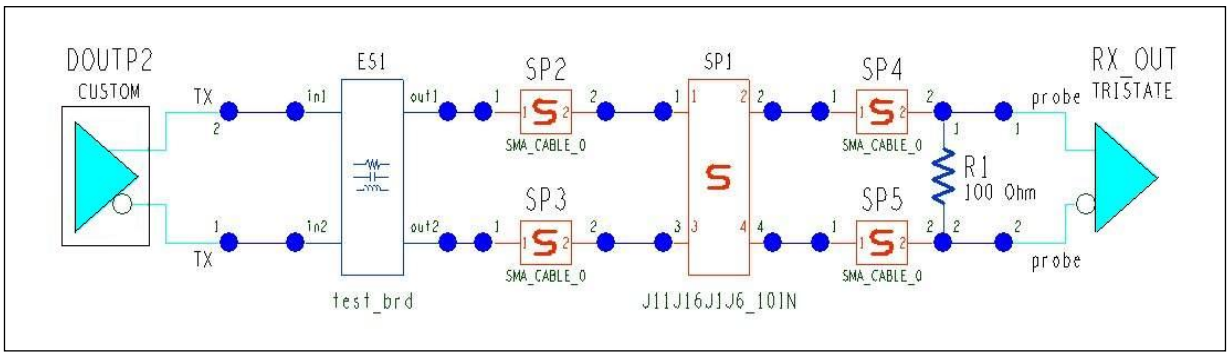
Macromdeling simulation w./wo. pre-emphasis

Red Curve: No Pre-emphasis Black Curve: 40% Pre-emphasis



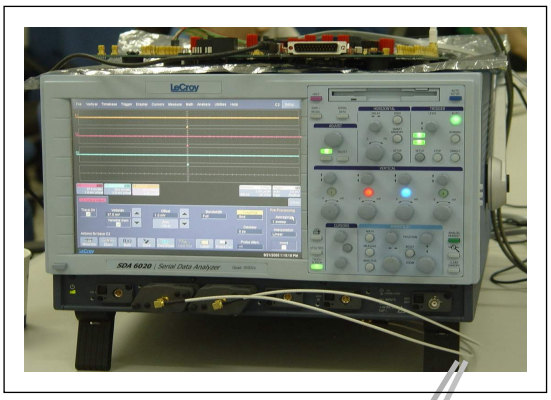
Lab Correlation for Macromodels

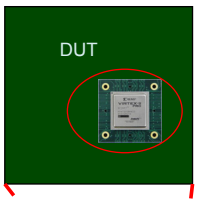
1 Simulation using HSPICE models
2 Simulation using macrmodels
3 Correlate with laboratory measurement

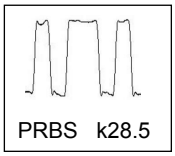


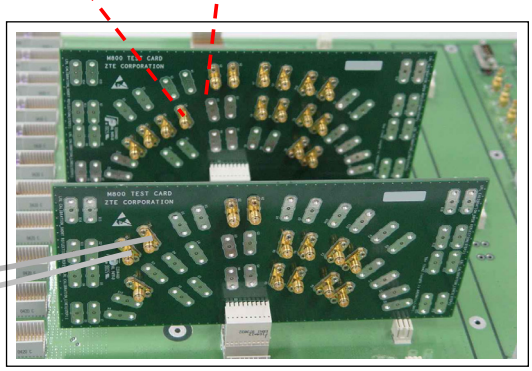
Measurement versus Simulation

Laboratory and measurement setup



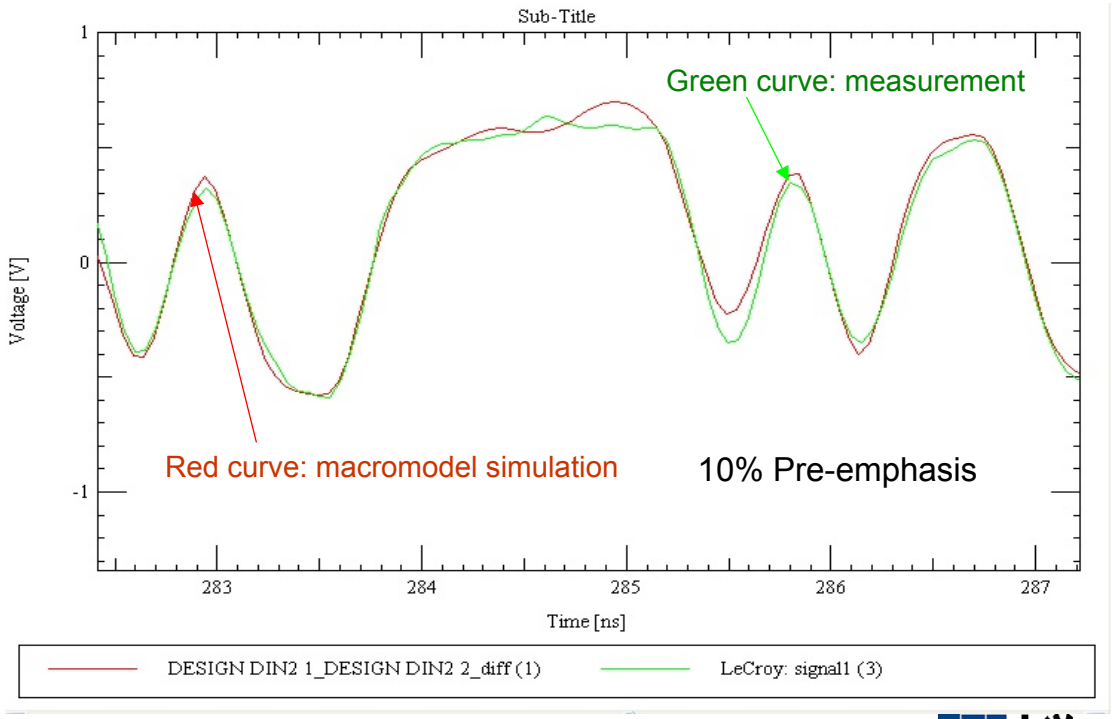




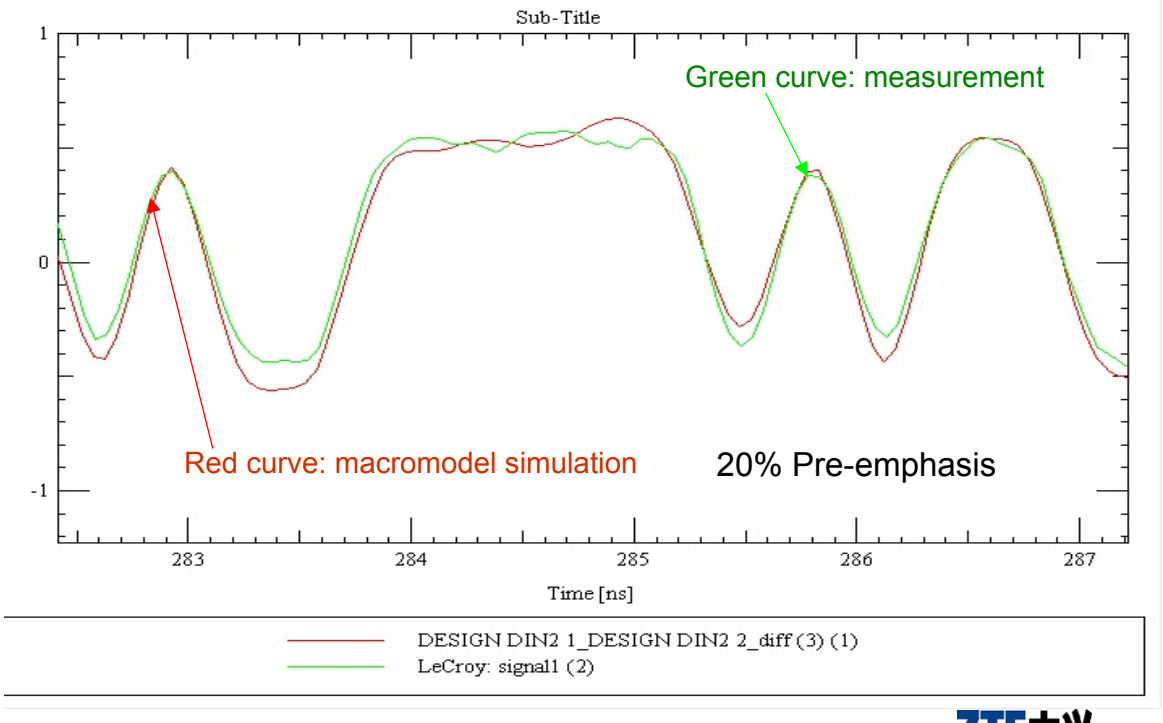


The backplane has 10'' of stripline
The daughter card has 3" of stripline
Data rate is 3.125Gb/s

Lab Correlation for Macromodels

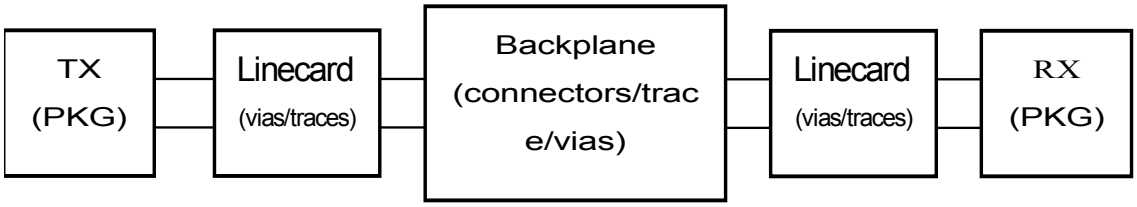


Lab Correlation for Macromodels



Multi-GHz System Interconnect Simulation

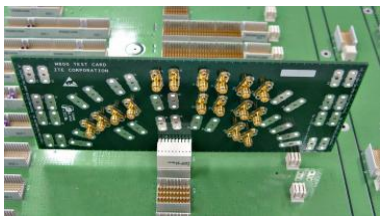
- Multi-GHz System Interconnect Simulation includes:
  - Transceiver Modeling
  - Transceiver Package Modeling
  - Interconnection (Traces, Vias, Connectors) Modeling



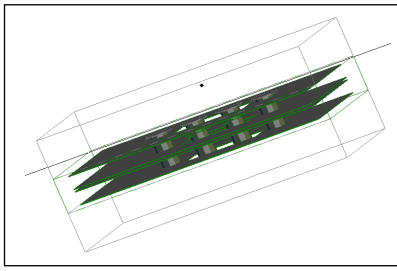
Multi-GHz System Interconnect Simulation

- Extracting models using 2D/3D EM solver
- Correlation based on VNA and TDR/TDT measurements
- SI/PI/EMC Simulations
- Eye diagram analysis and design margin budget
- Optimization

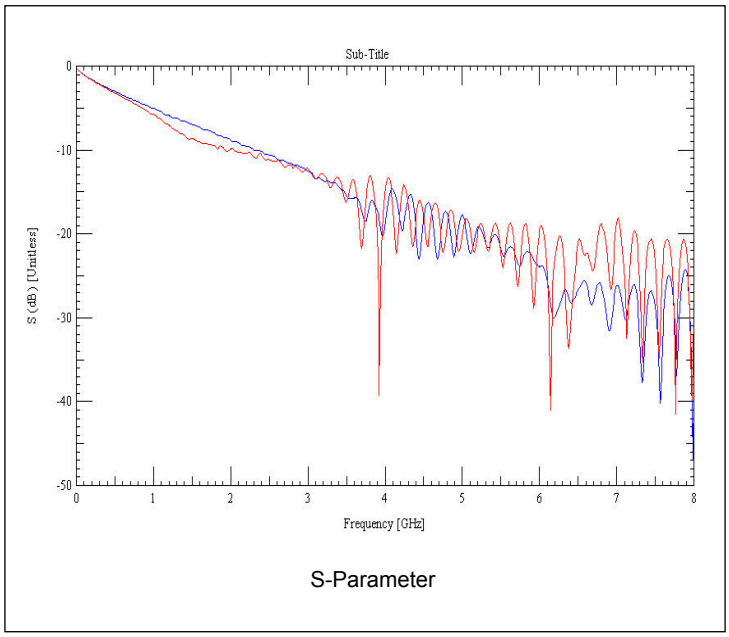
Measurement modeling



Measurement setup



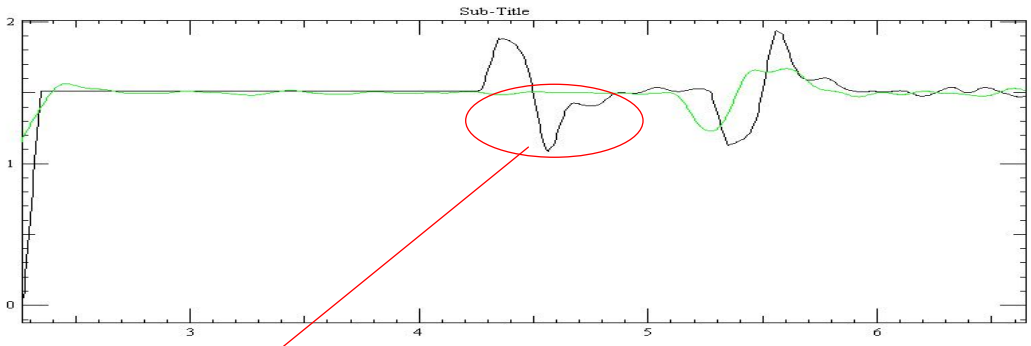
3D EM Solver Modeling

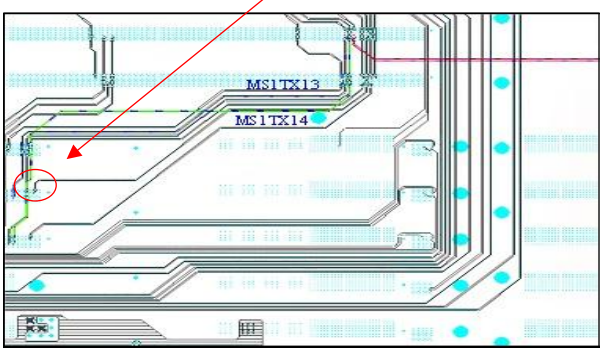


S-Parameter

S21 data comparison between VNA measurement and Simulation

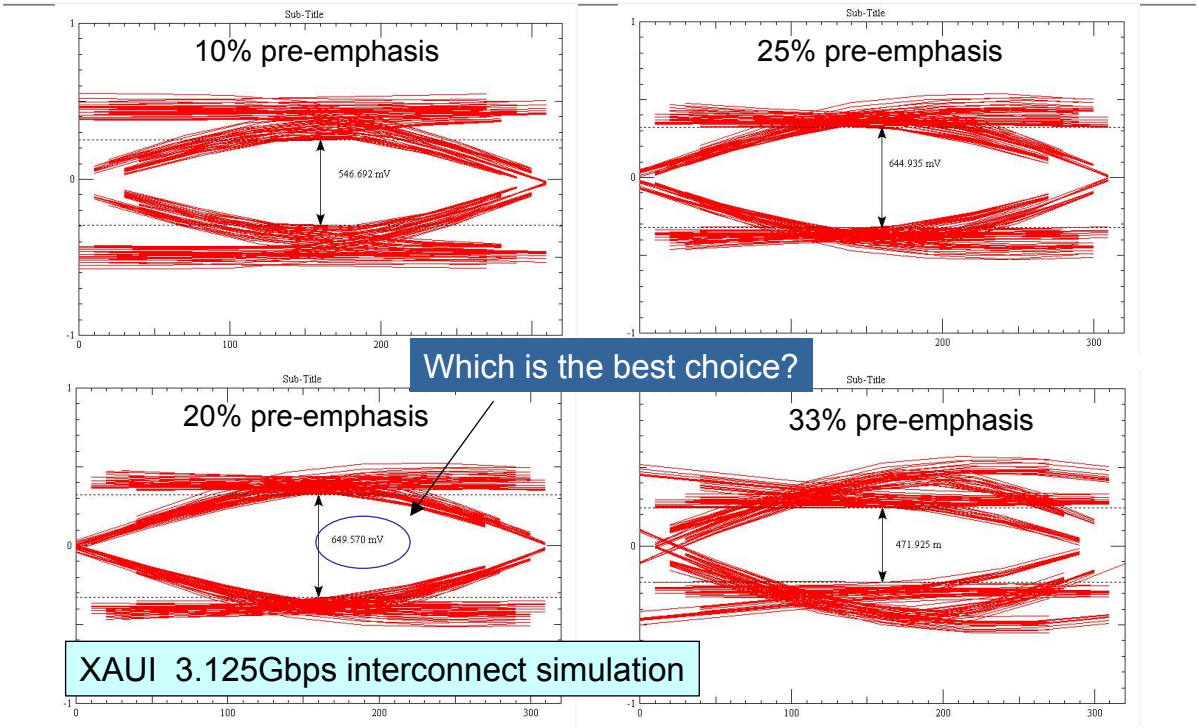
TDR optimization



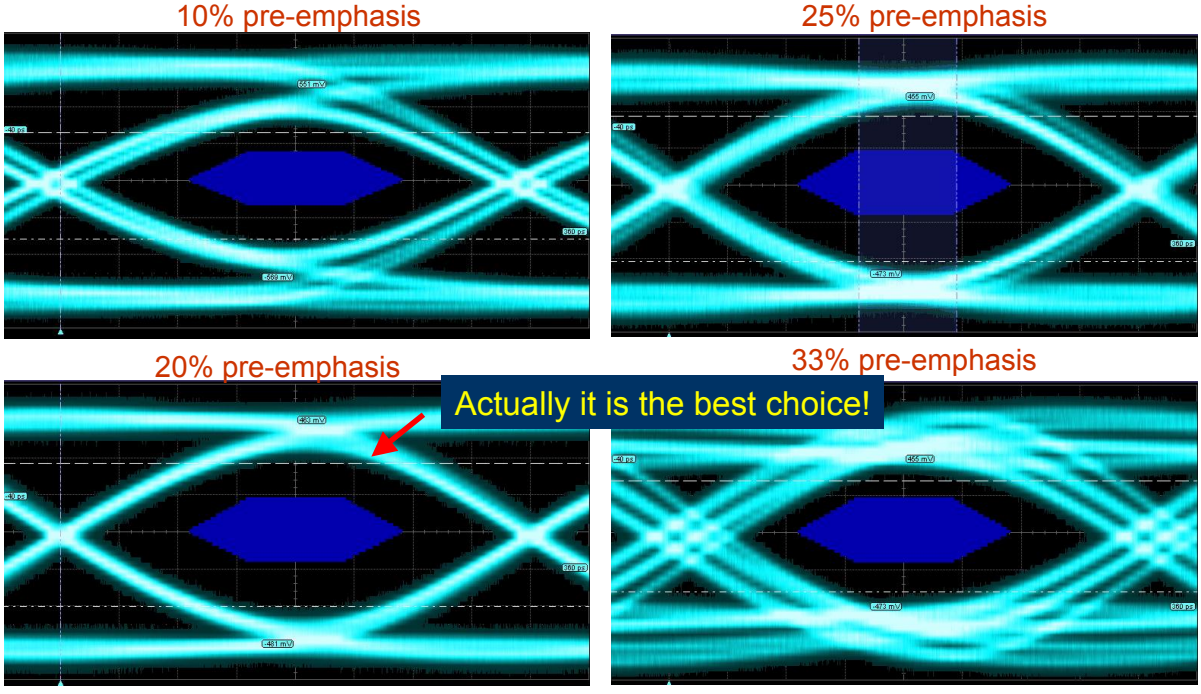


Impedance analysis of multi-GHz Interconnection is very important.

Macromodel application



Correlation



Conclusions

- Choose an appropriate modeling method is critical for simulation. Otherwise simulation may not be accurate enough or too complex and time consuming.
- Macromodel is an efficient solution for complex IO modeling, provided it be validated before usage.
- MacroModel enables much shorter simulation time than transistor-Level spice model. They can be used for system design and post-layout analysis.
- MacroModeling is appropriate for what-if analysis due to its relative short run time and sufficient accuracy.
- For multi-GHz Interconnection optimization, active device modeling using marcomodels, PCB modeling using EM solver, and correlation based on lab measurements have been proved to be very effective.

IBIS Models for DDR2 Analysis

Asian IBIS Summit 2005

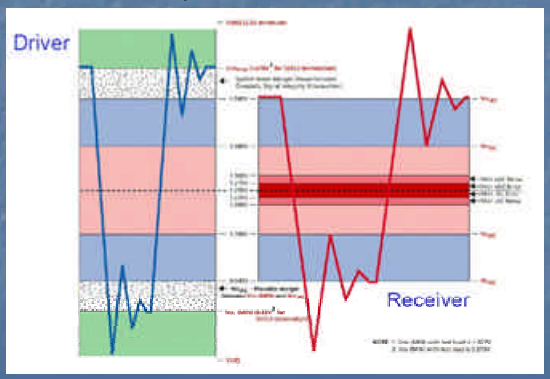
Barry Katz, President and CTO, SiSoft

DDR Overview: *Theory of Operation*

- Data captured on both clock edges
- Data (DQ) driven source synchronously with strobe (DQS)
- Proper source sync operation requires two conditions:
  - DQS positioned to meet data Setup/Hold requirements
  - Fixed relationship between CK and DQS must be maintained
- DDR1 Clock (CK) range from 100MHz to 200MHz
  - DQ 200Mbs to 400Mbs
- DDR2 Clock (CK) range from 200MHz to 400MHz
  - DQ 400Mbs to 800Mbs

DDR Overview: *Theory of Operation*

- DDR1: 2.5V SSTL
- DDR2: 1.8V SSTL
- SSTL introduces concept of AC and DC levels



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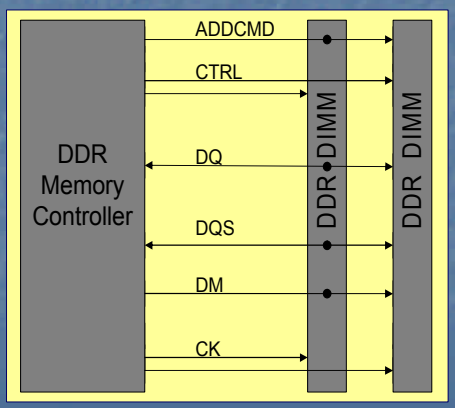
DDR System Configurations

- DDR1: One to four memory modules
- DDR2: One or Two memory modules
- Memory Modules
  - Registered and Unbuffered
  - 4 to 18 memory device



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DDR2 Enhancements

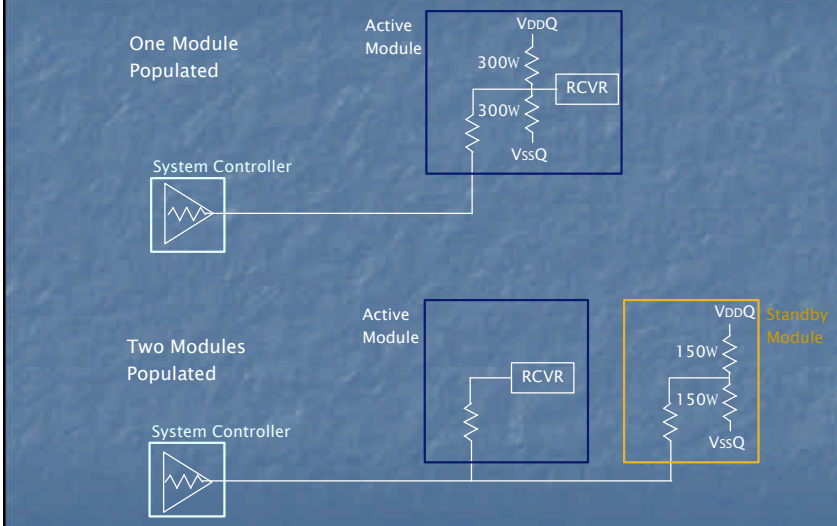
Moving beyond DDR1

- Technology
  - FBGA Package
  - Reduced Supply Voltage (1.8V)
  - Optional Differential DQS
  - Improved DIMM routing Topologies
  - Improved Load Balancing
  - **On-Die Termination (ODT)**
    - **Increases number of combinations to simulate**
  - **Slew-Rate Derating**
    - **Modifies Setup/Hold requirements**

On-Die Termination

- DQ, DM, DQS signals only
- Memory controller defined
  - Transfer by transfer basis
  - Dependent on loading configuration
- Multiple values: 50, 75,150, and “off”
- Reduces PCB component count
- Simplifies system implementation
- Increases analysis complexity

Data Write ODT Configurations



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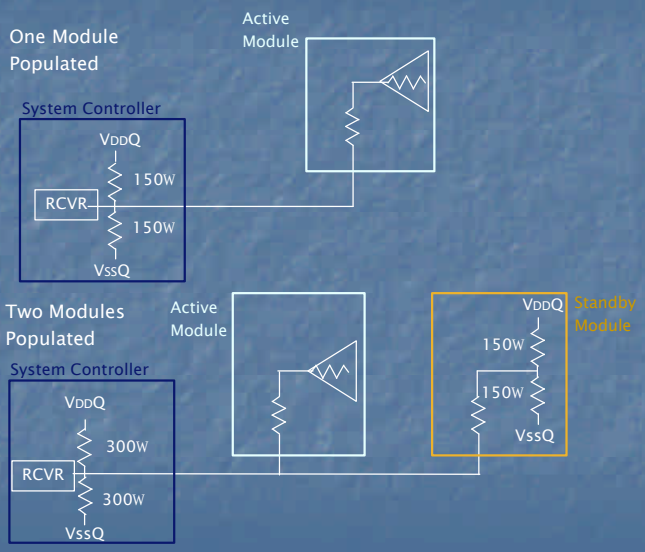
Data Read Configurations



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DDR2 I/O Buffer Modeling Challenges

Spice vs. IBIS

- SPICE models
  - Accurate, allow for PVT variation, over-clockable
  - Slow simulation time
- IBIS models
  - Can closely match SPICE models for accuracy
  - Higher simulation performance
  - Multiple simulator support, readily available

DDR2 I/O Buffer Modeling Challenges

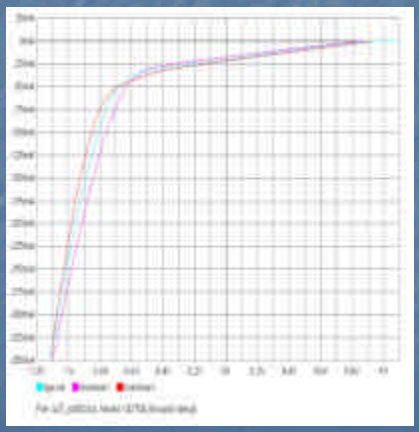
ODT Modeling in IBIS

- Three options for ODT modeling
  - 6 separate I-V curves
    - Normal [Pullup], [Pulldown], [POWER Clamp] and [GND Clamp] tables
    - ODT I-V curves included as [Submodel] tables
    - [Submodel] usage creates portability issues
  - Separate receive ODT-enabled model
    - Requires switching in of separate model
    - Increases complexity of simulation
    - Separate simulations for every case
  - 4 I-V curve model with ODT enabled in receive mode
    - Works well, but makes IBIS [Pullup] and [Pulldown] non-monotonic
      - This is OK because sum of [Pullup] and [Pulldown] with Clamp curves is monotonic

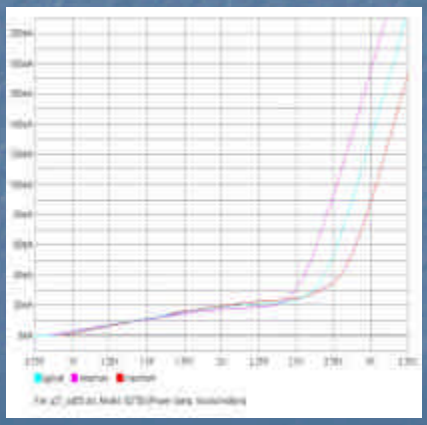
DDR2 I/O Buffer Modeling Challenges

ODT Modeling in IBIS – Thevenin ODT approach

50 O ODT model [GND Clamp]



50 O ODT model [POWER Clamp]



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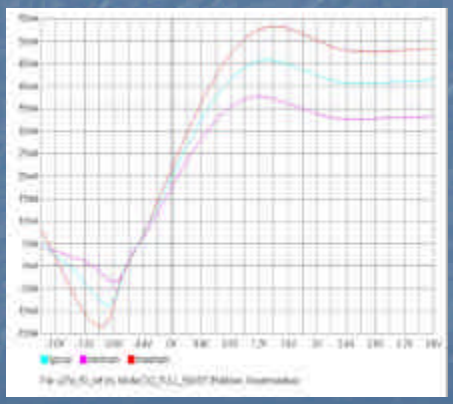
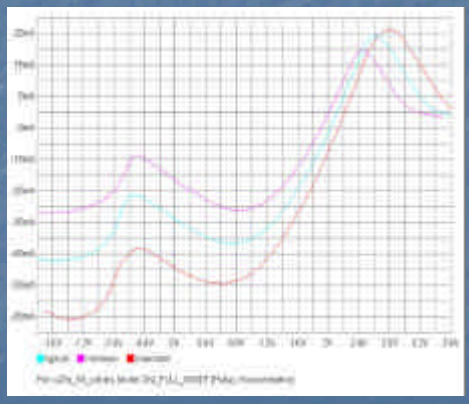
DDR2 I/O Buffer Modeling Challenges

ODT modeling in IBIS

[Pulldown] with 50 O ODT characteristics subtracted



[Pullup] with 50 O ODT characteristics subtracted



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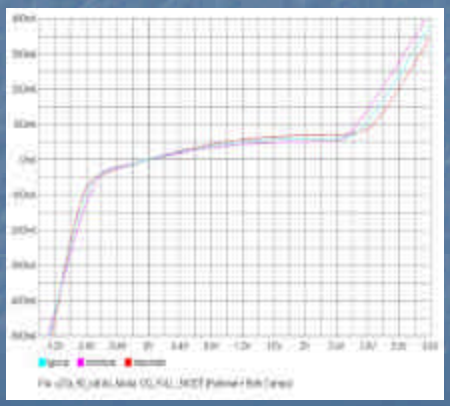
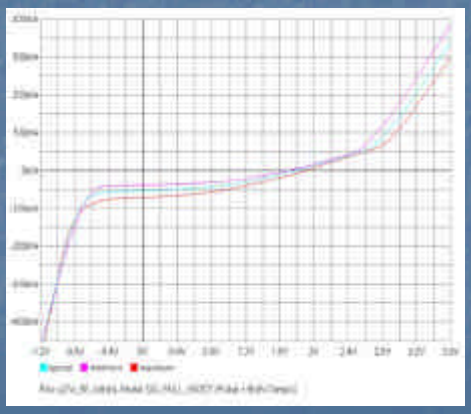
DDR2 I/O Buffer Modeling Challenges

ODT modeling in IBIS

[Pulldown] combined with [* Clamp] characteristics



[Pullup] combined with [* Clamp] characteristics



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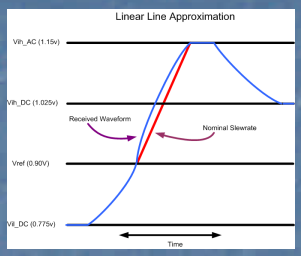
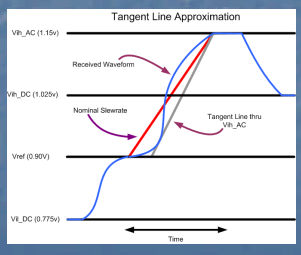
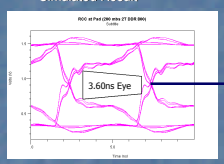
Future Considerations for IBIS

Slew-Rate De-Rating Tables



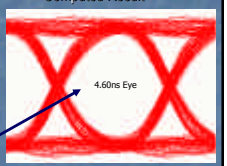


- EYE At Device PAD Simulated Result

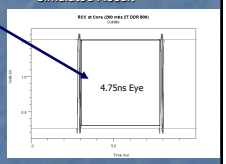


Receiver

- Virtual Eye at Receiver Computed Result



- Eye at Receiver Output Simulated Result



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Thank You!

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Practical Measurement vs. Simulation Correlation with DDR2 667 Interface

Kazuyoshi Shoji
Hitachi ULSI Systems Co., Ltd.

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People say :
IBIS model is NOT accurate.

Is that really TRUE?

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People say :
HSPICE model is essential for design.

Is that really TRUE?

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Let’s see what’s happening
in the real world and make
wise decisions!!

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Experiments

Step1

For a given target system, prepare following;

1. Measurement waveforms
2. Simulated waveforms using IBIS model
3. Simulated waveforms using HSPICE model

Step2

Verify accuracy with figure of merit method
(100% is perfect match)

Step3

Compare simulation time

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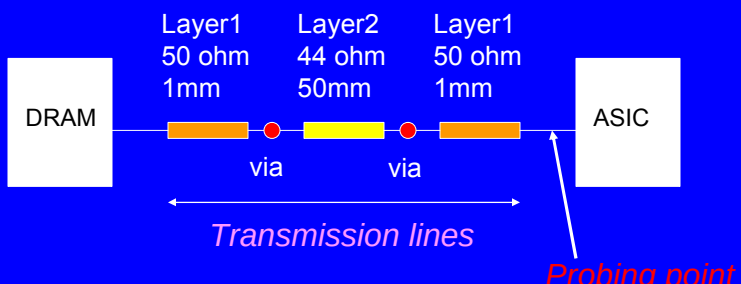
Target System

Digital consumer system
Point-to-point application
Memory interface with 333MHz (DDR2 667)



Parameters extracted from real design using Cadence Allegro

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Simulation condition

Models

Memory device:
DDR2-667 333MHz DRAM
IBIS model created by ***HITACHI ULSI systems***
Receiver:
ASIC Model
provided from system vendor

Tool

Synopsys HSPICE 2005.3 SP1

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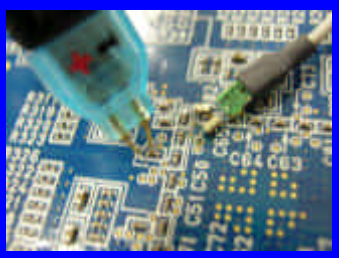
Measurement equipments

Oscilloscope:
Agilent technologies
Infiniium54855A 6GHz 20GSa/sec
InfiniiMax1134 probe
Single-End Solder (E2679A)



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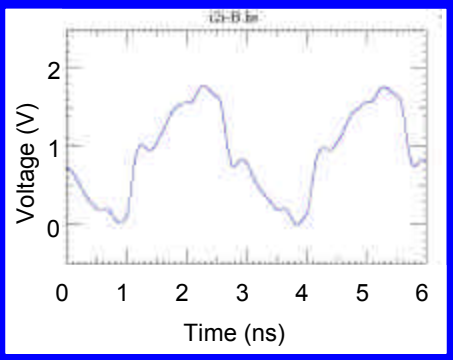
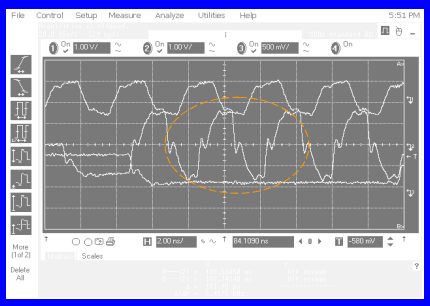
IBIS vs. Measurement



DRAM IBIS model



Measurement waveforms

Good match with Figure Of Merit of 96%

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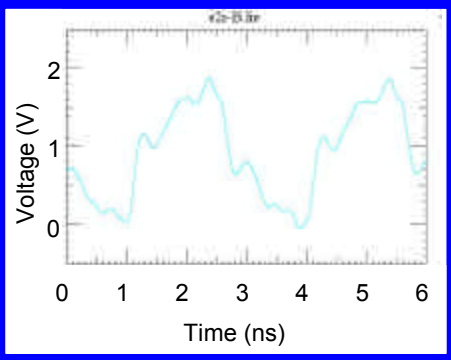
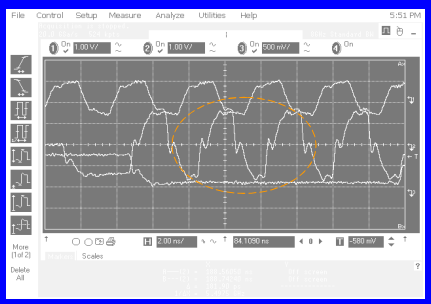
HSPICE vs. Measurement



DRAM HSPICE model



Measurement waveforms

Close match with FOM of 96%

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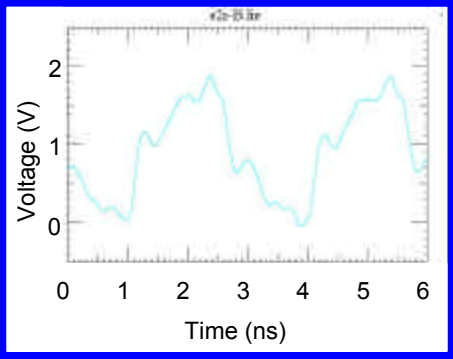
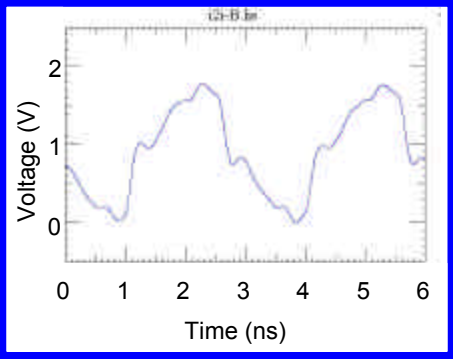
IBIS vs. HSPICE



DRAM HSPICE model



DRAM IBIS model

Nearly equal with FOM of 98%

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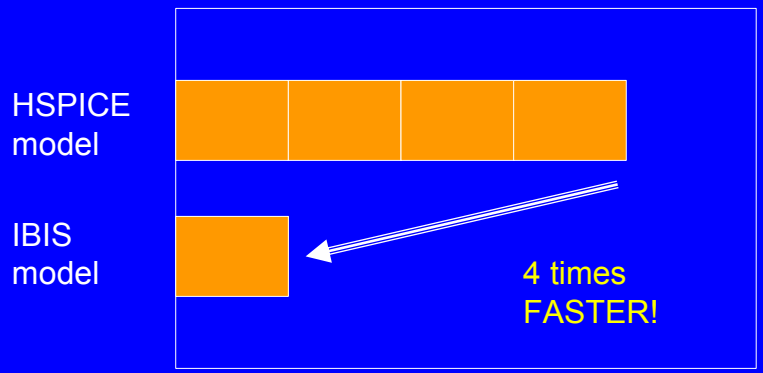
Simulation time comparison



Simulation CPU time

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Summary

1) Simulation results of DDR2 667 system shows IBIS & HSPICE DDR2 memory model simulation Correlation with measurement within FOM of 96%

2) IBIS model simulation faster than HSPICE model by four times.

3) Using IBIS model simulation is fairly accurate and fast. Good choice for practical purpose.

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Thank you!

Asian IBIS Summit Meeting
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Improving IBIS ECL Algorithms
改进 IBIS ECL 算法

Bob Ross 鲍伯 若什

Asian IBIS Summit 亚洲 IBIS 技术研讨会

Shenzhen, CHINA 中国 深圳

December 6, 2005 2005年12月6日

TERASPEED CONSULTING GROUP

Content
内容

- 2-Waveform Algorithm Overview
  2- 信号波形算法概要
- ECL 2-Waveform Algorithm
  ECL 2- 信号波形算法

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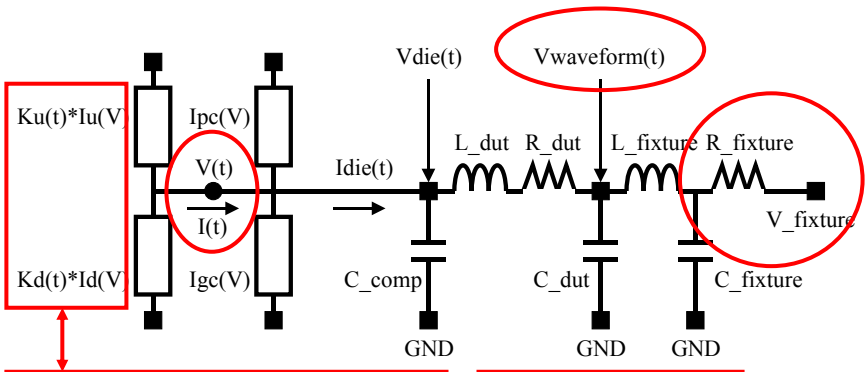
2-Waveform K(t) Algorithm
2- 信号波形 K(t) 算法



$Kd(t)Id(V_1) + Ku(t)Iu(V_1) = -I_1(t)$
$Kd(t)Id(V_2) + Ku(t)Iu(V_2) = -I_2(t)$

Recommended: 推荐

50 Ω to Vcc

50 Ω to Gnd

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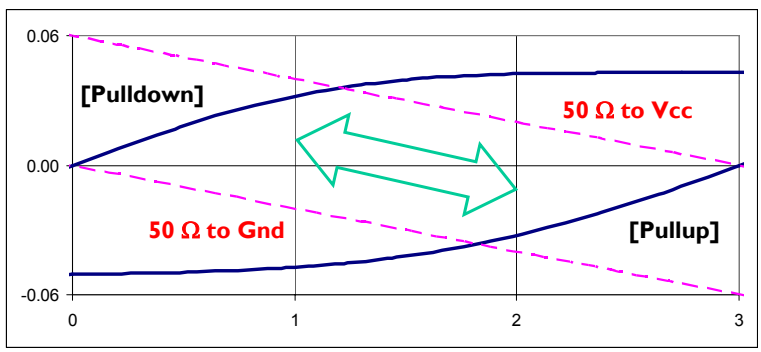
Example I-V Data
例子 I-V 数据



$Kd(t)Id(V_1) + Ku(t)Iu(V_1) = -I_1(t)$
$Kd(t)Id(V_2) + Ku(t)Iu(V_2) = -I_2(t)$

K(t) solution exists for fixture V

K(t) 算法工作

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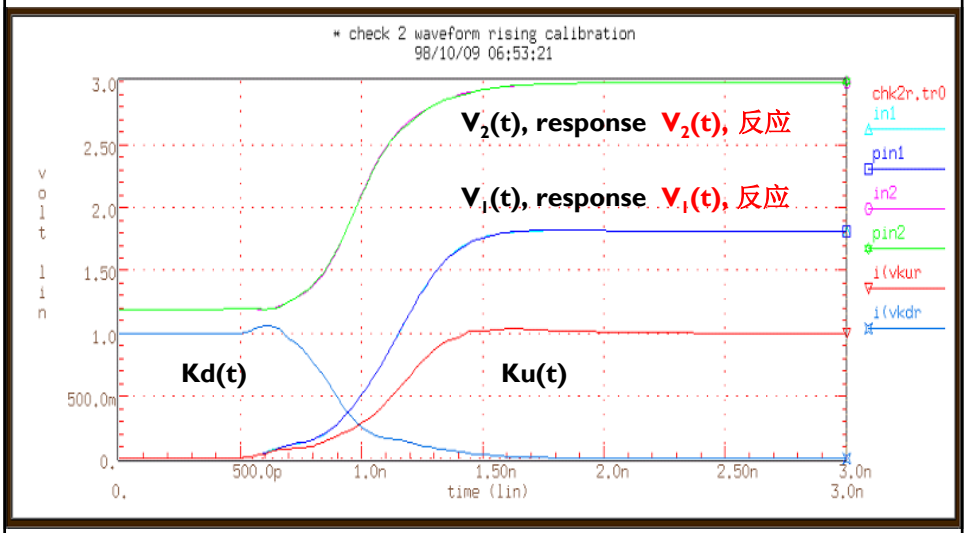
Example V-T, K(t)
例子 V-T, K(t)



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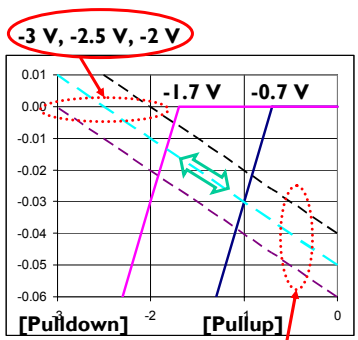
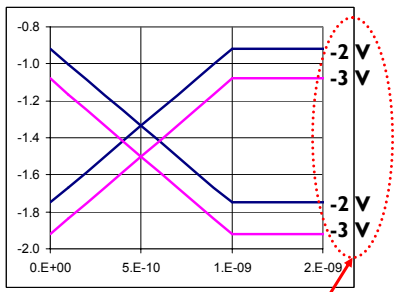
ECL 2-Waveform Data
ECL 2- 信号波形数据





ECL I-V Data

50 Ω loads

ECL V-T Data

R_fixure = 50 Ω

V_fixture = -2 V, -3 V

Example 例子

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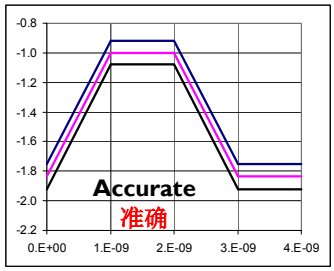
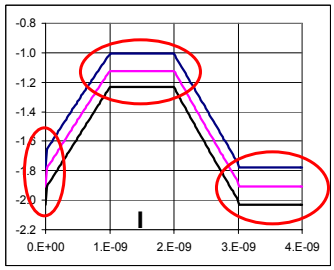
0-1-0 Calculation Errors

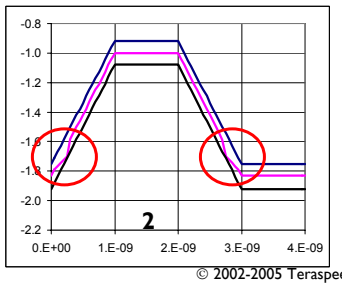
0-1-0 计算错误

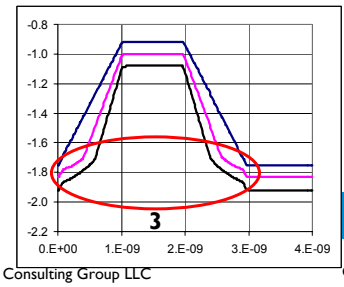




Wrong Volts
错误电压

Wrong Shape
错误波形





Wrong Shape
错误波形

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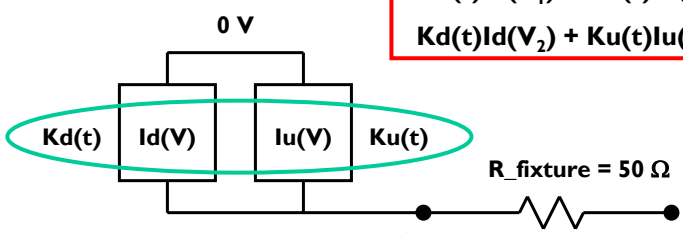
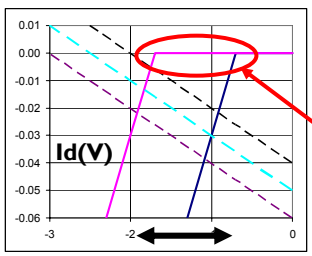
ECL K(t) Solution Fails

ECL K(t) 算法失败

$Kd(t)Id(V_1) + Ku(t)Iu(V_1) = I_1(t)$

$Kd(t)Id(V_2) + Ku(t)Iu(V_2) = I_2(t)$





$V_1(t), I_1(t)$ V_fixture = -2 V

$V_2(t), I_2(t)$ V_fixture = -3 V

K(t) solution fails for V values if Id(V) = 0

K(t) 算法失败

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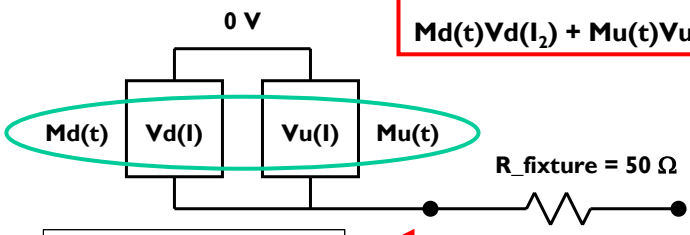
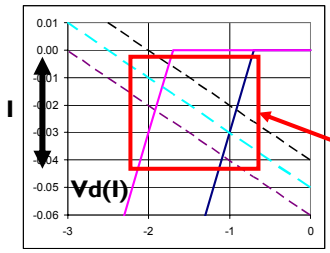
ECL M(t) Solution Exists
ECL M(t) 算法工作

$Md(t)Vd(I_1) + Mu(t)Vu(I_1) = V_1(t)$

$Md(t)Vd(I_2) + Mu(t)Vu(I_2) = V_2(t)$





$V_1(t), I_1(t)$ V_fixture = -2 V

$V_2(t), I_2(t)$ V_fixture = -3 V

M(t) solution exists for I values of Vd(I)

M(t) 算法工作

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ECL Improvement
ECL 改善

- Process 过程
  - Transform [Pullup], [Pulldown] data
    变换 [Pullup], [Pulldown] 数据
    - From I-V 从 I-V
    - To V-I data 对 V-I 数据
  - Solve for Mu(t), Md(t)
    发现解法为 Mu(t), Md(t)
- Advantages 好处
  - Supports 2-waveform analysis
    支持 2- 信号波形分析
  - Avoids adjustments
    避免调整

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