ASIAN IBIS SUMMIT INFORMATION
亚洲 IBIS 技术研讨会

Time/Date: 8:00 - 17:30, Tuesday, December 6, 2005
2005 年 12 月 6 日，星期二，8:00 - 17:30

Location:

Crowne Plaza Hotel Shenzhen	深圳威尼斯大酒店
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http://www.ichotelsgroup.com/h/d/cp/1/en/hd/SZXNS

Room: Crowne Plaza Ballroom #2, First Floor
1 楼威尼斯 2 号宴会厅

Registration: FREE, 免费

Sponsors: Huawei Technologies (Primary)
Cadence Design Systems, Mentor Graphics Corporation,
Signal Integrity Software (SiSoft) and Sigrity

IBIS SUMMIT MEETING AGENDA
IBIS 技术研讨会日程表

8:15 REFRESHMENTS & SIGN IN 签到，点心
- Vendor Tables Open

9:00 INTRODUCTIONS AND PROGRAM OVERVIEW 与会者和会议介绍
- Welcome, Jiang, XiangZhong, (Huawei Technologies, China)
- Welcome to Summit, Mirmak, Michael (Intel Corporation, USA)
- Welcoming Comments, Invited Chinese Leader/Speaker (China)

9:30 IBIS AND BEHAVIORAL MODELING
- Mirmak, Michael (Intel Corporation, USA)

9:45 FIBERHOME TELECOMMUNICATIONS TECHNOLOGY EXPERIENCES WITH IBIS MODELS
- Zheng, Qi (Fiberhome Telecommunications Technology, China)

10:15 BREAK (Refreshments) 休息，点心

10:30 SIMULATION WITH IBIS IN TIGHT TIMING BUDGET SYSTEMS
- Sui, ShiJu, (ZTE Corporation, China)

11:00 THREE FACETS OF IBIS: INTERFACE, BEHAVIOR AND MEASUREMENT
- Dodd, Ian* and Li, Henry** (Mentor Graphics Corporation, *USA and **China)

11:30 JEITA EDA - WG ACTIVITY AND STUDY OF INTERCONNECT MODEL
- Watanabe, Takeshi (NEC Electronics Corporation, Japan)

12:00 FREE BUFFET LUNCH (Hosted by Sponsors) 自助午餐
- Vendor Tables

12:00 - 12:45 Press Conference for IBIS Officers and Sponsor 新闻发布会

13:30 IBIS AND POWER DELIVERY SYSTEMS
- Jiang, XiangZhong, Li, JinJun, and Zhang, ShengLi (Huawei Technologies, China)

14:00 POWER DELIVERY SYSTEM, SIGNAL RETURN PATH AND SSO ANALYSIS GUIDELINES
- Chen, Raymond Y. and Chitwood, Sam (Sigrity, USA)

14:30 SPLITTING THE C_COMP FOR POWER INTEGRITY SIMULATIONS
- Yang, Zhiping (Apple Computer, USA)

15:00 USING IBIS FOR SI ANALYSIS
- Wang, Lance* and Zhong, ZhangMin** (Cadence Design Systems, *USA and **China)

15:30 BREAK (Refreshments) 休息，点心

15:45 MACRO MODEL AND MULTI-GHZ SYSTEM SIMULATION
- Zhu, ShunLin (ZTE Corporation, China)

16:15 IBIS MODELS FOR DDR2 ANALYSIS
- Katz, Barry (Signal Integrity Software (SiSoft), USA)

16:40 PRACTICAL MEASUREMENT VS. SIMULATION CORRELATION WITH DDR2 667 INTERFACE
- Shoji, Kazuyoshi (Hitachi ULSI Systems Co., Japan)

17:05 IMPROVING IBIS ECL ALGORITHMS
- Ross, Bob (Teraspeed Consulting Group, USA)

17:20 CONCLUDING ITEMS 会议闭幕

17:30 END OF IBIS SUMMIT MEETING 结束
- Final Vendor Tables and Teardown