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Standard Power Integrity Model (SPIM) and Unified PI Target (UPIT)

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Presenter

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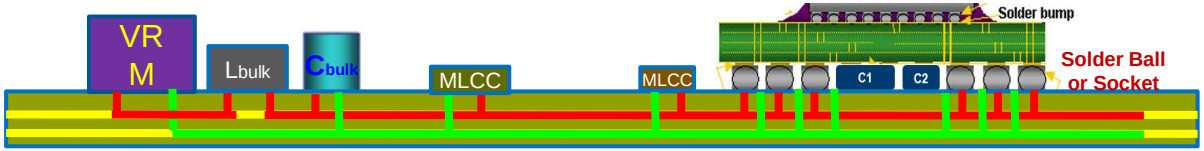
Kinger Cai has been driving I+I strategy for Notebook platforms, and strategic PI design tool evolution in Client Computing Group. Kinger was awarded Ph. D by Shanghai Jiao Tong University in 2001, and MBA degree by W.P. Carey business school in 2008. Kinger works in signal & power integrity domains for 20+ years. Kinger published 30+ papers and holds 7 granted patents.

Agenda

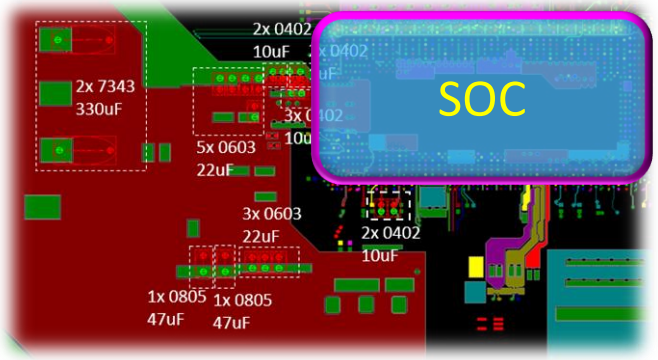
- Industry Platform PI Design Challenges
- Platform PI design Architecture Standardization
  - FastPI – Platform PI design Framework
  - SPIM – Standard Power Integrity Model
  - UPIT- Unified PI design Target
- SPIM with UPIT in FastPI Status Update
- IBIS BIRD Draft Example
- Call to Actions

Platform PI design: Beyond Conventional Methodology

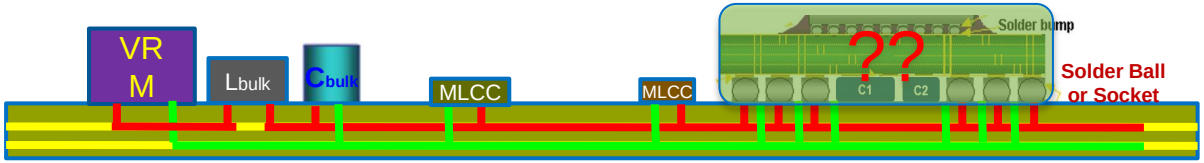


- More flexibility, besides copy exactly from reference design with platform design guideline
- Effective platform PDN optimization, more than what-if simulation
- Efficient platform PI design review and sign-off process

	8L-T3-DS (SD) BOM	
	Primary (TSC)	Secondary (BSC)
VCCin	2x 7343-330uF	4x 0402 1uF
	3x 0805-47uF	
	10x 0603-22uF	
	2x 0402-10uF	
VCCin_Aux	2x 7343-220uF	12x0402 -10uF
	13x0402-10uF	
	2x0603 -22uF	
VDDQ		6x0402-1uF
	2x0603-22uF	2x0402-10uF
	1x0603 (PH)	3x0402 (PH)

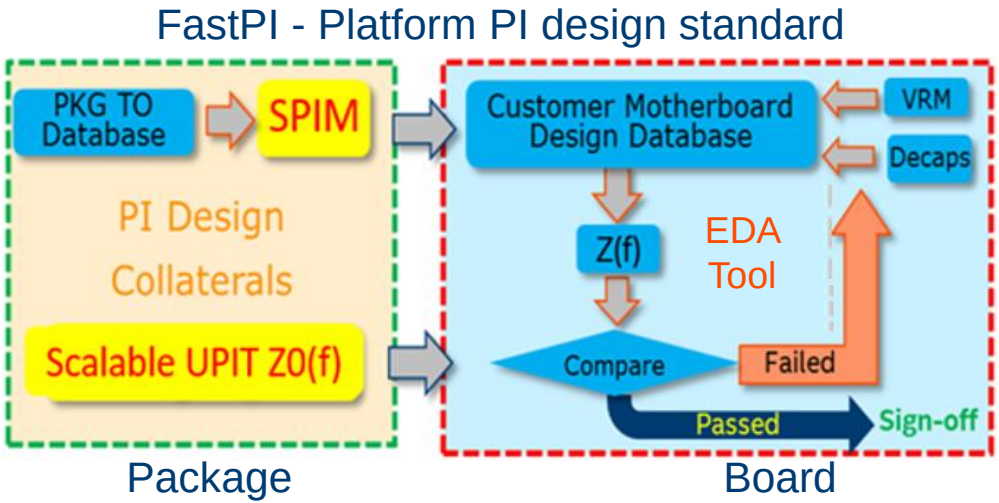


Platform PI design: Collateral, Architecture and Tools



- PI design collateral: Chip vendors to platforms designers
  - ✓ Minimal and standardized
  - ✓ Sufficient, while IP protected
  - ✓ Flexibility, while accuracy guaranteed
- PI design Architecture, Framework and Tool
  - ✓ Standard architecture
  - ✓ Flexible framework
  - ✓ Efficient tool

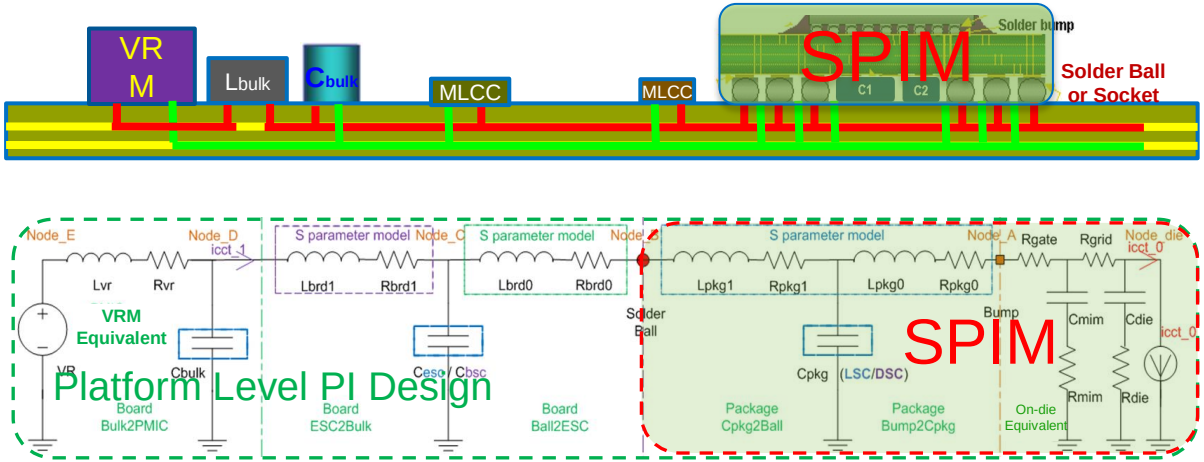
Platform PI design: FastPI with SPIM and UPIT



- **SPIM:** Standardized PI Model, for each power rail in SoC/PKG, to customers
- **UPIT:** Unified PI design Target, an impedance target for each power rail
- **FastPI:** Platform PI design standard, to integrate with industry leading EDA

FastPI supports chip suppliers, EDA vendors and platform designers, with SPIM and UPIT.

Platform PI Design: SPIM- Standard Power Integrity Model



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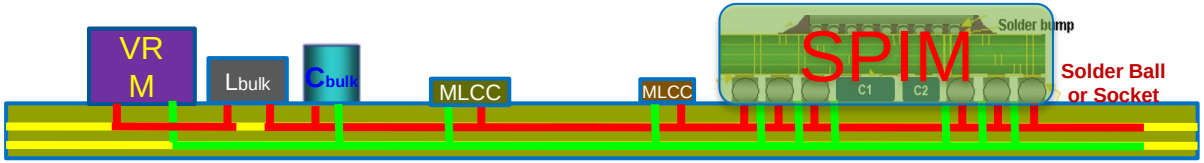
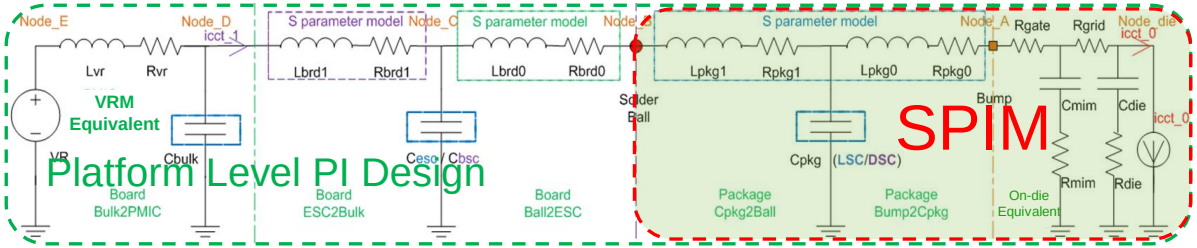
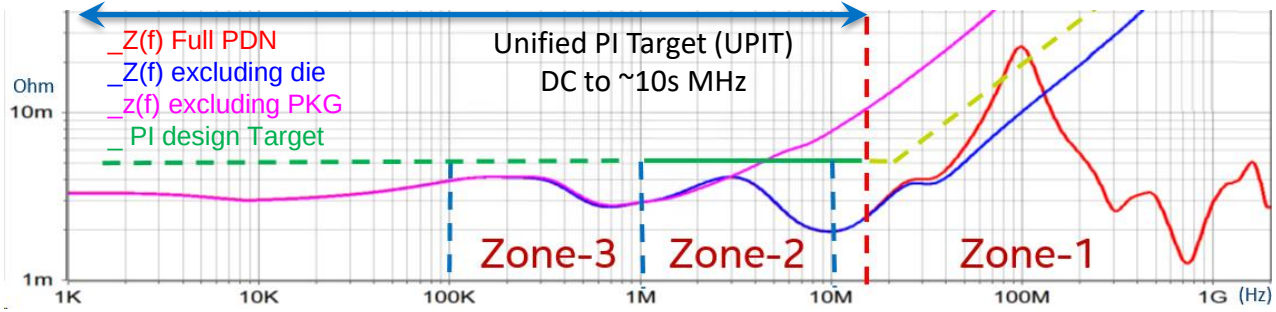
Platform PI Design: SPIM with UPIT (Unified PI Target)

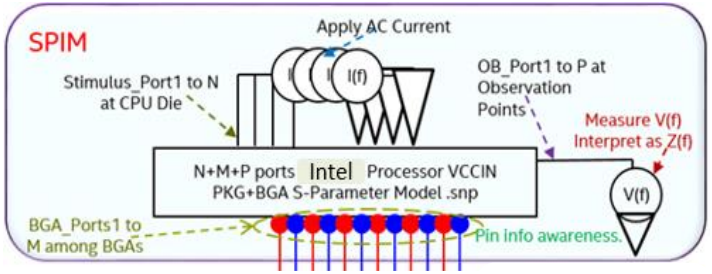


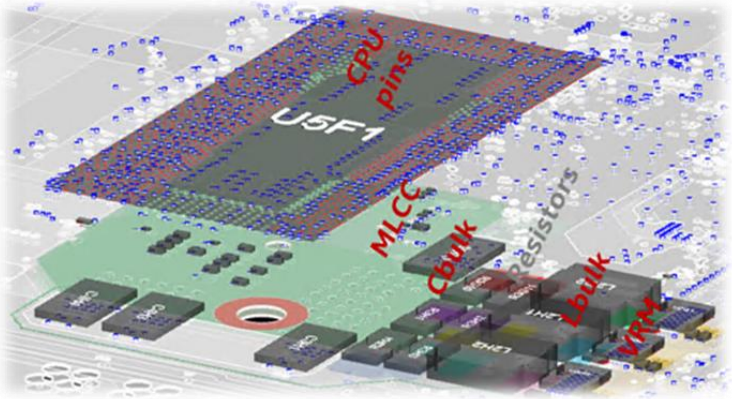




SPIM- Standardized Power Integrity Model

- Standardized PI model
  - S parameter, BGA/pin to bump, and Caps
  - Weighted/normalized AC source
  - Impedance target, at observation port
  - Pin(/BGA) awareness
- Usage model
  - Directly merged as a virtual PKG database, with physical BRD database
  - Backwards compatible to SPICE simulator
  - IP information protection
- Development
  - Promote as industry standard
  - Adopted by major EDA tools
  - Scalable UPIT included

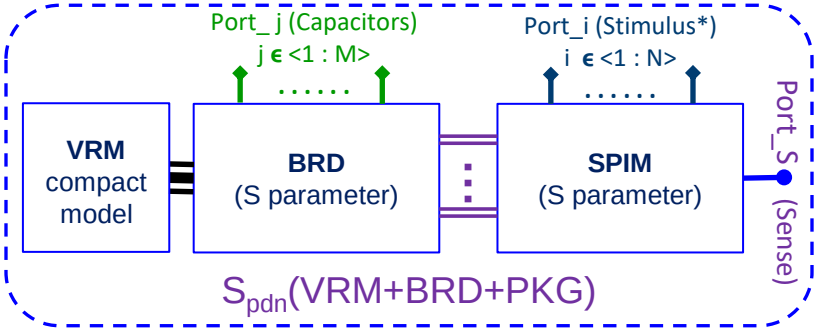




SPIM for platform PI design, while IBIS for platform SI design.

FastPI PI Design Target Definition

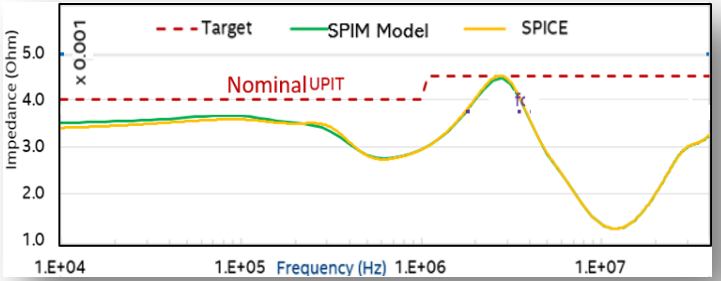
- Impedance at Sense Port_S
  - $[S_{pdn}] \rightarrow [Z_{pdn}]$, in FastPI
  - $[V] = [Z_{pdn}][I]$
  - $[V]=[v_1, v_2, \ldots, v_N, v_S]^T$
  - $[I]=[w_1, w_2, \ldots, w_N, 0]^T$
  - $\sum_{i=1}^{i=N} w_i = 1$, weighted normalization
  - $Z_S=V_S= \sum_{i=1}^{i=N+1}(Z_{pdn(N+1),i} * w_i)$
  - $Z_S= \sum_{i=1}^{i=N}(Z_{pdn(N+1),i} * w_i)$

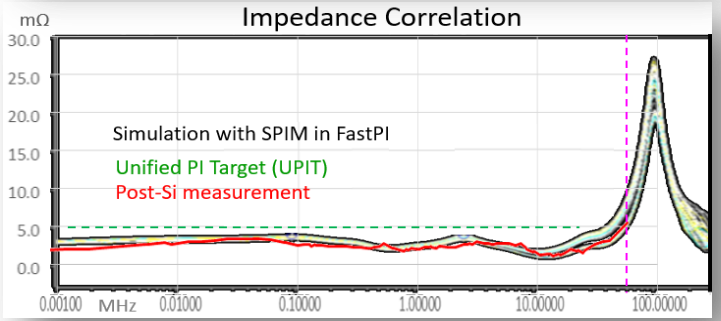


Impedance target is generally defined at sensing/feedback port.

UPIT - Unified Power Integrity (design) Target

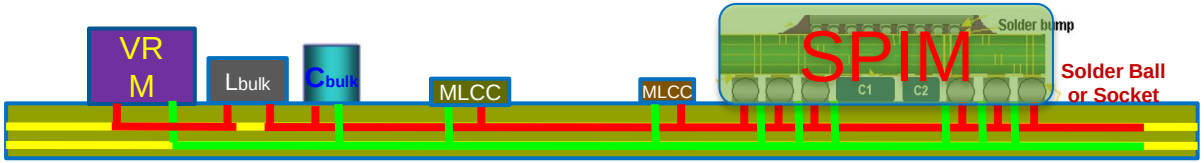
- Extended to cover PD
  - Conventionally PI covers >1MHz
  - Traditionally PD target defined in TD
  - Unified PD Target in FD
- Expanded to IO Power rails
  - Started for computing rails
  - Expanded as Z target, to IO power rails
  - Extrapolated from time domain
- Correlation for UPIT
  - Correlated in frequency domain
  - SPIM vs. conventional SPICE
  - Pre-Si simulation vs. Post-Si measurement



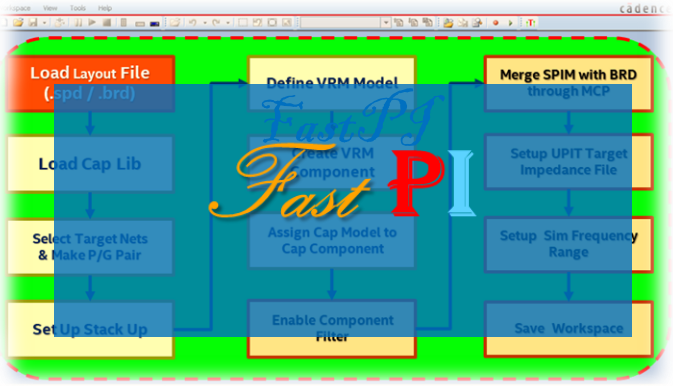


UPIT with SPIM has been well correlated with conventional SPICE, as well as post-Si measurement.

Platform PI Design: SPIM with UPIT in FastPI



- SPIM and UPIT has become one of the standard PI collaterals
- FastPI has been fully supported by two leading EDA vendors
- Proposing to make it 1st PI standard in the industry



IBIS BIRD Draft Example, for SPIM with UPIT included in IBIS

```
|
|SPIM 1
[SPIM] SPIM-1
VCC_Net VCC1
VSS_Net  VSS
[Port Group]
A1_1
VCC1        B28 B30 D28 D30 A28 A30 B26
VSS         B31 C31 D26 A26

A1_2
VCC1        E26 E28 E30 F28
VSS         F26 F30 F31

A1_3
VCC1        G26 G28 J27 J29 K28 K30
VSS         F26 F30 G30 K26 K31

A1_4
VCC1        B22 B23 B25 D23 D25 A23 A25
VSS         D22 D26 A22 A26
…
```

```
U1_1
VCC1        2082 2207
VSS         2179 2180

U1_2
VCC1        2085 2210
VSS         2182 2183
…
[SnP Model] SnP_model_1
[Snp File Name]
Icelake_VCC1_PKG.s58p
[END SnP Model]

[UPIT] UPIT-1
[OB Port]
OB_VCC1
[S1P File Name]
Icelake_VCC1_OB_TargetZ.s1p
[END UPIT]

[END SPIM]
```

Call to Action:

- Call to form a platform PI design standardization WG
- Call chip vendors to support FastPI architecture
- Call EDA vendors to support FastPI framework
- Call platform designers to adopt SPIM and UPIT
- Call to submit IBIS BIRD for SPIM with UPIT

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