Enhanced Mpilog Model for Power Integrity Analysis

A. Girardi[1], **I.S. Stievano**[2],:R. Izzi[1], T. Lessio[1], F.G. Canavero[2], I. Maio[2], L. Rigazio[2]

[1] Numonyx Italy S.r.l., [2] Politecnico di Torino, Italy

Ref. contacts: {antonio.girardi@numonyx.com, igor.stievano@polito.it}

MOCHA, MOdelling and CHAracterization for SiP - Signal and Power Integrity Analysis

❑ European Project FP7-ICT-2007-1 (Jan 2008 – Dec 2009)

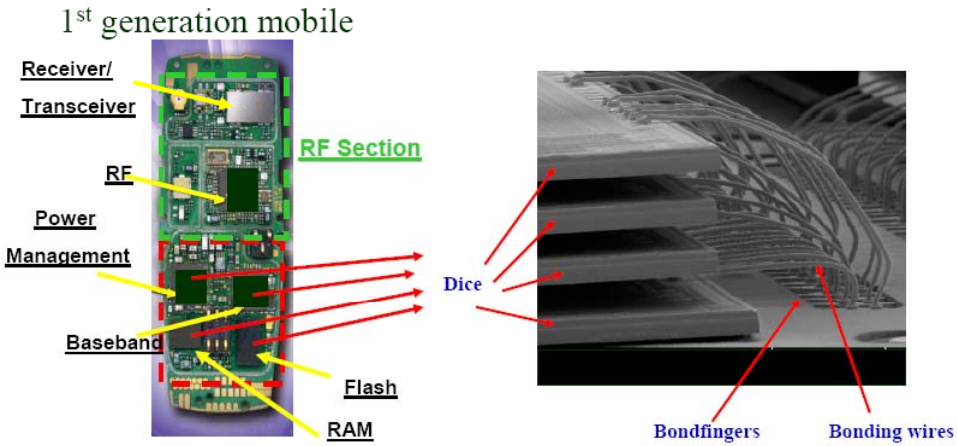
"Develop reliable modelling and simulation solutions for SiP design verification"

❑ Partecipants:

- **Numonyx Italy Srl (Italy) [Coordinator]**
- Politecnico di Torino (Italy)
- Cadence Design Systems Gmbh (Germany)
- Agilent Technologies (Belgium)
- Universidade de Aveiro (Portugal),
- Microwave Characterization Center (France)

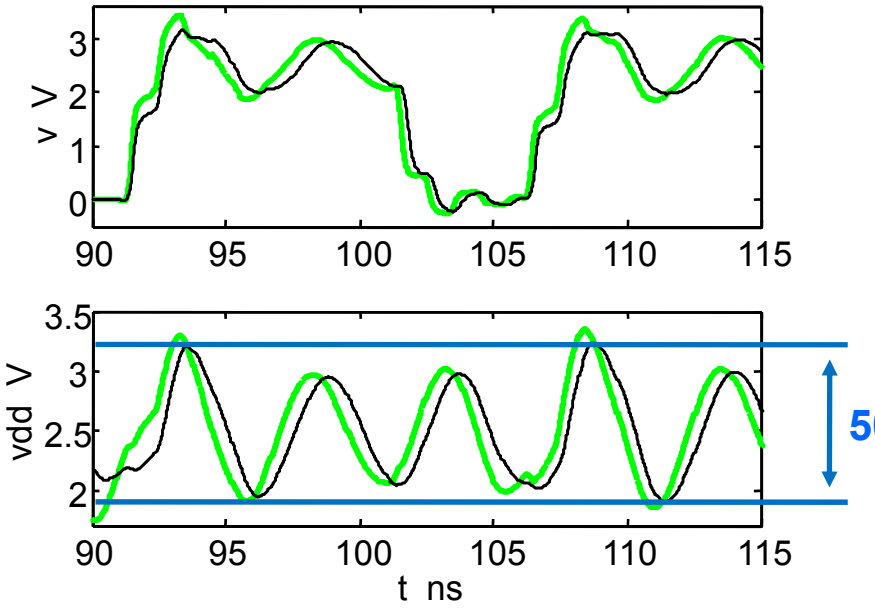
❑ Work Packages

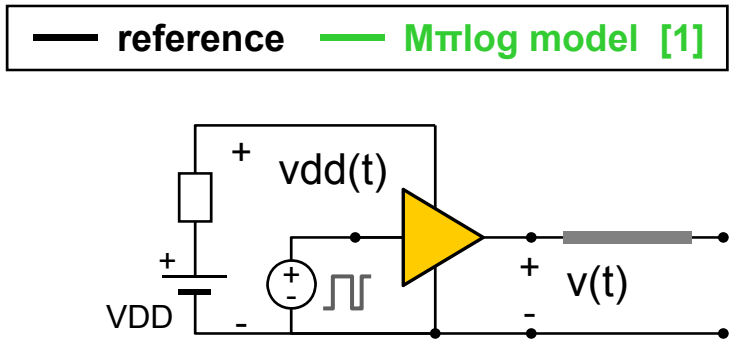
- IC power integrity model
- **IC buffers' innovative modelling approach**
- SiP design and verification EDA platform
- SiP signal integrity measurement platform



IC buffers' innovative modelling approach

- Recent applications (e.g., stacked SiP devices, → memories) exhibit large variation (30÷40%)
- State-of-the art models allow only for limited variations (10÷15% of the nominal power supply voltage)





[1] I.S.Stievano et. Al., "M[pi]log, Macromodeling via parametric identification of logic gates", TADVP 2004.

Overcome current limitations of existing models

Achievements

- Availability of the General structure of the extended model for digital buffers

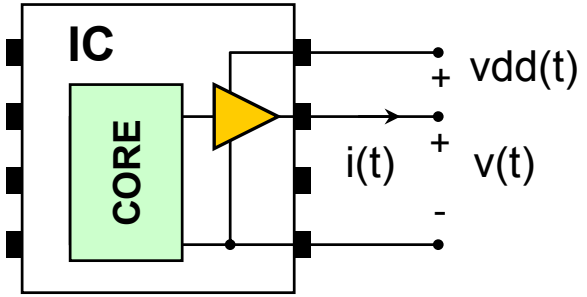
@ IBIS Summit, DATE 2008

- Procedure for parameter estimation from simulation / measurement
- Model implementation in different formats
- Application to test cases (proprietary and third party devices) from simulation
- Systematic assessment for
  - Accuracy
  - Efficiency

@ IBIS Summit, DATE 2009

State-of-the-art Mπlog model structure

e.g., IC output buffer (single-ended)



❑ **2-piece model representation**

$$i(t) = w_H(v,vdd,t)\, i_H(v,vdd,d/dt) + w_L(v,vdd,t)\, i_L(v,vdd,d/t)$$

$i_{H,L}$: submodels accounting for buffer behavior @ fixed logic H and L state

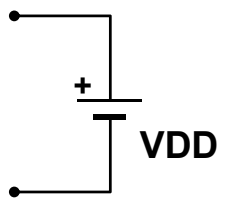
$w_{H,L}$: weighting signals for state switchings

❑ **Underlying (simplifying) assumptions**

Model parameters computed for the **nominal power supply VDD**

Weighting signals → $\mathbf{w_{H,L}(t)}$

Submodels $i_{H,L}$ → $\mathbf{i_H = i_H(vdd\text{-}v,d/dt)}$, $\mathbf{i_L = i_L(v,d/dt)}$



Enhanced model structure

$$i(t) = \begin{matrix} w_H(v,VDD,t) \\ w_L(v,VDD,t) \end{matrix} * \begin{matrix} i_H(VDD-v) \\ i_L(v,VDD) \end{matrix} +$$

$$w_{H,L}(t - \tau(vdd))$$

- Include the dependence of switching events on vdd

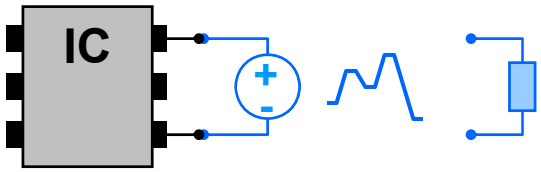
$$i_{H,L}(v,vdd,d/dt) = k_{H,L}(vdd) * i_{H,L}(v,VDD)$$

- Must depend on both v and vdd
- Simple yet accurate solution: approximate a complex 2D relation with a 1D curve * coefficient

- ❑ differences in two terms only
- ❑ no additional characterization required
- ❑ improved accuracy
- ❑ same complexity

Parameter estimation

Step 1: follow the same procedure for the estimation of the classical MπIog model



- **Device is conveniently stimulated and reaction is recorded**
- **Device responses to fit model responses via optimization algorithms**

…from simulation

[1] I. S. Stievano et Al., “Behavioral models of IC output buffers from on-the-fly measurements,” IEEE Transactions on Instrumentation and Measurement, vol. 57, No. 4, 2008.

…from measured data

[2] I. S. Stievano et Al. , "Behavioral modeling of digital devices via composite local-linear state-space relations," IEEE Transactions on Instrumentation and Measurement, Vol. 57, No. 8, 2008

Parameter estimation, cont'd

Step 2: compute the two additional parameters

$$i_{H,L}(v,vdd,d/dt) = k_{H,L}(vdd) * i_{H,L}(v,VDD)$$

$$w_{H,L}(t - \tau(vdd))$$

…from simulation

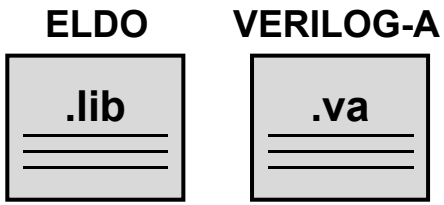
Parameters computed from the transistor level responses of buffer transistor-level model **(parameters as tabular data)**

…from measured data

Use analytical approximations from basic MOS equations **(parameters as functions)**

Model implementation

- **Model equations have been implemented in SPICE and hardware description languages**

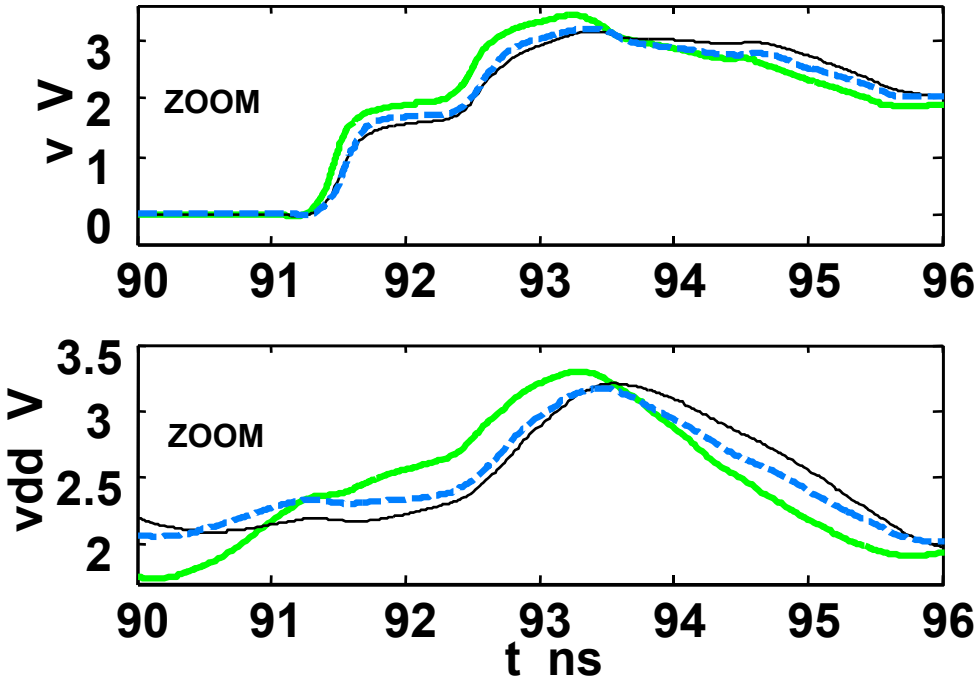


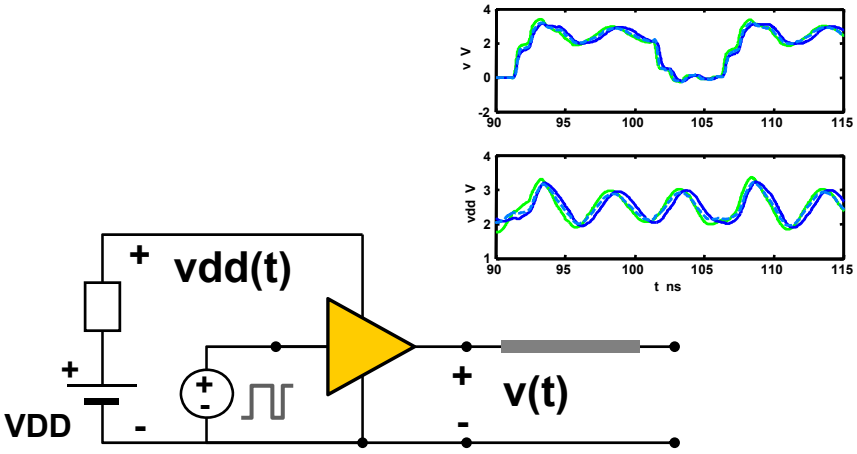
e.g, Verilog-A

```
module drvmod(v,vdd,ref,w1,w2,w3,w4,di,ref2);
        electrical v,vdd,ref,f1,f2,f3,f4,f6,ref2,myVo;
        parameter real VDD=2.5;
        analog
            V(myVo) <+ V(v,ref)-V(vdd,ref)+VDD;
        drvmod_core DRVCORE(v,vdd,ref,w1,w2,w3,w4,di,f1,f2,f3,f4,f6);
        drvmod_fH DRV1(f1,myVo,ref2);
        drvmod_fL DRV2(f2,v,ref2);
        …
endmodule
```

Enhanced model performance

- preliminary validation test case





reference — Mπlog model

enhanced model (static & delay comp.)

Accuracy confirmed for vdd(t) > 40% VDD

Current vs. enhanced models

$$i(t) = w_H(v,vdd,t)\, i_H(v,vdd,d/dt) + w_L(v,vdd,t)\, i_L(v,vdd,d/t)$$

Model	Submodels $i_{H,L}$	Weighting signals $w_{H,L}$
Mπlog	$i_{H,L}(v,VDD,d/dt)$	$w_{H,L}(t)$
Enhanced Mπlog	$i_{H,L}(v,vdd,d/dt)$	$w_{H,L}(t-\tau(vdd))$

- no additional characterization required
- same complexity → same speed-up (10 ÷ 100x)

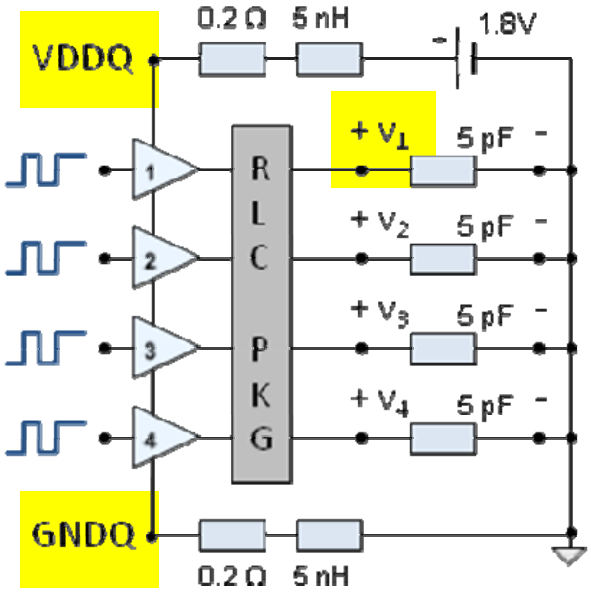
Validation test cases

First test case:	512Mb NOR Flash memory in 90nm technology (Numonyx proprietary device)
Second test case:	512Mb DDR third party device, in 70nm technology and clock frequency of 133MHz
Third test case:	Test chip designed by Numonyx in 90nm technology, with a Low Power DDR interface for I/O buffers and a clock frequency of 166MHz.

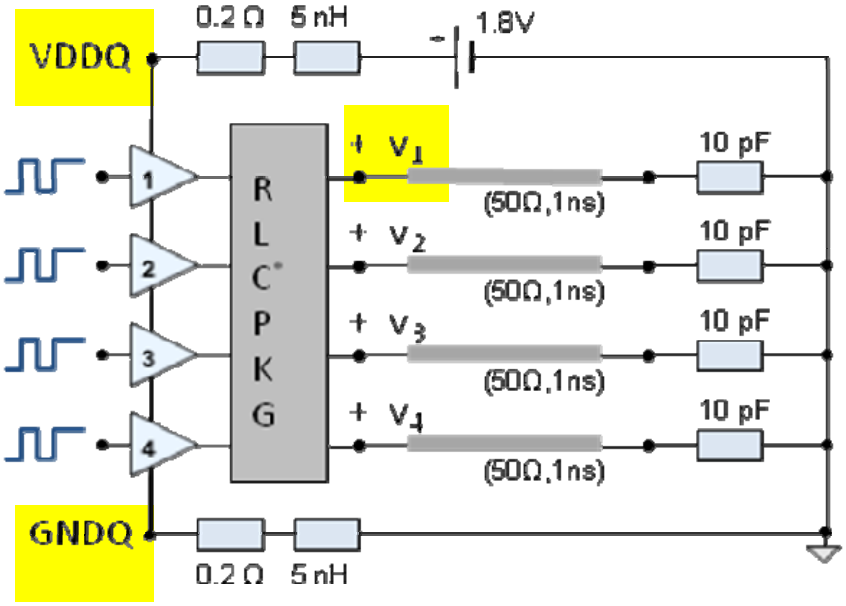
Same results (accuracy and efficiency) for the three examples!

Simulation test setups

Setup (A)

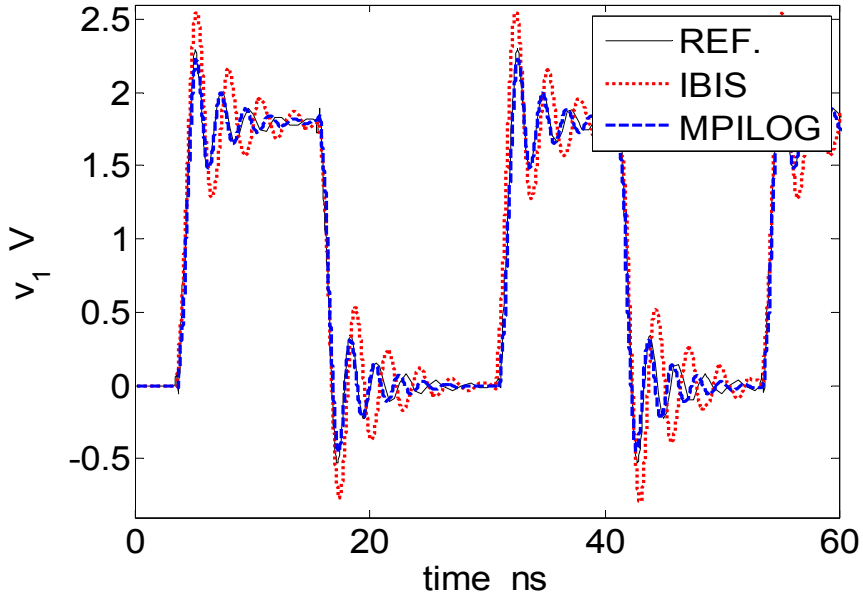


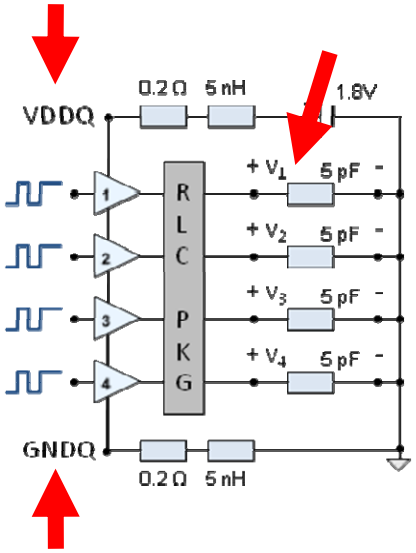
Setup (B)

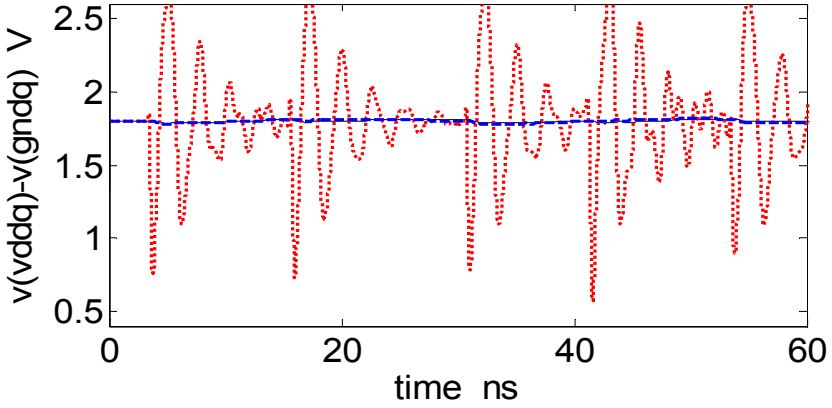


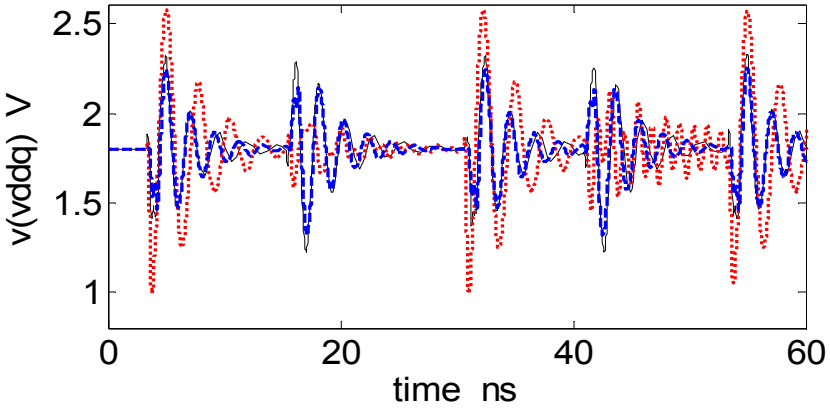
RLC PKG: R=200mΩ, L=10nH, C=0.5pF

Accuracy – 2nd test case (Setup A)

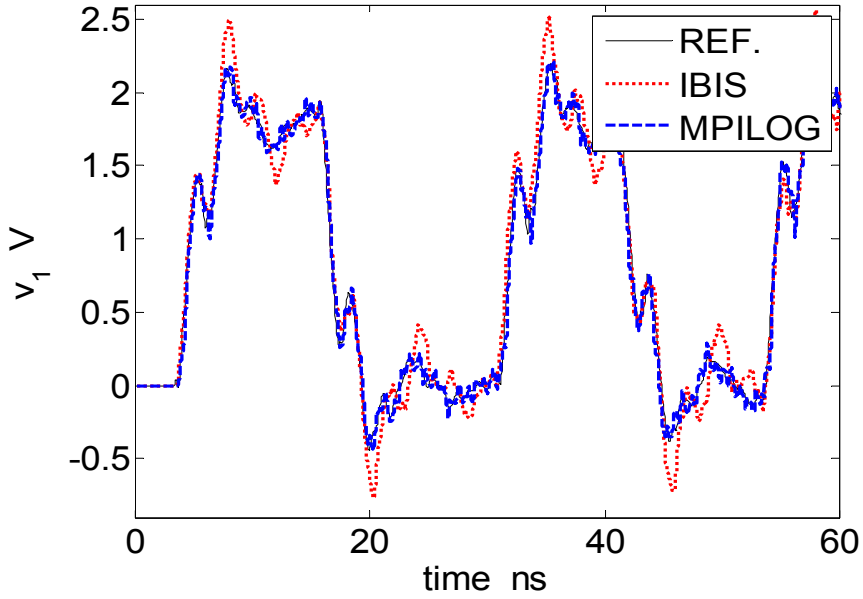


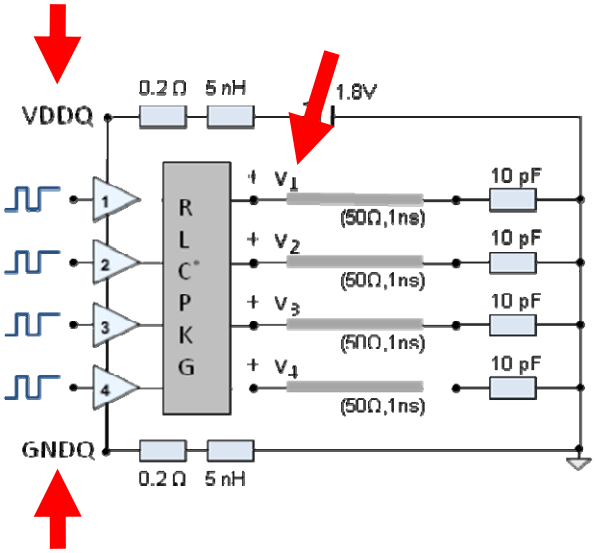


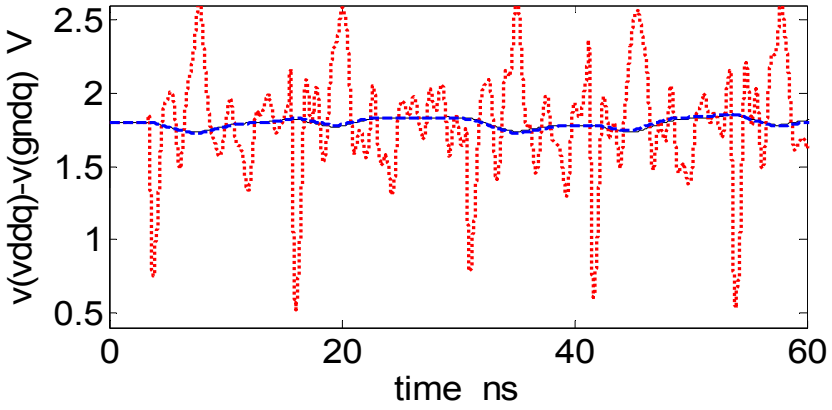


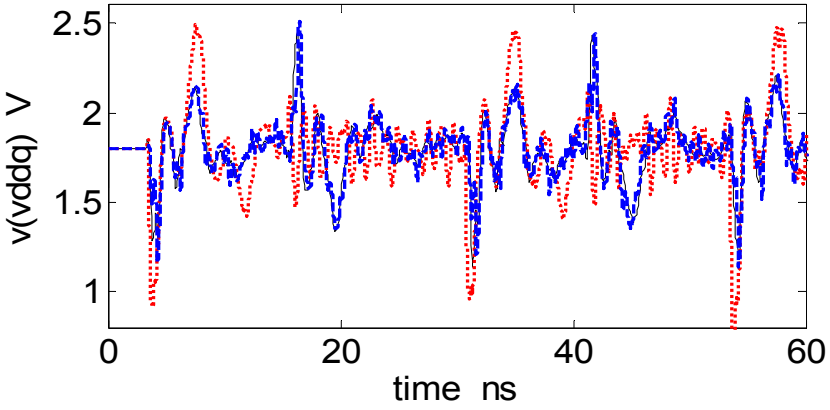


Accuracy – 2nd test case (Setup B)

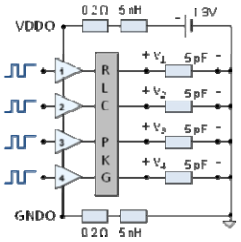


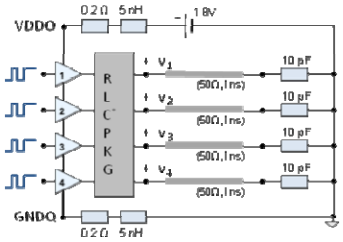






Accuracy figures, 2nd test case





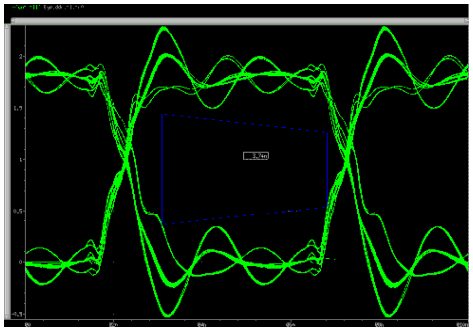
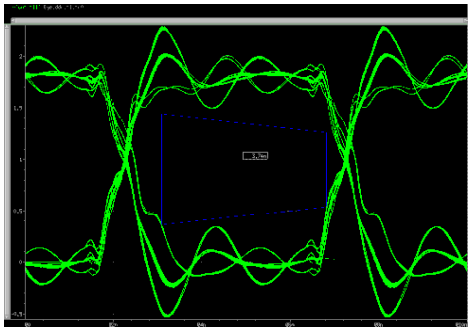
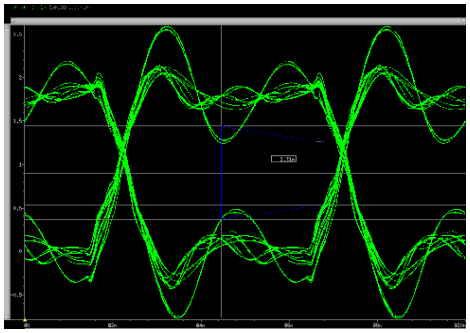
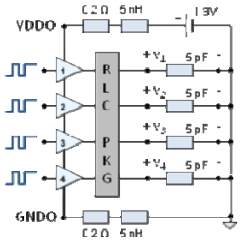
	Setup (a), second test case		Setup (b), second test case	
	Max rel. timing error on $v_1(t)$ (low-to-high event)	Max rel. timing error on $v_1(t)$ (high-to-low event)	Max rel. timing error on $v_1(t)$ (low-to-high event)	Max rel. timing error on $v_1(t)$ (high-to-low event)
IBIS	37 %	10 %	87 %	25 %
MPILOG	6 %	12 %	75 %	12 %
	Max relative error of vddq(ref.)-vddq(model)	Max relative error of gndq(ref.)-gndq(model)	Max relative error of vddq(ref.)-vddq(model)	Max relative error of gndq(ref.)-gndq(model)
IBIS	47 %	38 %	71 %	50 %
MPILOG	14 %	14 %	32 %	31 %
	Standard deviation of vddq(ref.)-vddq(model)	Standard deviation of gndq(ref.)-gndq(model)	Standard deviation of vddq(ref.)-vddq(model)	Standard deviation of gndq(ref.)-gndq(model)
IBIS	195 mV	170 mV	302 mV	250 mV
MPILOG	99 mV	110 mV	103 mV	103 mV

Application: Eye diagrams

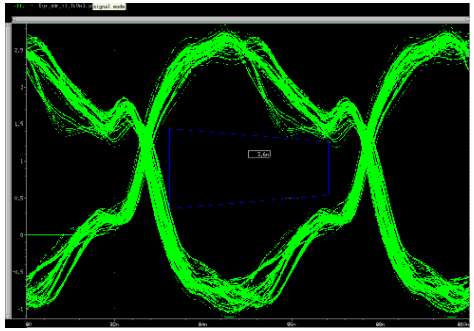
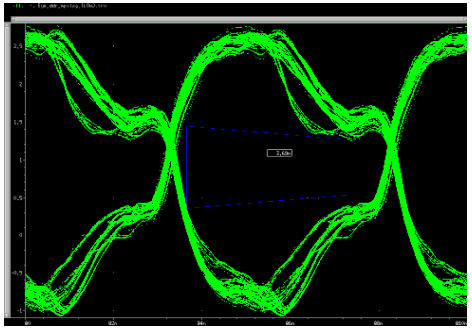
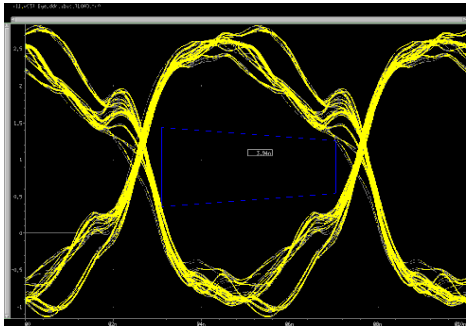
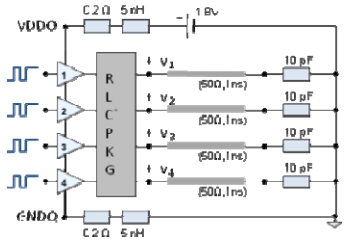
- **DDR, second test case**

Reference **Mπlog** **IBIS**

Setup A

Setup B

Application: Eye diagrams

❑ DDR second test case

	Setup (a), second test case		Setup (b), second test case	
	Eye opening	Error	Eye opening	Error
Reference (trans. level)	73.8%	-	72%	-
IBIS	46.2 %	38.3 %	78.8 %	9.5 %
MPILOG	77.6 %	3.75 %	73.8 %	2.5 %

❑ DDR third test case

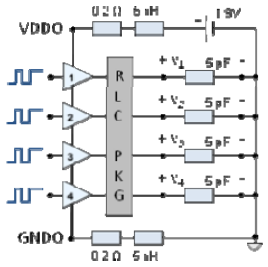
	Setup (a), third test case		Setup (b), third trst case	
	Eye opening	Error	Eye opening	Error
Reference (trans. level)	70.2%	-	64%	-
IBIS	80.6 %	14.8 %	70.8 %	10.6 %
MPILOG	76 %	5.3 %	65.8 %	2.8 %

Conclusions

- Generation of **enhanced device models** for large VDD variations (>30%); tabular data or simplified analytical equations to account for vdd
- **High accuracy** verified on realistic tests
- **High efficiency**

e.g., 2nd test case, setup (A)

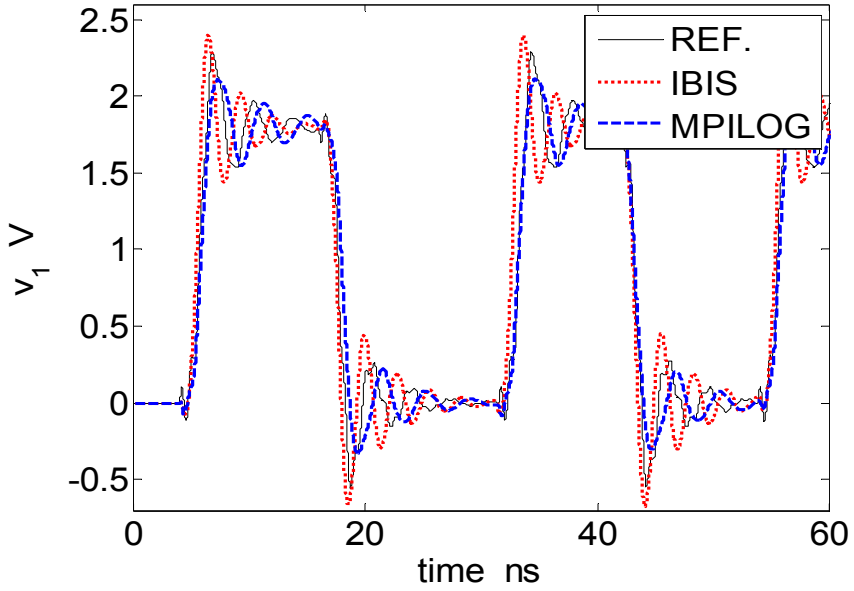
	CPU time	Speed-up
Reference	773 s	-
IBIS	13 s	59 x
MPILOG	31 s	25 x

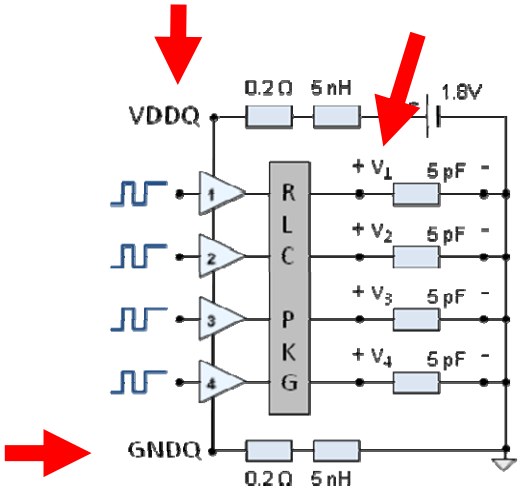


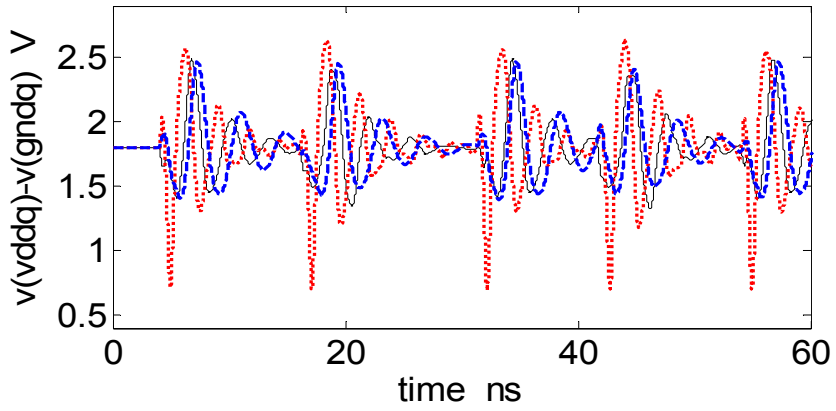
- **Mπlog modeling tool (ver. 5.2)** freely available for downloading @ **www.emc.polito.it**

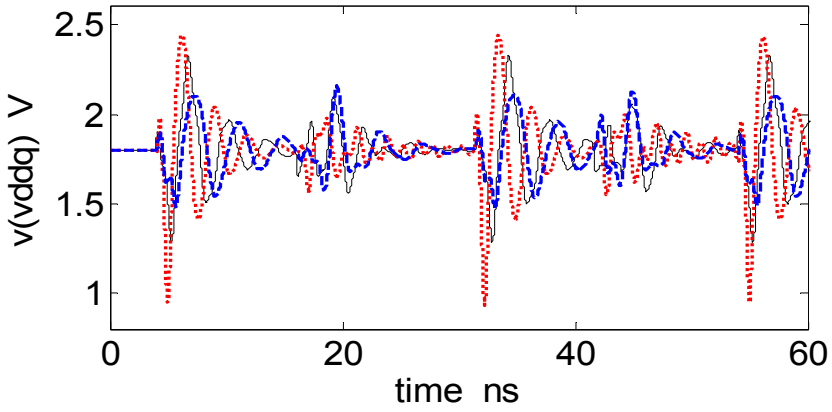
Q&A

Accuracy – 1st test case (Setup A)

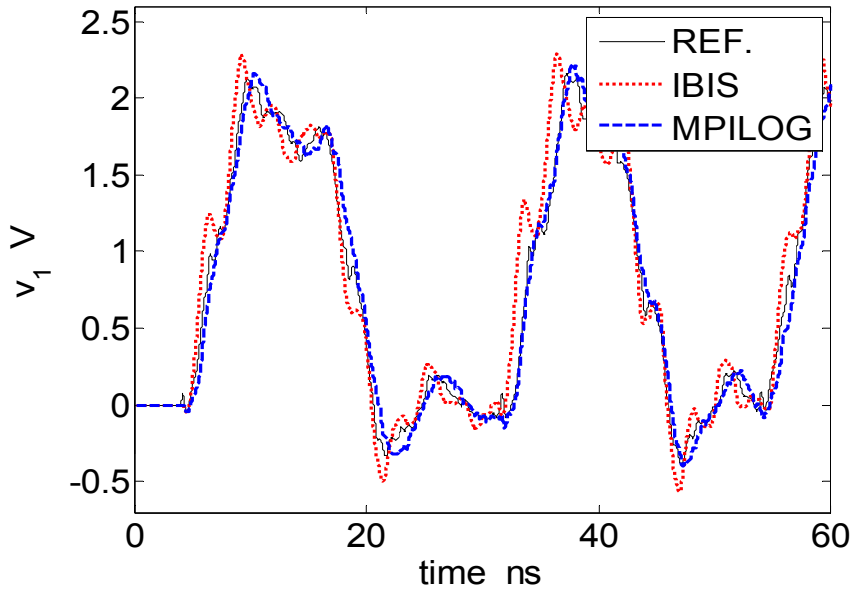


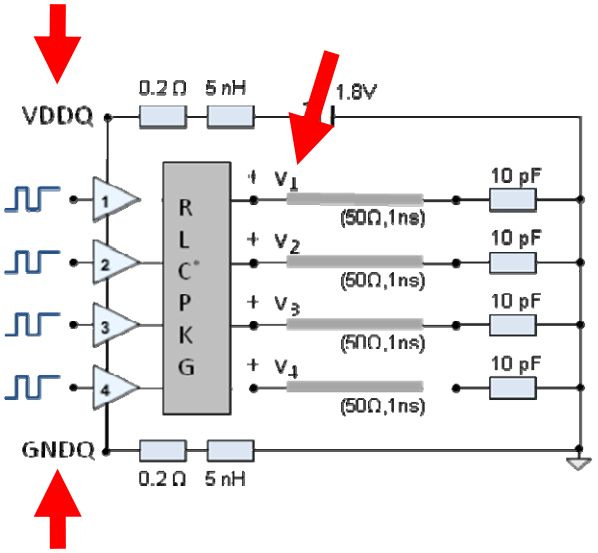


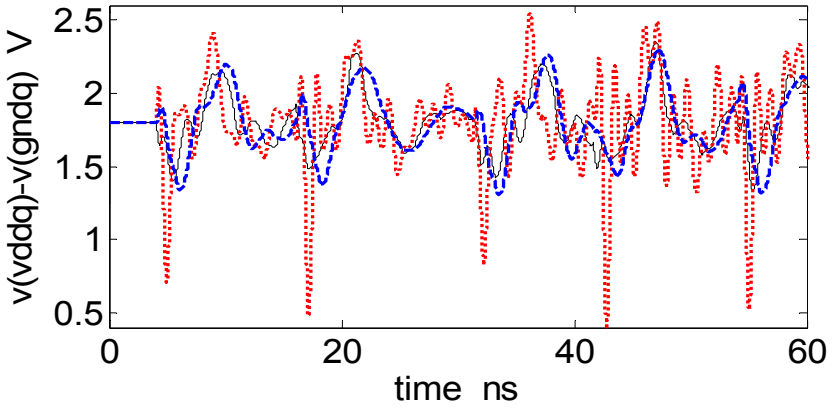


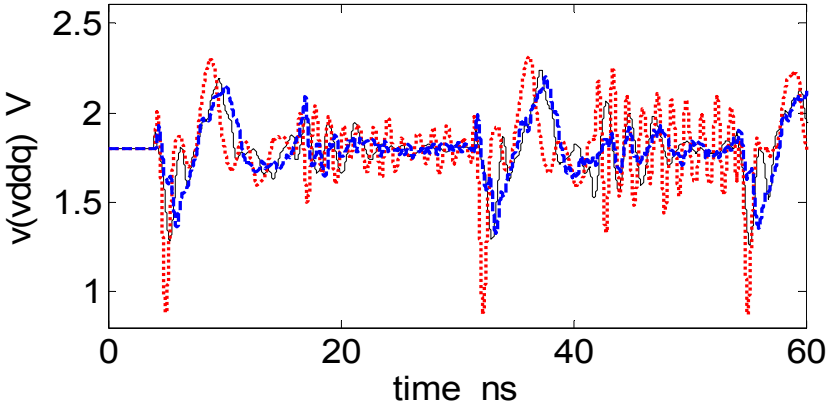


Accuracy – 1st test case (Setup B)

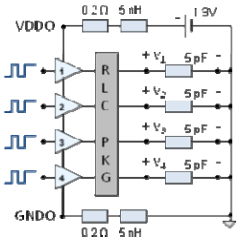


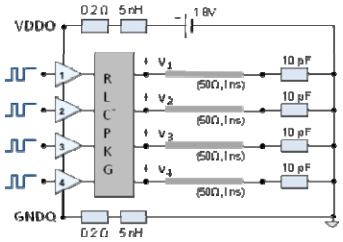






Accuracy figures, 1st test case

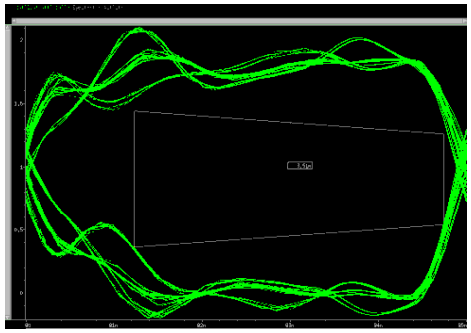
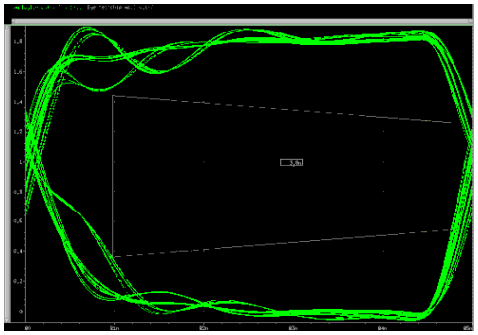
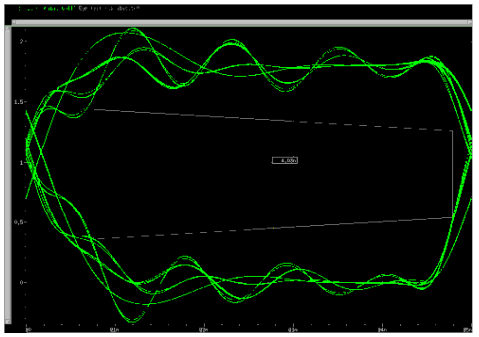
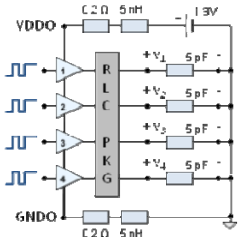
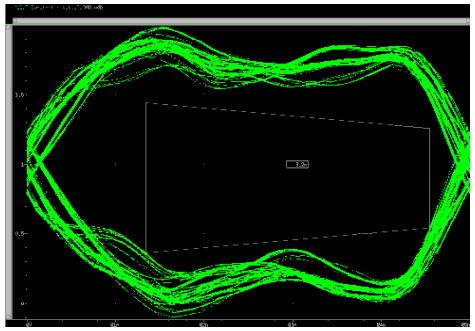
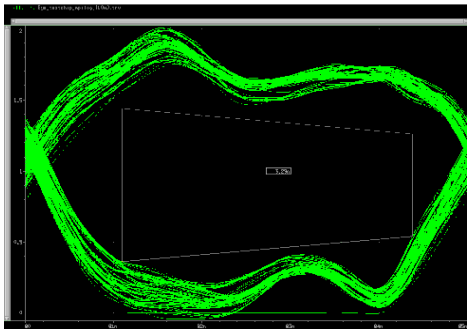
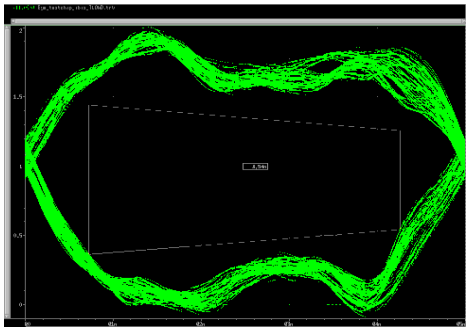
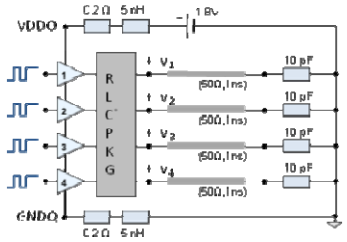




	Setup (a), first test case		Setup (b), first test case	
	Max rel. timing error on $v_1(t)$ (low-to-high event)	Max rel. timing error on $v_1(t)$ (high-to-low event)	Max rel. timing error on $v_1(t)$ (low-to-high event)	Max rel. timing error on $v_1(t)$ (high-to-low event)
IBIS	36%	12 %	70 %	47 %
MPILOG	7 %	26 %	7 %	50 %
	Max relative error of vddq(ref.)-vddq(model)	Max relative error of gndq(ref.)-gndq(model)	Max relative error of vddq(ref.)-vddq(model)	Max relative error of gndq(ref.)-gndq(model)
IBIS	43 %	29 %	37 %	26 %
MPILOG	18 %	25 %	21 %	20 %
	Standard deviation of vddq(ref.)-vddq(model)	Standard deviation of gndq(ref.)-gndq(model)	Standard deviation of vddq(ref.)-vddq(model)	Standard deviation of gndq(ref.)-gndq(model)
IBIS	218 mV	166 mV	324 mV	308 mV
MPILOG	121 mV	130 mV	86 mV	86 mV

Application: Eye diagrams

- **DDR, third test case**

	Reference	Mπlog	IBIS	
Setup A				
Setup B				

Application: Eye diagrams

❑ DDR second test case

	Setup (a), second test case		Setup (b), second test case	
	Eye opening	Error	Eye opening	Error
Reference (trans. level)	73.8%	-	72%	-
IBIS	46.2 %	38.3 %	78.8 %	9.5 %
MPILOG	77.6 %	3.75 %	73.8 %	2.5 %

❑ DDR third test case

	Setup (a), third test case		Setup (b), third trst case	
	Eye opening	Error	Eye opening	Error
Reference (trans. level)	70.2%	-	64%	-
IBIS	80.6 %	14.8 %	70.8 %	10.6 %
MPILOG	76 %	5.3 %	65.8 %	2.8 %