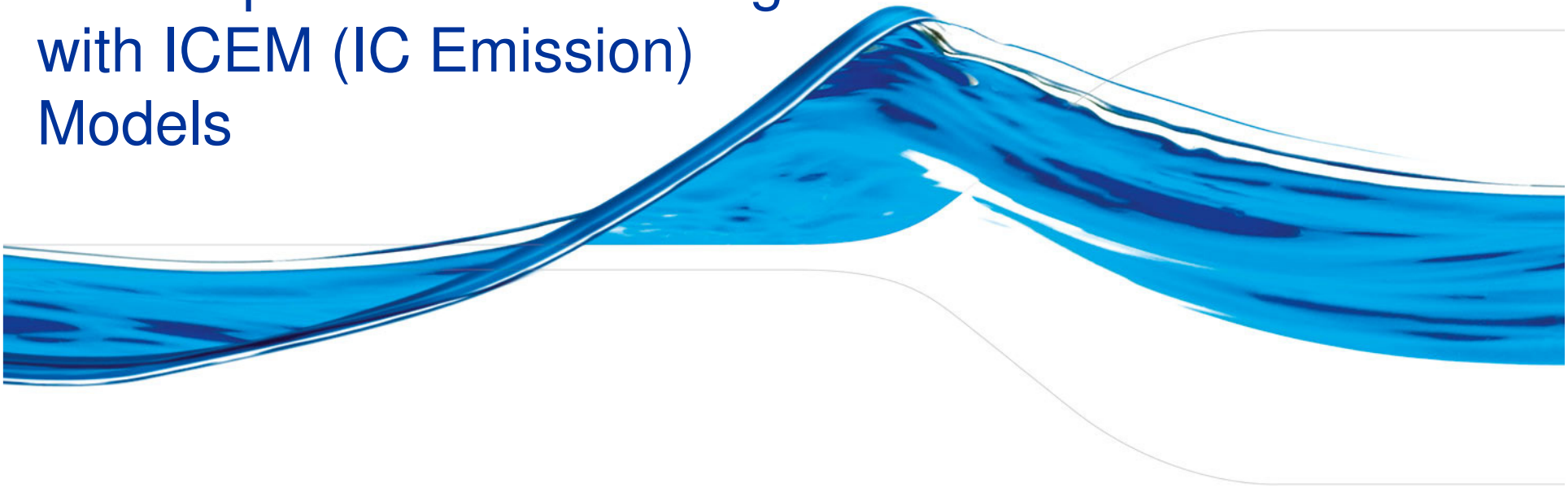
First Experiences in dealing with ICEM (IC Emission) Models



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Goal of this Presentation

Already did an ICEM status presentation 3 years ago → meant as an status update what happened since then.

Aim of this presentation is to give an update after some ICEM related work which took place in the last 3 years in MEDEA project (PARACHUTE).

Some of the pictures are borrowed from Etienne Sicard (INSA) and Thomas Steinecke (Infineon) or are related to the European funded project Medea+/Eureka Parachute Project A701 (shown at DATe booth as well).

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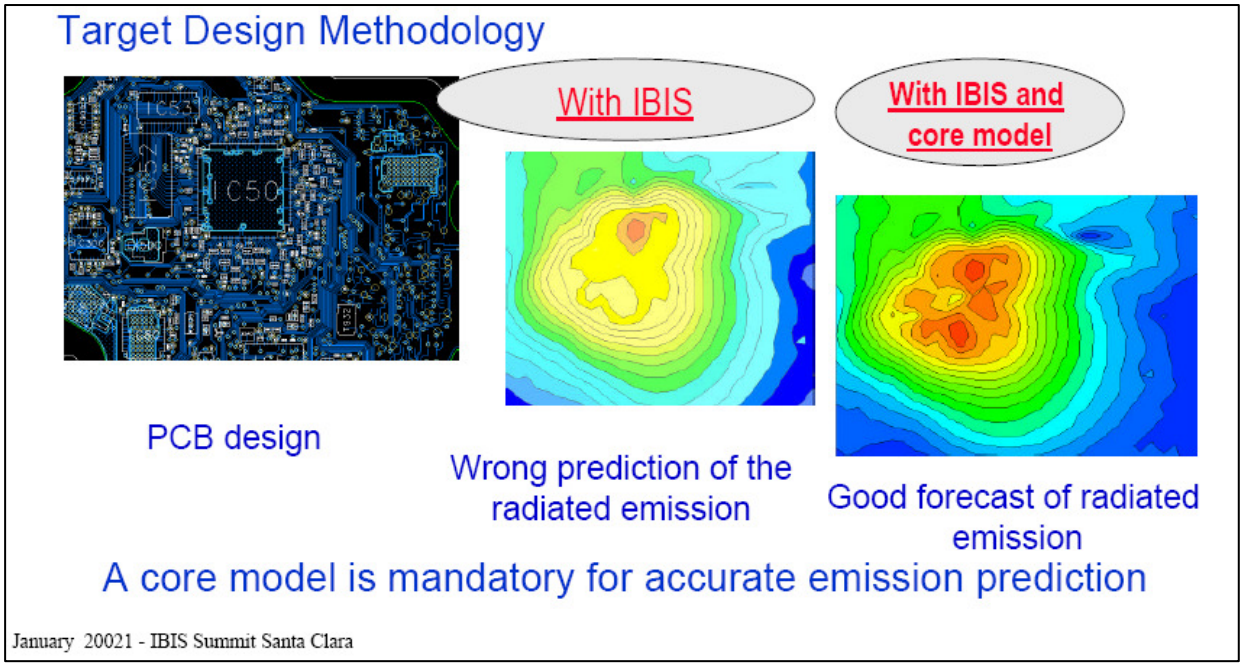
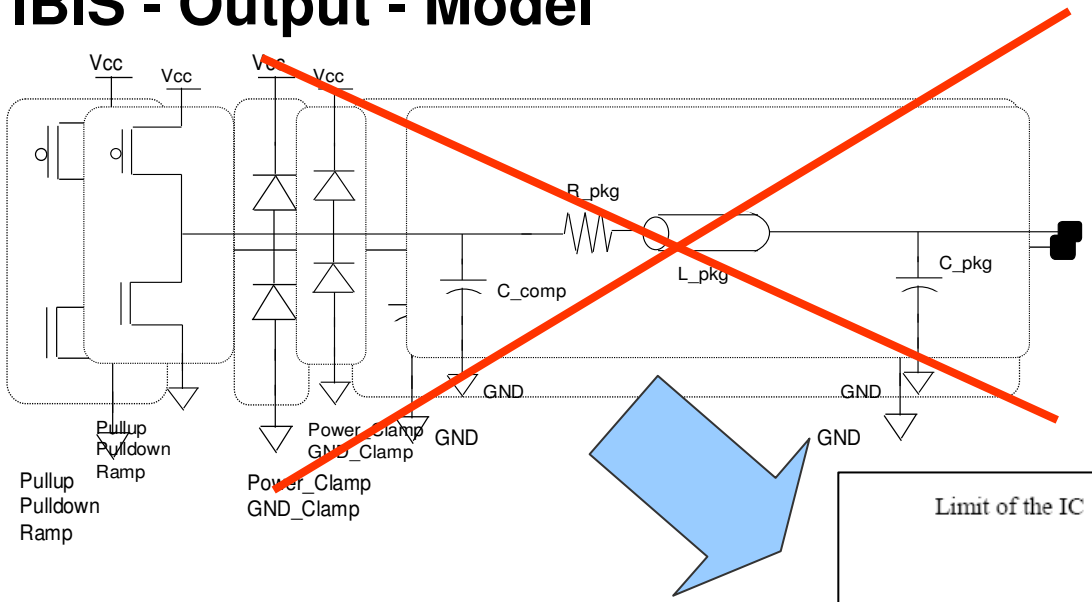
ICEM ? IBIS for EMI analysis ?

- IBIS models repesent voltage versus time (edges) or voltage versus current (clamps)
- Relevant information for EMC analysis, especially on core activity and the switching currents within the ICs is lacking.
- ICEM has been initiated years ago (slide below from 2001 !!!)
- Driving forces:
  - Aerospace
  - Automotive
- Standardized format

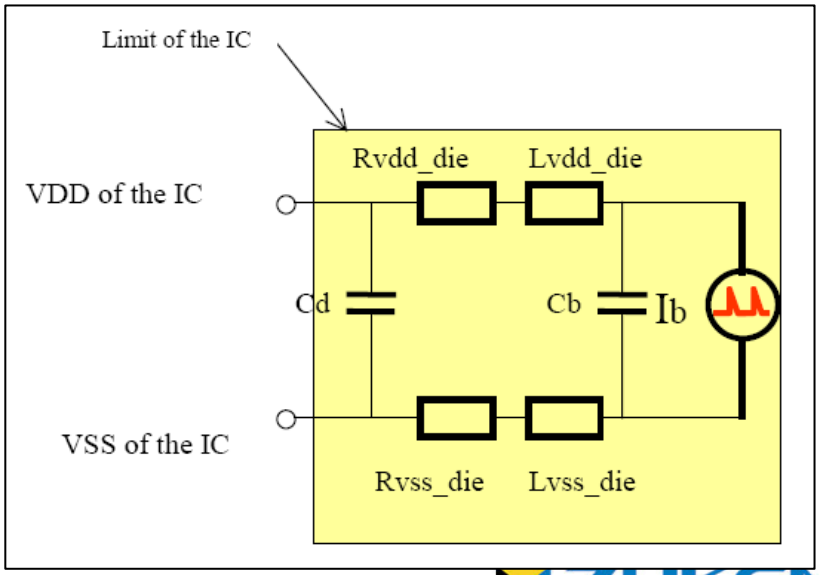


IBIS & ICEM Models in EMC Context

IBIS - Output - Model



ICEM Model

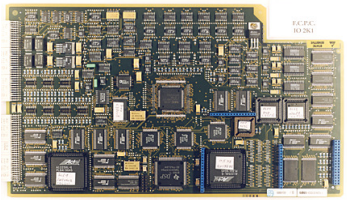


Driving Force: Automotive &Aerospace) (still the only ones ?)

Susceptibility

Equipments

Boards



Component

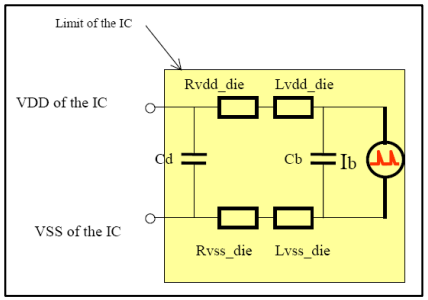
Emission

Personal entrainments

Mobile phone

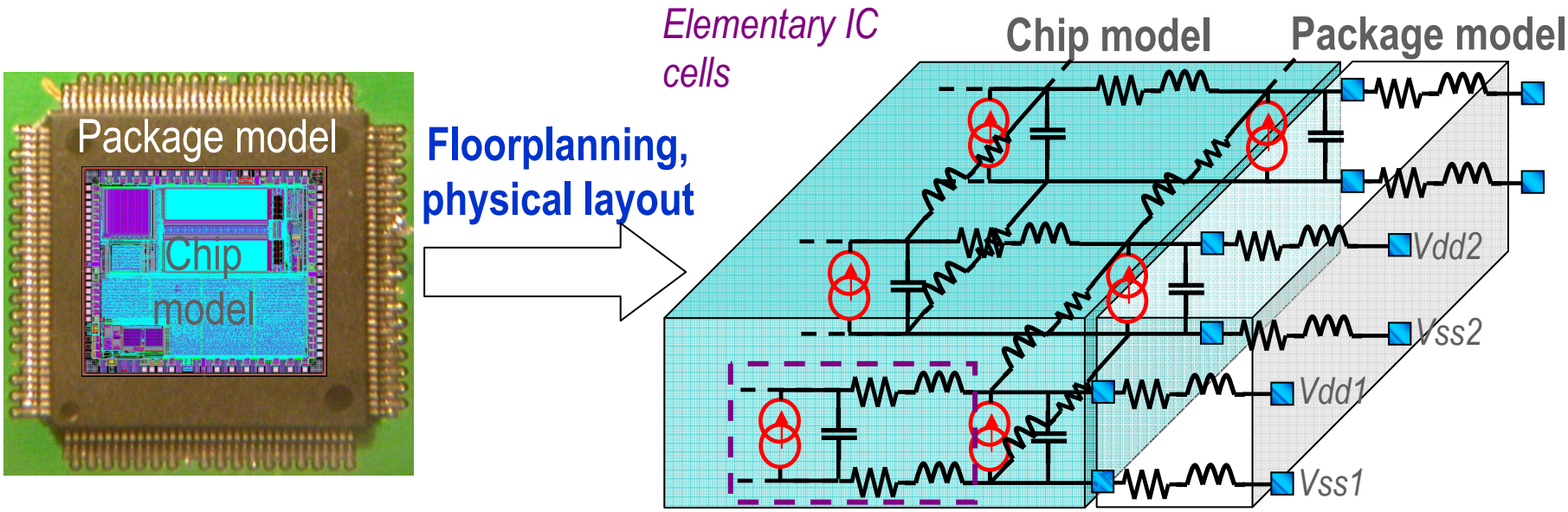
Safety systems

Content of an ICEM Model



Ib	Current source. Unit: Ampere Description: piece-wise-linear	Main source of parasitic emission considered in the model is the current source Ib. The current shape may consist either of the time-domain description of the current versus time or as an equivalent triangular waveform. Typical values for Ib are several mA, up to 1A for the amplitude, 0.5 to 5ns for duration, and 500ps to 50ns for the period.
Cd	Decoupling capacitance. Unit: Farad Description: discrete C	On-chip decoupling capacitance between VDD and VSS. Cd is a physical coupling between the internal supply rails VDD (positive supply) and the ground rail VSS (0V supply). The origin of the capacitance Cd is rail to rail or junction capacitance. Typical value ranges from 100pF (very small Ics) up to 20nF (0.18µm System-on-chip).
Lvdd_die, Lvss_die	Serial internal inductance. Unit: Henry Description: discrete L	The serial inductance Lvdd_die, Lvss_die, in serial with the local block capacitance Cb creates a high frequency resonance effect. Typical value ranges from 0.1nH (very short connection to supply) up to 10nH (long connection).
Rvdd die, Rvss_die	Serial internal resistance. Unit: Ohm Description: discrete R	The serial resistance of the supply network models the path that connects the block supply to the main supply ring. Typical value for Rvdd, Rvss are 0.5 to 50 ohm.
Cb	Block decoupling capacitance. Unit: Farad Description: discrete C	The local block decoupling Cb is the local supply-to-ground capacitance placed in serial with the local current generator Id. It accounts for the equivalent decoupling capacitance of the block. Separating the block capacitance from the on-chip capacitance Cd creates a second LC network (Lvdd, Cb, Lvss) at the origin of a secondary resonance.

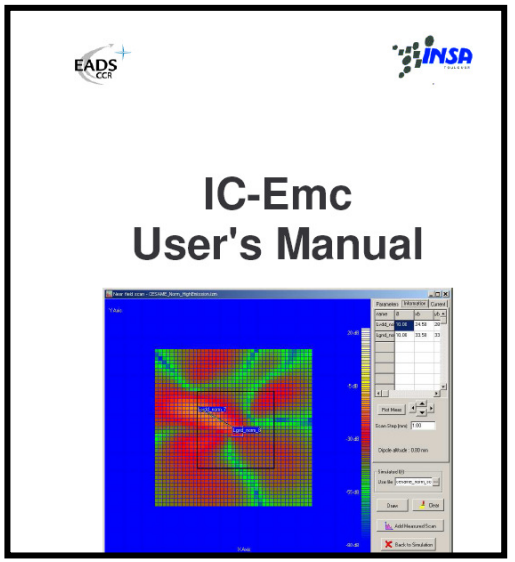
ICEM Core Model Structure

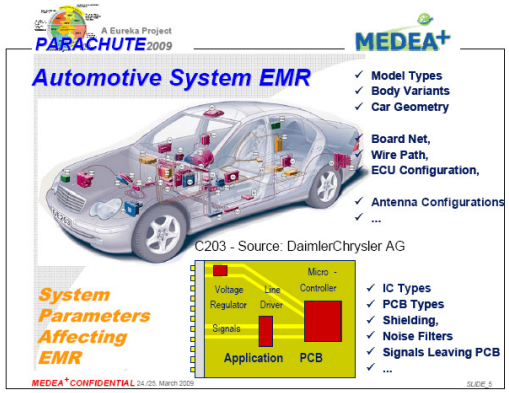


- Full chip switching noise analysis, mapping of voltage drop, evaluation of power integrity, crosstalk, EMI, effect of on-chip decoupling.
- Very large netlists.
- Too much complex to add PCB model.

ICEM Resources/Activities

- There exists already:
  - ICEM Cookbook
  - Some Tooling (IC-Emc)
  - Some EDA tool work (research oriented)
- Still only few samples available
- Very research project oriented
  - MESDIE
  - EMC-Pack (PIDEA)
  - Parachute
  - others





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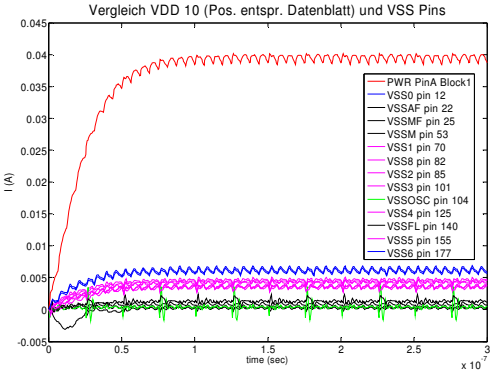
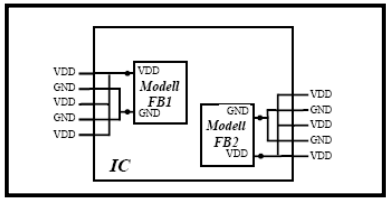
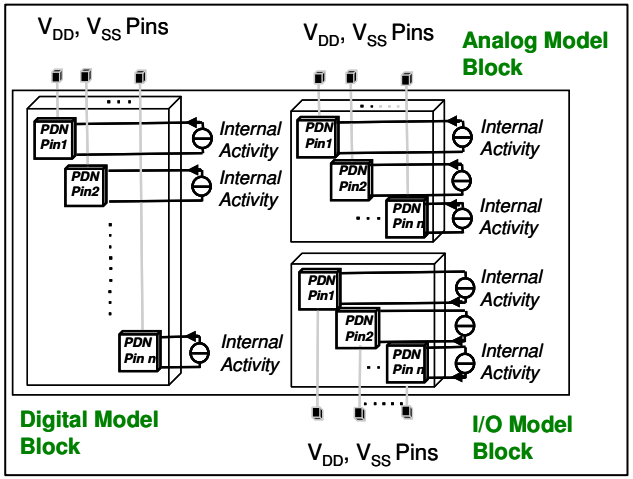
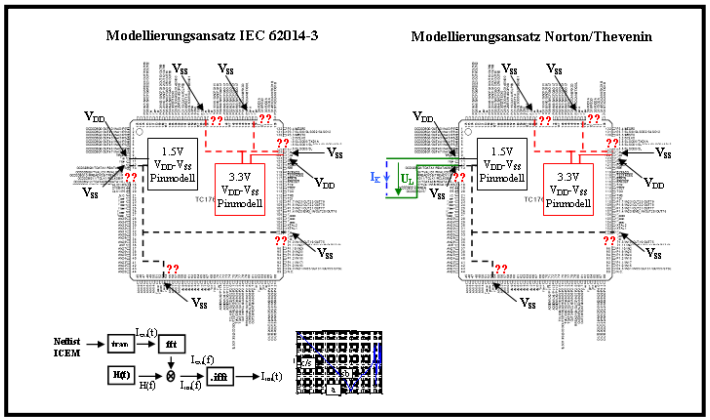
ICEM Modelling Challenges

- Various Modelling Challenges
  - Correlation Vss/Vdd Pins within the IC
  - Internal activity (IA) model (current source)
  - Model resolution
  - Various PWR/GND pins have different **I(t)**
  - Functional IC blocks (i.e. Flash) can share power supply
    - Internal coupling effects



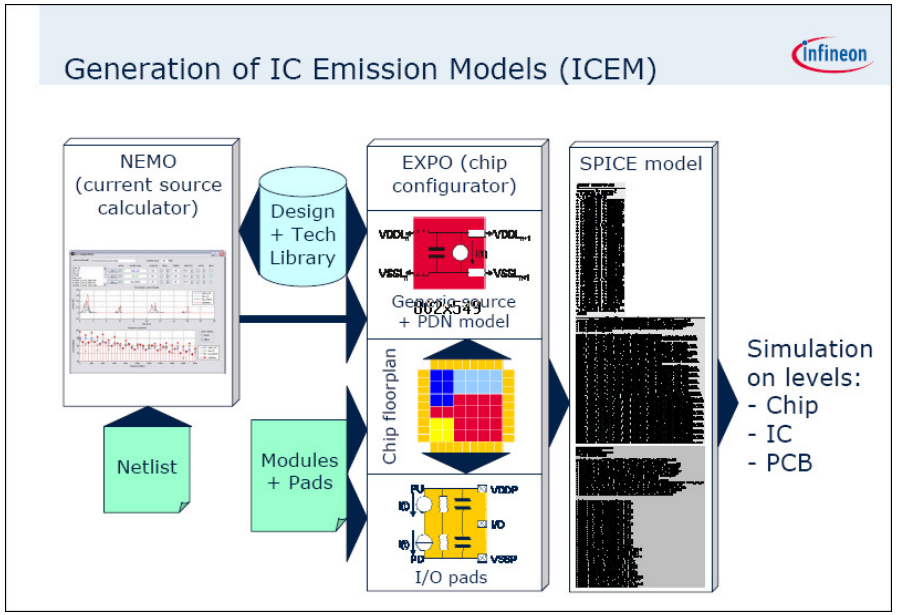




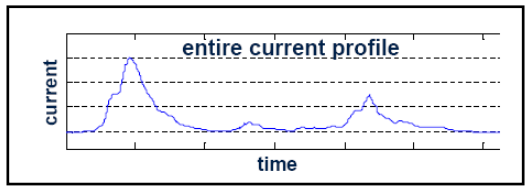


Semiconductor Vendor Activities

- Just little support or commitments from semiconductor vendors (TI, Atmel, NXP and Freescale unclear).
- Infineon has inhouse toolchain for ICEM development ready (taking netlist from IC design flow and package information, NEMO), then generation of ICEM models (large SPICE netlists, EXPO).



- Result: current profile d(I)/d(t)



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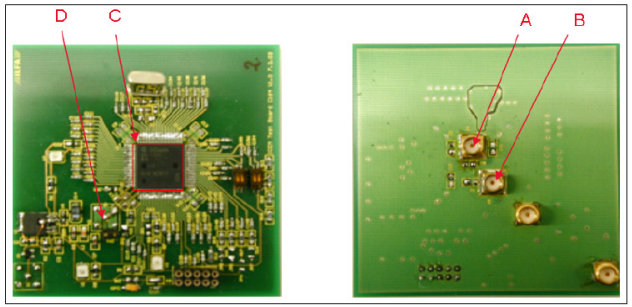
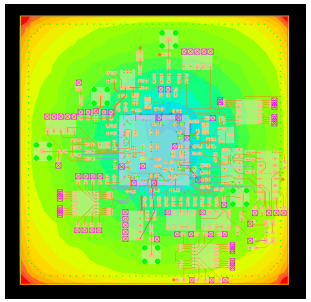
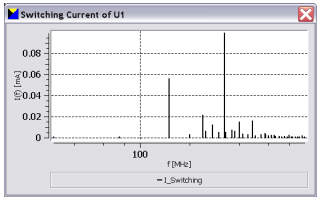
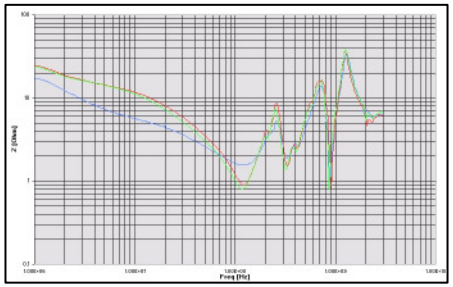
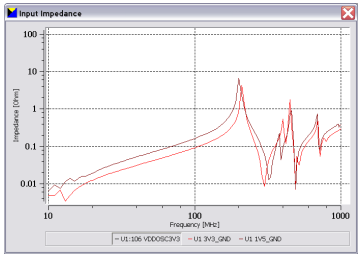
Parachute MEDEA Project: ICEM Demonstrator for EMC/PI Simulation

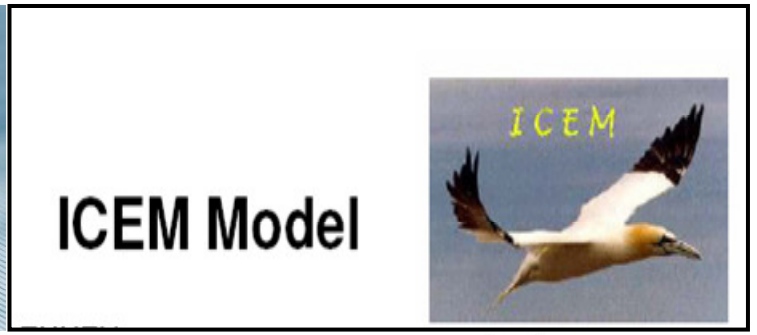












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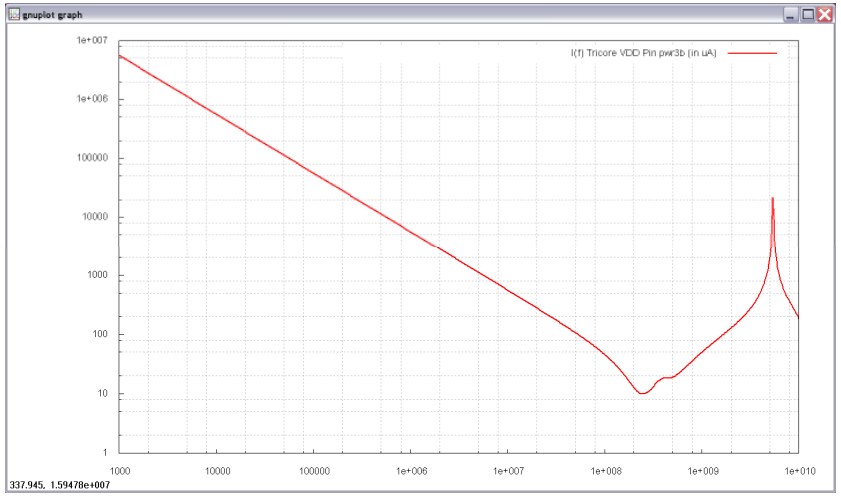
Practical Experiences & Observations

- ICEM model definition allows to define models with various granularity levels of the DIE → different model complexity
- Models with high resultion are HUGE → hours (or days) simulation time (time domain)
- Correlation of simulation results challenging (as well SPICE issues)
- ICEM model as it is cannot been used ready to run like IBIS models

- Generation of Z11(f) from HSPICE AC simulation possible → multiple simulation runs !
- Simplification of models mandatory for practical use in electronic design flow (i.e. mathematical MOR approaches) or usage of parts of an ICEM model (i.e. I(f) of each single power pin extracted from large model)



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Conclusion & Outlook

- ICEM is still not at that status as expected by its initators !
  - Only few models available
  - Only limited tool/simulation support
- Still a chicken-egg issue (no models → no tools & no tools → no models)
- Some companies commit to ICEM for application specifuc ICs (i.e. automotive)
- ICEM application currently seen more for IC design flow then for electronic design (boards, systems) –
  CAUTION: Personal judgement !!!