IdEM & MπLOG: MACROMODELING TOOLS FOR SYSTEM-LEVEL SIGNAL INTEGRITY AND EMC ASSESSMENT

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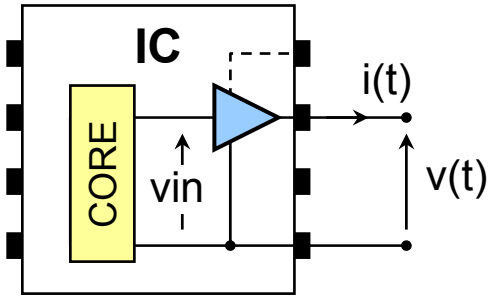
Outline

- **MπIog - Macromodeling via Parametric Identification of LOgic Gates**
- **IdEM - Identification of Electrical Macromodels**

Review of IC model generation (i)

e.g., IC output buffer (single-ended)



In any approach, 2-piece model representation

$$i(t) = w_H(t)\, i_H(v,d/dt) + w_L(t) i_L(v,d/t)$$

$i_{H,L}$: submodels accounting for buffer behavior @ fixed logic H and L state

$w_{H,L}$: weighting signals for state switchings

→ **suitable modifications for handling power/ground pins and different device technologies**

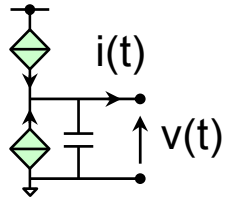
Review of IC model generation (ii)

Classification

$$i(t) = w_H(t)\, i_H(v,d/dt) + w_L(t)\, i_L(v,d/dt)$$

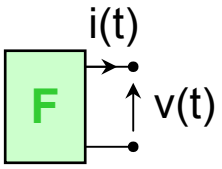
- **Equivalent circuits**

  → Input Output Buffer Information Specification, **IBIS**



- **Nonlinear parametric relations**

  → Macromodeling via Parametric Identification of Logic Gates, **MπIog**



  - parametric relations approximate any nonlinear dynamic system
  - theory/tools from system identification
  - improved accuracy for recent devices
  - IBIS compliant (ver. 4.1)

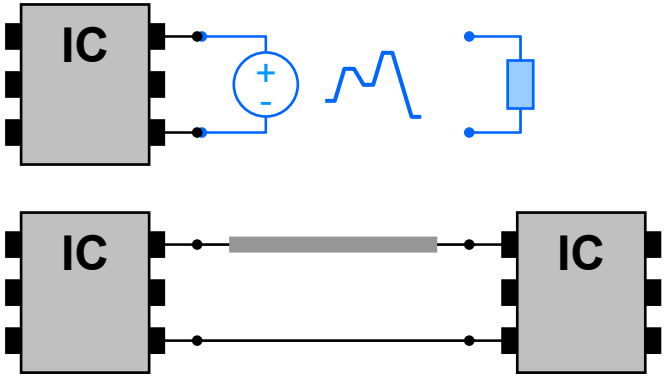
$$i(k) = F(i(k-1),\ldots,v(k), v(k-1),\ldots)$$

Summary of MπLog model generation

(1)

Device is conveniently stimulated and reaction is recorded

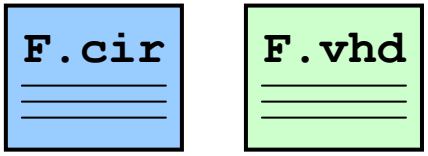
Device mounted directly on the board and responses are recorded



(2) Port responses feed an algorithm for the computation of model parameters

$i(k) = F(i(k-1),\ldots,v(k),v(k-1),\ldots)$

(3) Model equation F is implemented in SPICE or in metalanguages like VHDL-AMS



References

[1] I. S. Stievano, I. A.Maio, F. G. Canavero, C. Siviero, “ParametricMacromodels of Differential Drivers with Pre-Emphasis,” IEEE Transactions on Advanced Packaging. (accepted, in press)

[2] I.S. Stievano, I. A. Maio, F. G. Canavero, “On-the-fly estimation of IC macromodels”, IEE Electronics Letters, Vol. 42, No. 14, pp. 801–803, 6th July 2006.

[3] I. S. Stievano, I. A. Maio, F. G. Canavero, C.Siviero, “Reliable Eye-Diagram Analysis of Data Links via Device Macromodels,” IEEE Transactions on Advanced Packaging, Vol. 29, No. 1, pp. 31–38, Feb. 2006.

[4] I. S. Stievano, I. A. Maio, F. G. Canavero, C.Siviero, “Parametric Macromodels of Differential Drivers and Receivers,” IEEE Transactions on Advanced Packaging, Vol. 28, No. 2, pp. 189–196, May 2005.

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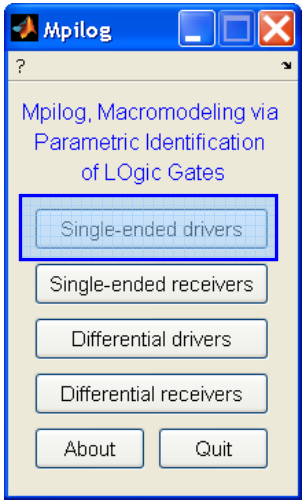
[6] I. S. Stievano, I. A. Maio, F. G. Canavero, “Mπlog Macromodeling via Parametric Identification of Logic Gates,” IEEE Transactions on Advanced Packaging, Vol. 27, No. 1, pp. 15–23, Feb. 2004.

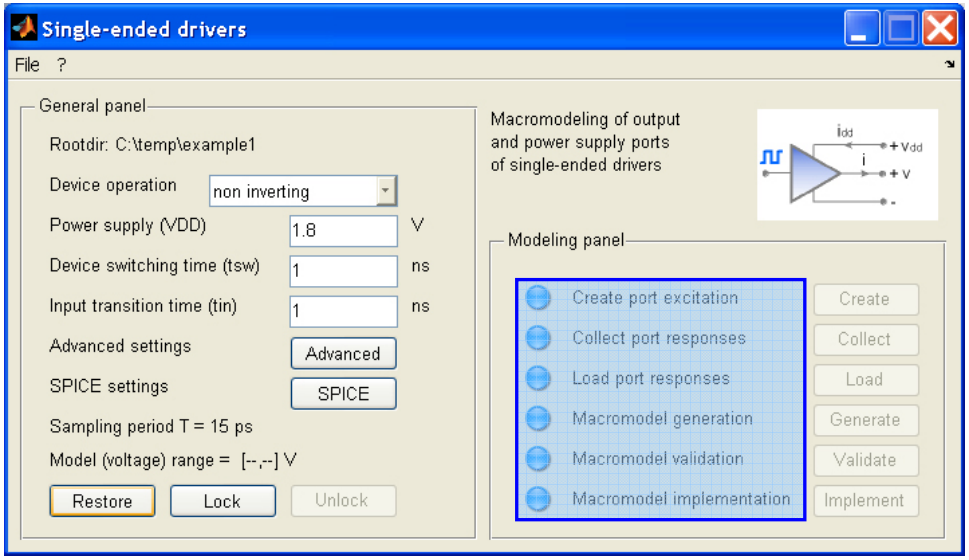
[6] I. S. Stievano, I. A. Maio, F. G. Canavero, “Behavioral Models of I/O Ports from Measured Transient Waveforms,” IEEE Transactions on Instrumentation and Measurement, Vol. 51, No. 6, pp. 1266–1270, Dec. 2002.

[7] I. S. Stievano, I. A.Maio, F. G. Canavero, “ParametricMacromodels of Digital I/O Ports,” IEEE Transactions on Advanced Packaging, Vol. 25, No. 2, pp. 255–264, May 2002.

MπIog© tool

Updated on Mar. 2007 !

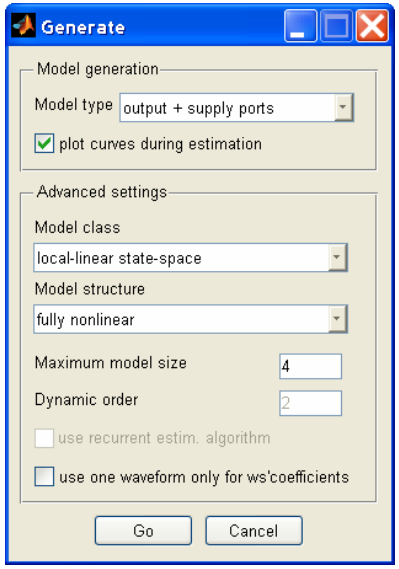




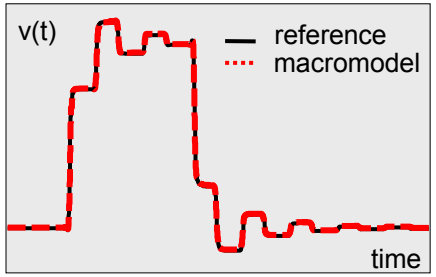
(1) Create port excitations

(2,3) Run SPICE to collect port responses

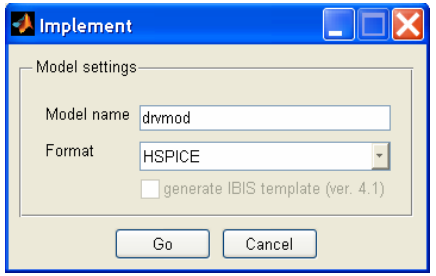
(4) Generate the model



(5) Validate the model



(6) Exctract SPICE circuit, AMS code,...



Outline

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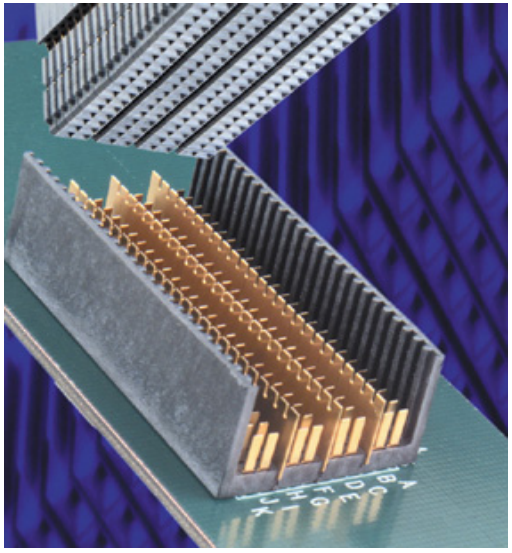
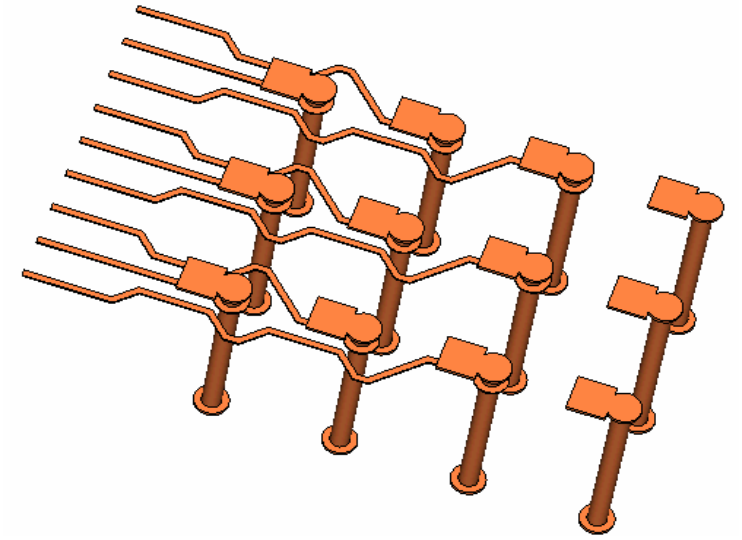
Models for system-level characterization



Connectors



Via fields

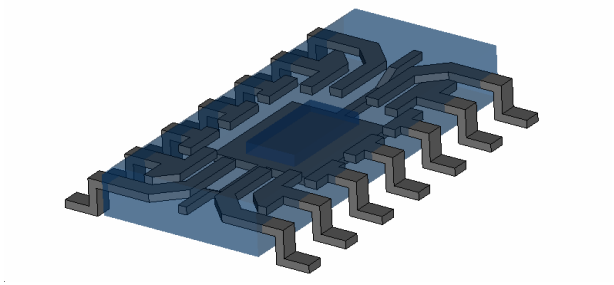
Lumped models (passive RLC networks)

Broadband and SPICE-ready

IdEM©

Identification of Electrical Macromodels

The Approach



EM simulation

Measurement

$$\begin{cases} \mathbf{H}(j\omega) & \text{f}-\text{domain} \\ \mathbf{y}(t) & \text{t}-\text{domain} \end{cases}$$

Rational Approximation

$$\mathbf{Y}(s) = \mathbf{H}(s)\mathbf{X}(s)$$

$$\mathbf{H}(s) = \mathbf{H}_\infty + \sum_n \frac{\mathbf{R}_n}{s - p_n}$$

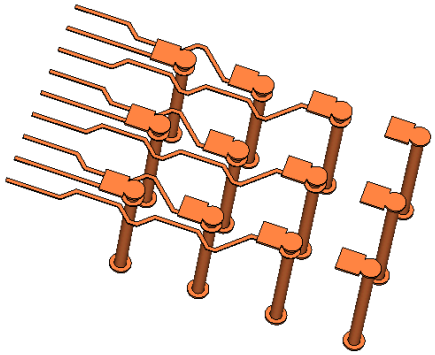
Realization

Passivity Enforcement

$$\begin{cases} \dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\,\mathbf{u} \\ \mathbf{y} = \mathbf{C}\mathbf{x} + \mathbf{D}\,\mathbf{u} \end{cases}$$

Macromodel

IdEM© Tool



IdEM Control Center
Workspace
Setup
New / clear
Load
Data
Import
Operations
Visualization
Export current
Macromodel
Import
Build model
Check accuracy
Export current
Passivity-sweep
Check Data
Check Model
Passivity-Hamiltonian
Check Model
DUM Graphical Display
Click matrix elements for plot
(non-reciprocal)
One figure
Time
Source
Frequency
Mag/Phas
Real/Imag
Stretch colormap
RMS norm
0
0.002*Max
Close all
Exit
Model Options
Current dataset: 'Connector'
Model name:
Connector_Model
Algorithm Selection
Frequency-Domain
FDVF
Block FDVF
Time-Domain
TDVF
Block TDVF
Block TDVF (iterative)
Control Parameters
Bandwidth (Hz):
6e9
Minimum Order
2
Increment:
2
Maximum Order:
12
Stop Accuracy:
1e-03
Advanced...
Generate model
Help
Cancel

IdEM© features

Fully-featured **Graphical User Interface**

Windows and **Linux** platforms

Easy to use and **Customizable**

Accurate and **Efficient**

Handles many ports via splitting strategies

Passivity guaranteed

Data import and **Model export**

References

[1] F. G. Canavero, S. Grivet-Talocia, I. A. Maio, I. S. Stievano, "Linear and Nonlinear Macromodels for System-Level Signal Integrity and EMC Assessment" , IEICE Transactions on Communications - Special Issue on EMC, pp. Vol. E88-B, No. 8, August, 2005.

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[3] S. Grivet-Talocia, "The Time-Domain Vector Fitting Algorithm for Linear Macromodeling" , Int. Journal of Electronics and Communications (AEU), pp. 293-295, vol. 58, 2004.

[4] S. Grivet-Talocia, M. Bandinu, "Improving the Convergence of Vector Fitting for Equivalent Circuit Extraction From Noisy Frequency Responses" , IEEE Transactions on Electromagnetic Compatibility, vol. 48, issue n. 1, pp. 104-120, February, 2006.

MπIog & IdEM

- **Free** trial version of the tools at http://www.emc.polito.it
- Extensive tool **demonstration**

DATE 2007 - UNIVERSITY BOOTH

Thursday, April 19th, 15:15 - 17:00 pm

Section U9: DFM + Test and Yield Solutions