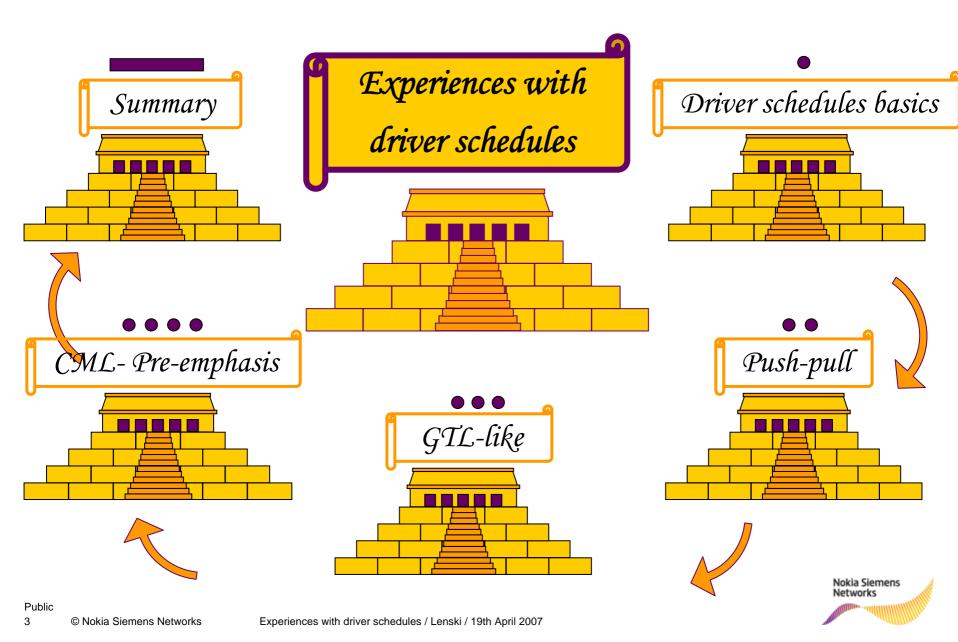


Experiences with driver schedules Eckhard Lenski DATE , Nice , France 19th April 2007



Agenda

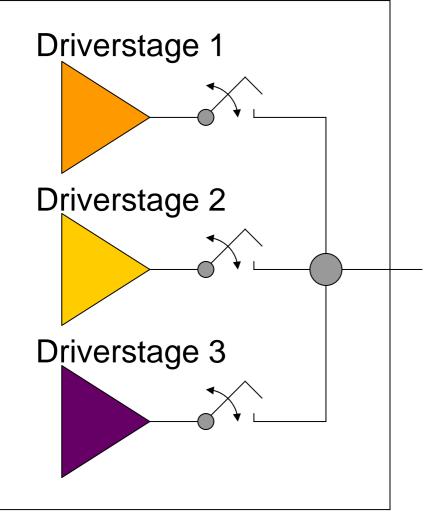




Driver schedule basics...



Multistage driver



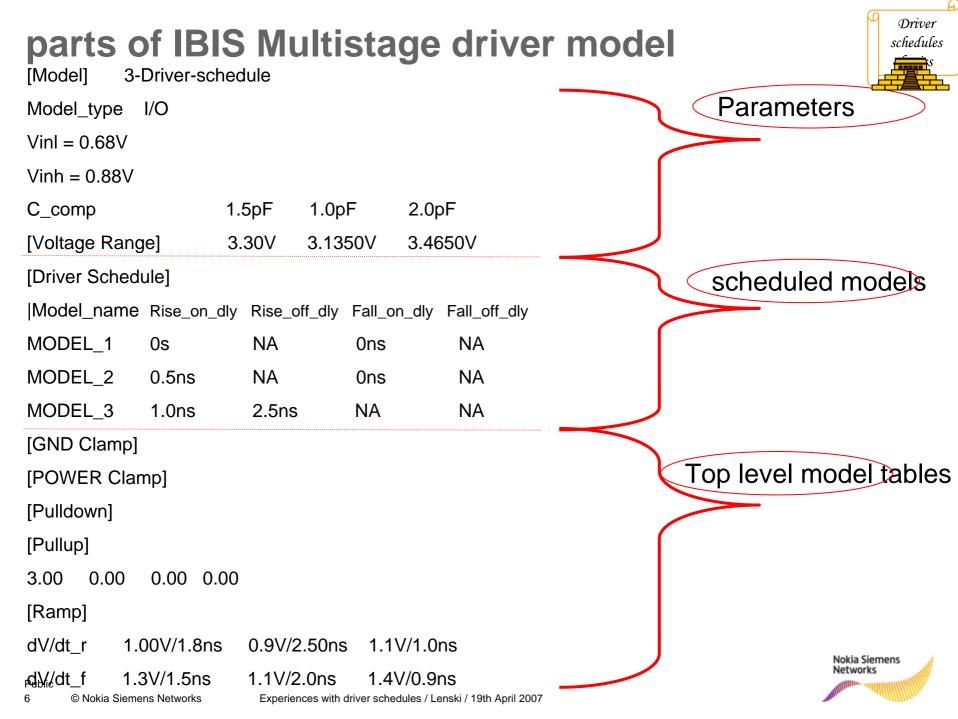
OUTPUT



A Multistage driver consists of several driverstages, which are switching at different times

Or different voltage levels Or





top level model	Driver schedules basics
C_comp	
[Voltage Range] 3.30V	
[GND Clamp]	el model tables
[POWER Clamp]	
[Pulldown]	
[Pullup]	
[Ramp]	
dV/dt_r 1.00V/1.8ns	
dV/dt_f 1.3V/1.5ns	

For tools, which don't understand the [Driver schedule] keyword, there is a description of the rough/approximate behavior of the output with normal IBIS keywords, (called top level model)



scheduled models

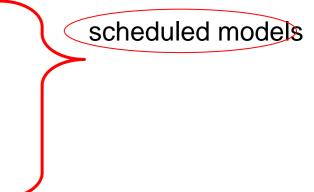
[Model] 3-Driver-schedule

Model_type I/O

[Driver Schedule]

|Model_name Rise_on_dly Rise_off_dly Fall_on_dly Fall_off_dly

MODEL_1	0s	NA	Ons	NA
MODEL_2	0.5ns	NA	Ons	NA
MODEL_3	1.0ns	2.5ns	NA	NA



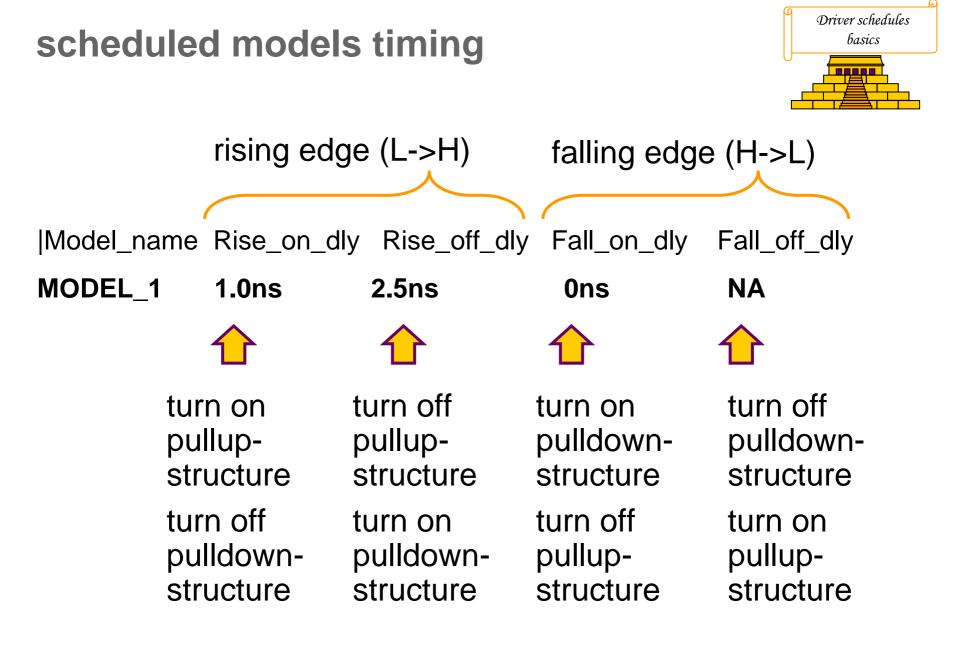
The Driver schedule contains the exact timing information about the time, when the different driverstages are used.

The switching behavior of each driverstage itself is described like that of a normal IBIS IO-model in a [Model] statement



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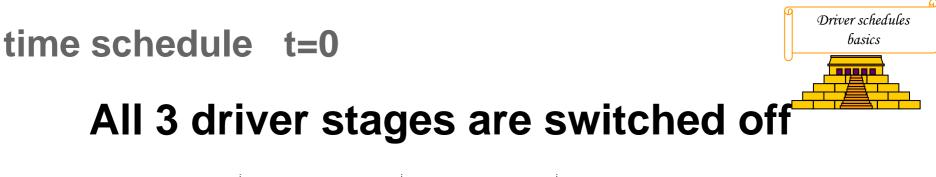
example timing schedule

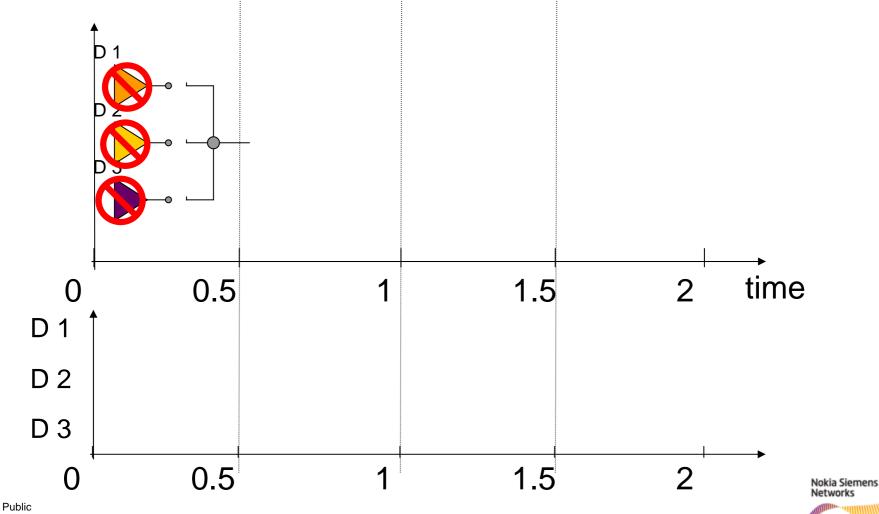


[Driver Schedule]

Model_name	Rise_on_dly	Rise_off_dly	Fall_on_dly	Fall_off_dly
MODEL_1	0.5ns	NA	0ns	NA
MODEL_2	1.0ns	NA	0ns	NA
MODEL_3	1.5ns	2.5ns	NA	NA



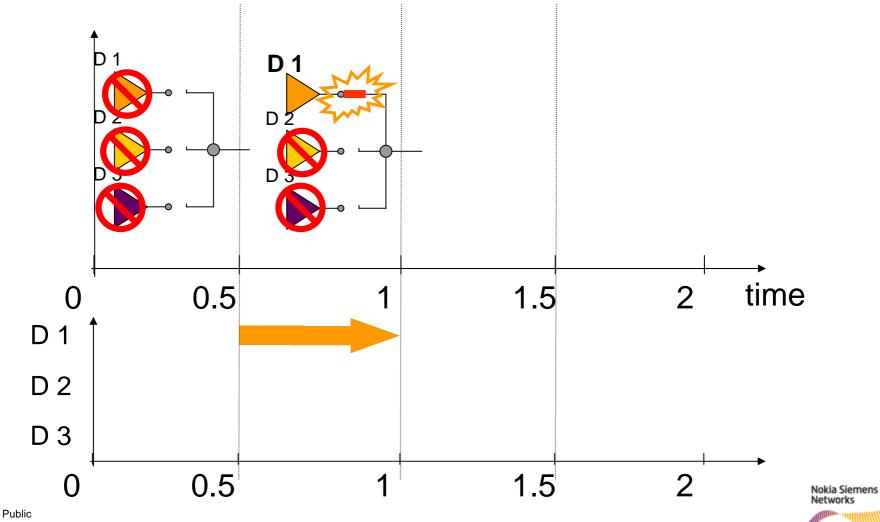








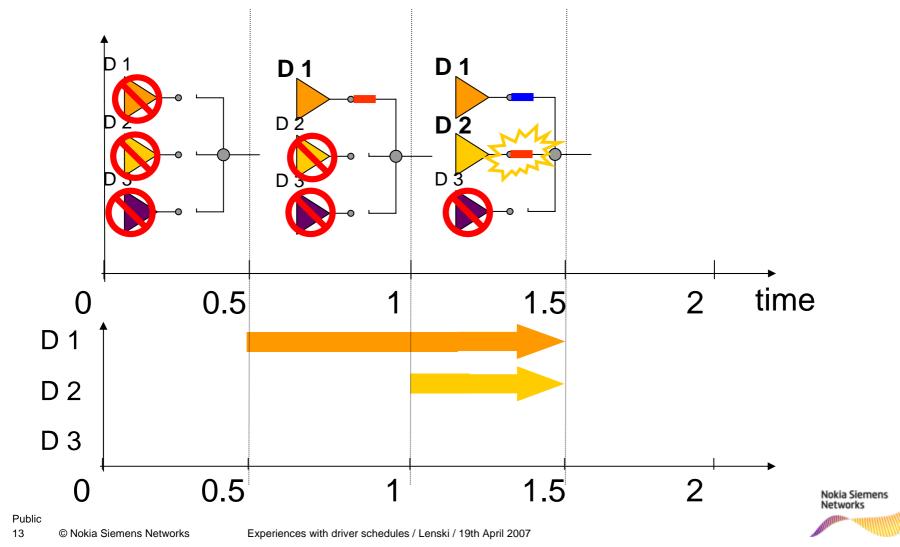
Driver stage D1 is switched on



time schedule t = 1



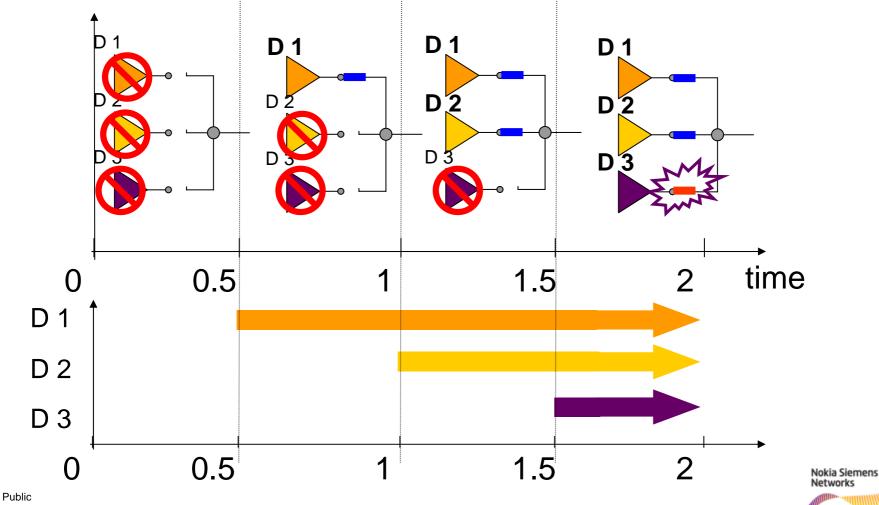
Driver stage D2 is additionally switched on







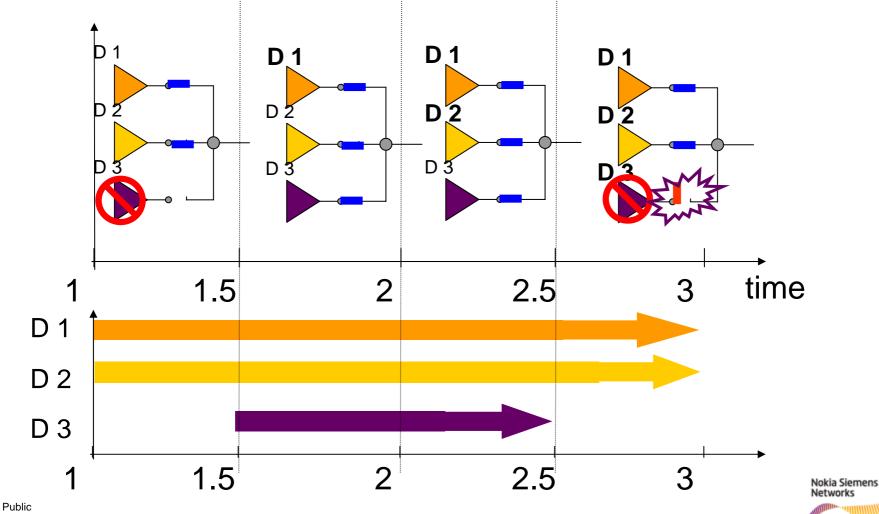
Driver stage D3 is additionally switched on





time schedule t = 2.5

Driver stage D3 is switched off

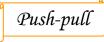


Driver schedules with push-pull (CMOS) Models

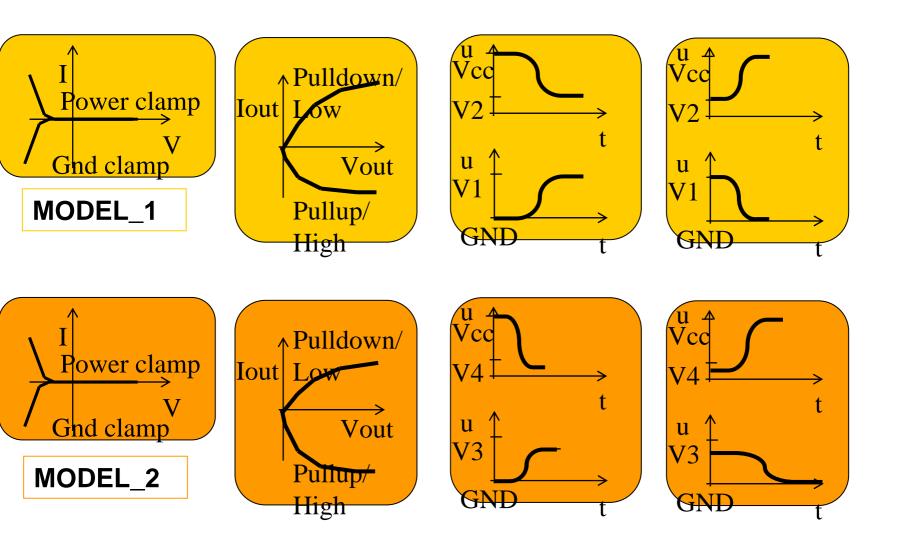




IBIS push pull driver schedule

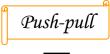








realization



Example with two IO-Models and no top level model information

[Driver schedule]

.

.

|Model_nameRise_on_dlyRise_off_dlyFall_on_dlyFall_off_dlyMODEL_12.00nsNA2.0nsNAMODEL_22.50nsNA2.0nsNA

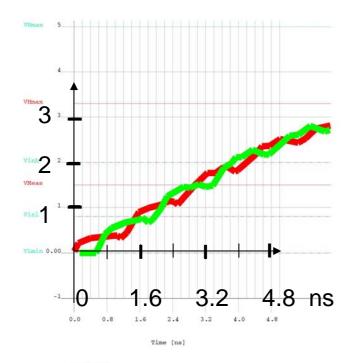


IO-models stand alone

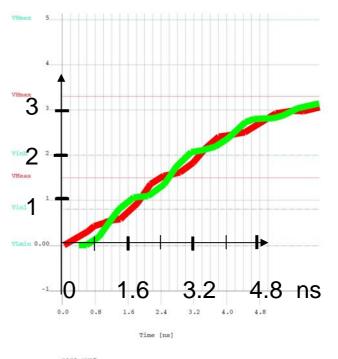




MODEL_1 stand alone



MODEL_2 stand alone

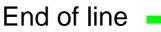


R1E9_GND7 design/U_7P5cmltg_1-1./pinIn= design/UI_1-1./pinInst R1E9_GND7 design/U_7P5cmltg_1-1./pinIns- design/UI_1-1./pinInst

Testload was a 3 inch transmission line (open)

Driver

- E





3 test cases



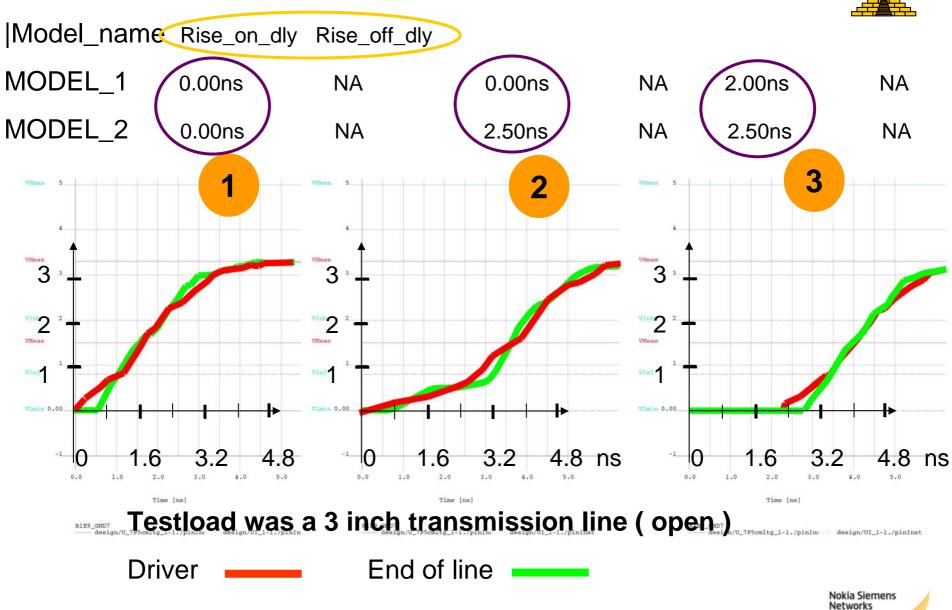
(examples show only rising edge)

[Model_name Rise_on_dly Rise_off_dly Fall_on_dly Fall_off_dlyMODEL_10.00nsNA2.0nsNAMODEL_20.00nsNA2.0nsNA

|Model_name Rise_on_dly Rise_off_dly Fall_on_dly Fall_off_dly

MODEL_1 NA NA 0.00ns 2.0ns 2 MODEL 2 2.50ns NA 2.0ns NA Fall_on_dly Rise_off_dly Fall_off_dly Model_name Rise_on_dly **MODEL 1** NA 2.00ns NA 2.0ns 3 MODEL 2 2.50ns NA 2.0ns NA

results

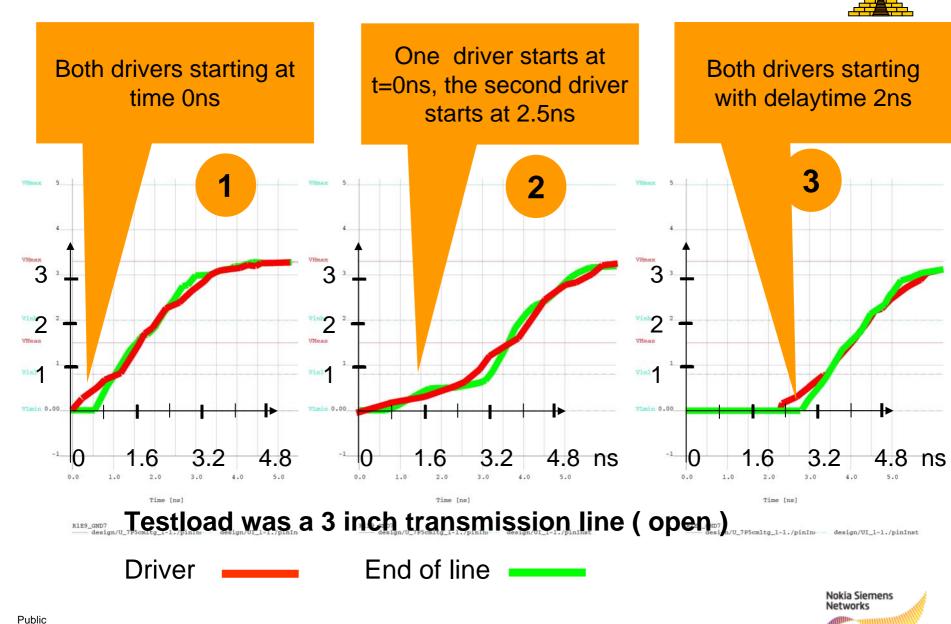


Push-pull

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results with comments

Push-pull



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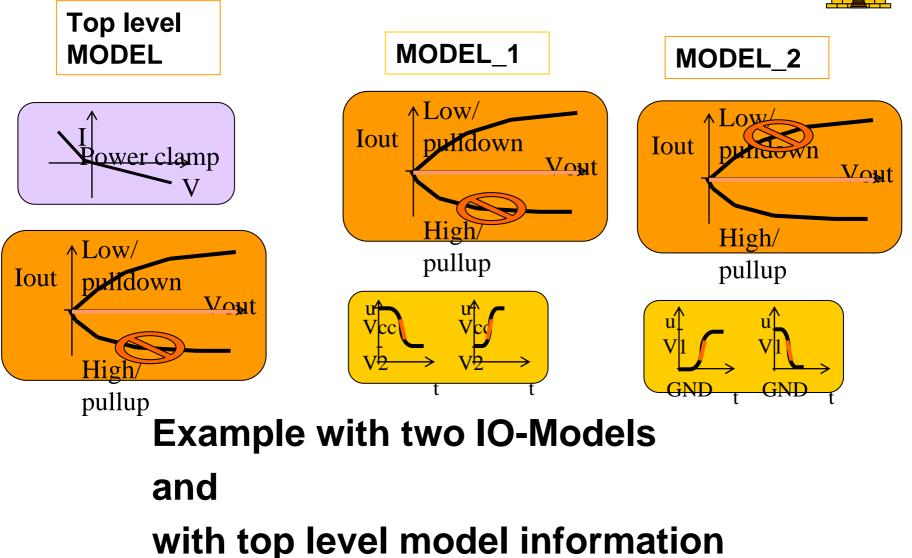
GTL-like driver schedules





IO models





IBIS gtl driver schedule

[Driver schedule]

|Model_name Rise_on_dly Rise_off_dly Fall_on_dly Fall_off_dly

- MODEL_OPSINK 0.00ns NA 2.0ns NA
- MODEL_OPSOURCE 0.00ns 2.0ns NA NA
- [pullup]
- 0.0V 0mA
- [pulldown]
- 0.0V 0mA
- 2.0 35mA
- [powerclamp]
- 0.0V 0mA
- 2.0V -10mA



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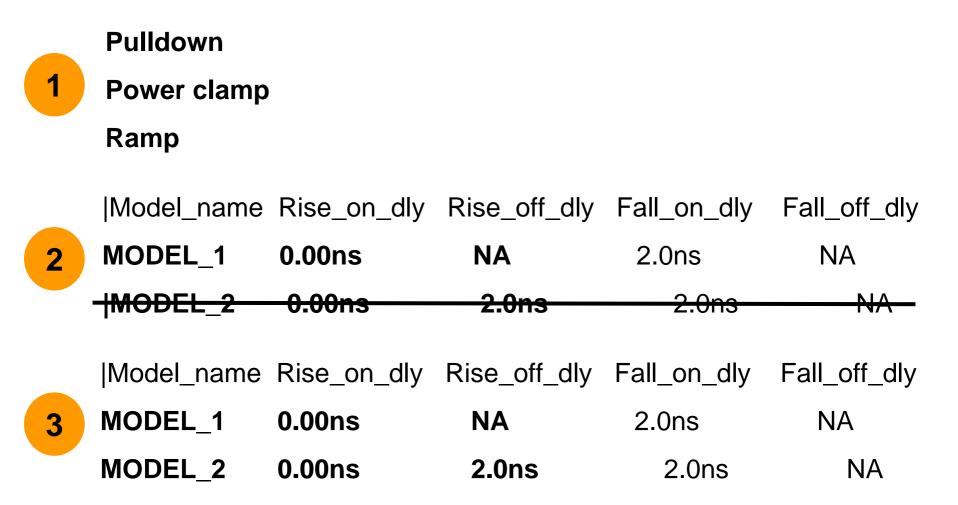
GTL-like

Public 25

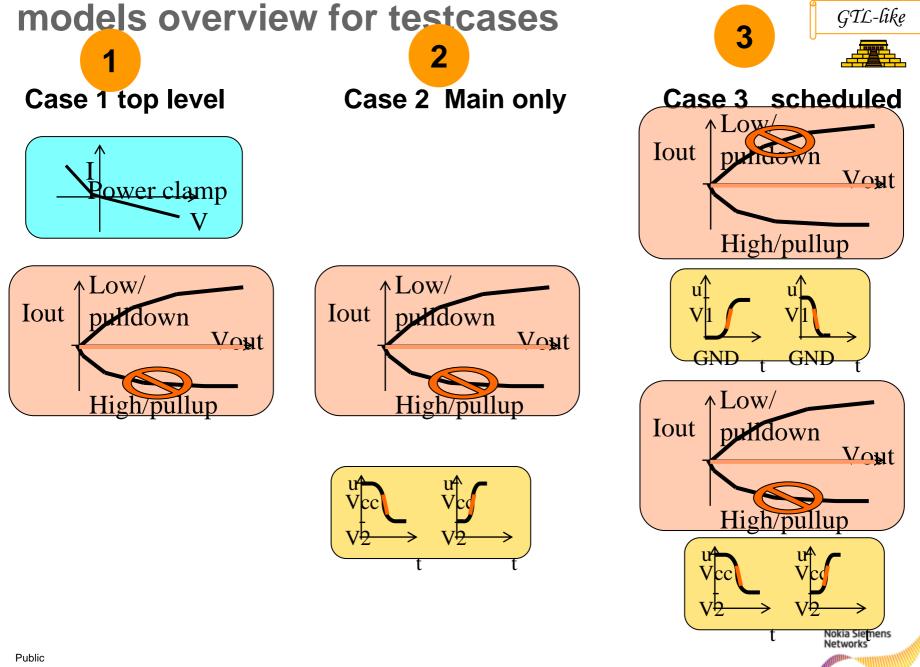
3 test cases



(here only rising edge shown)



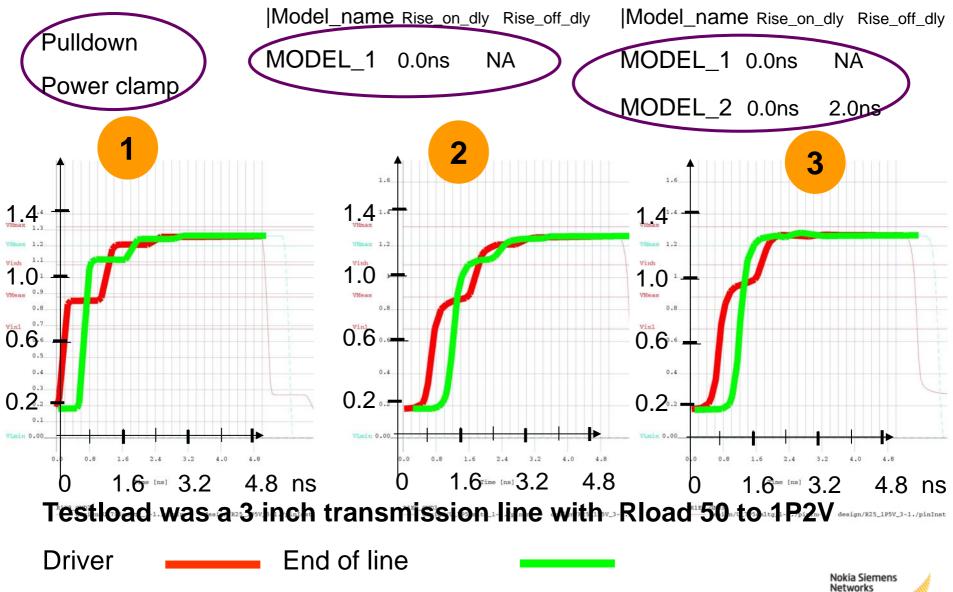




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results

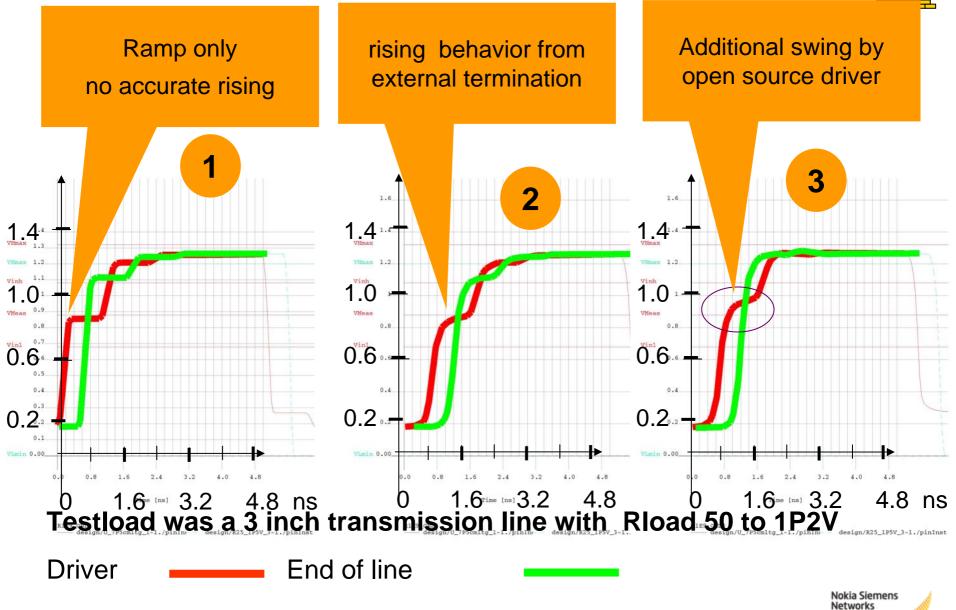




Public

results with comments

GTL-like

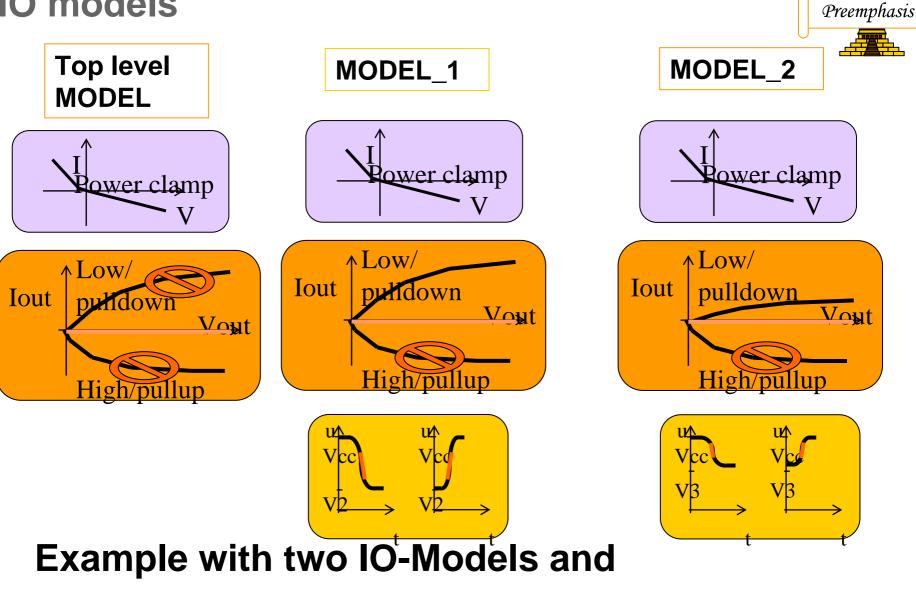


CML pre-emphasis





IO models



with wrong top level model information

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CML-

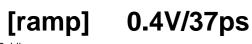
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IBIS cml driver schedule

[Driver schedule]

|Model_name Rise_on_dly Rise_off_dly Fall_on_dly Fall_off_dly

- MODEL_OPSINKMAIN 0.00ns NA 2.0ns NA
- MODEL_OPSINKBOOST 0.00ns 0.8ns NA NA
- [pullup]
- 0.0V 0mA
- [pulldown]
- 0.0V 0mA
- 2.0V 0mA
- [powerclamp]
- 0.0V 0mA
- 2.0V -10mA



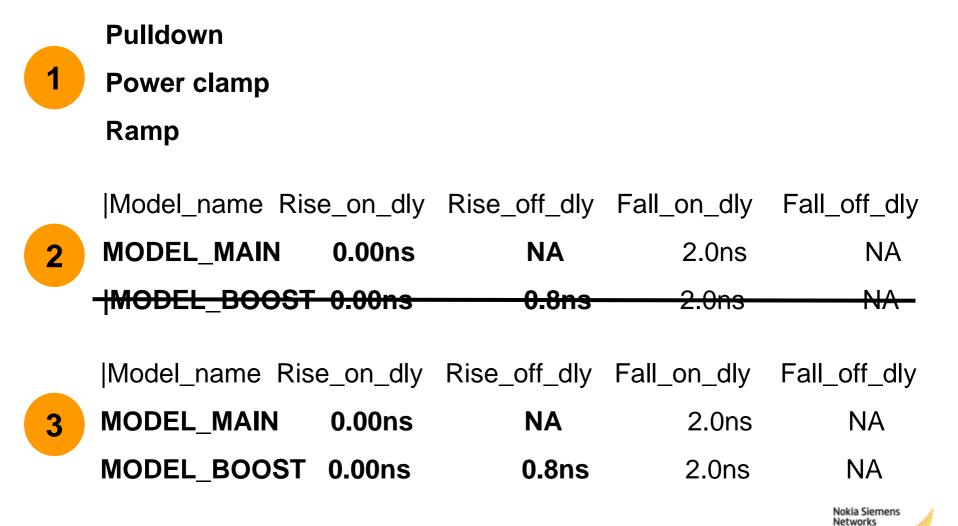






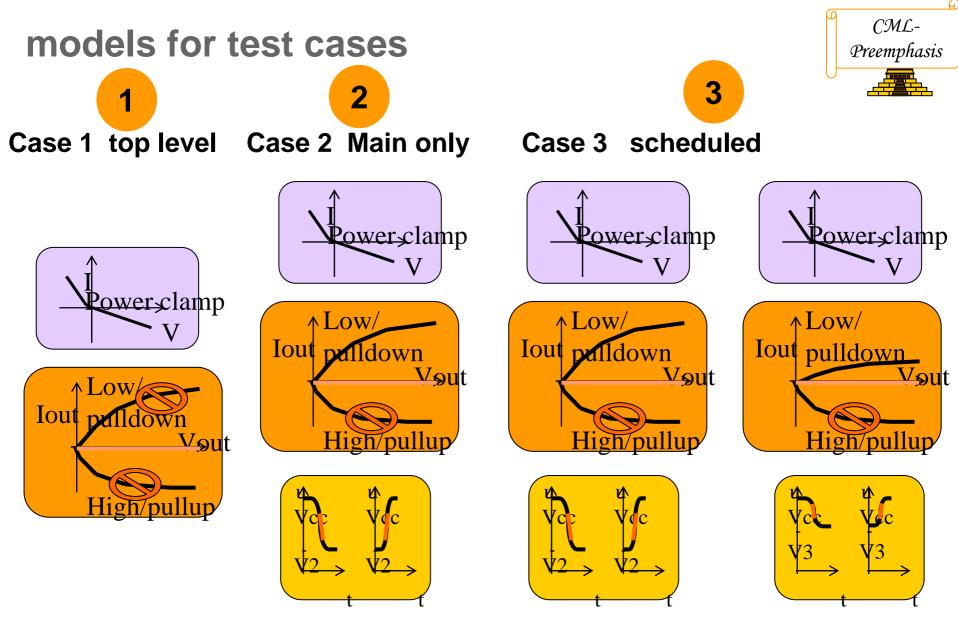


(here only rising edge shown)

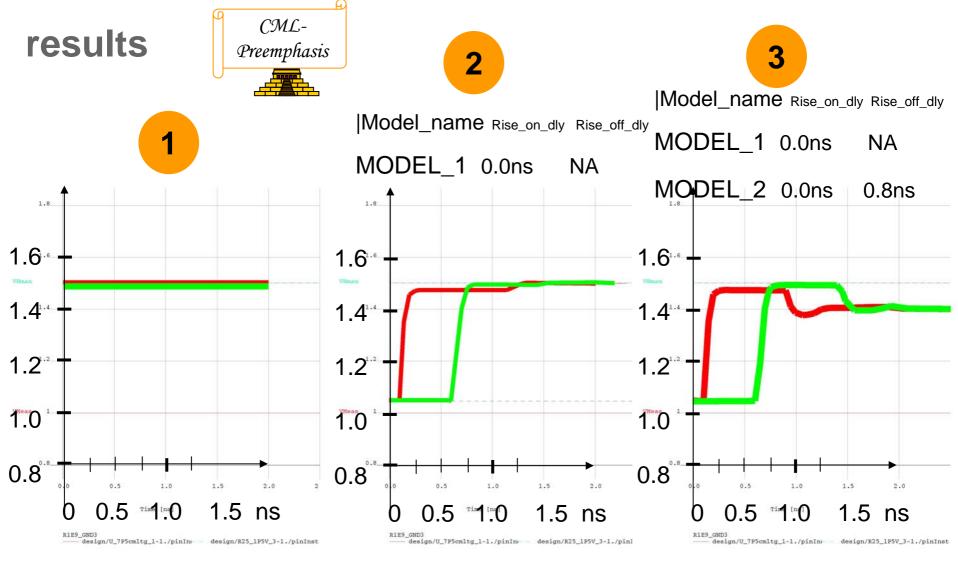




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Testload was a 3 inch transmission line with Rload 50 to 1P5V

Driver End of line

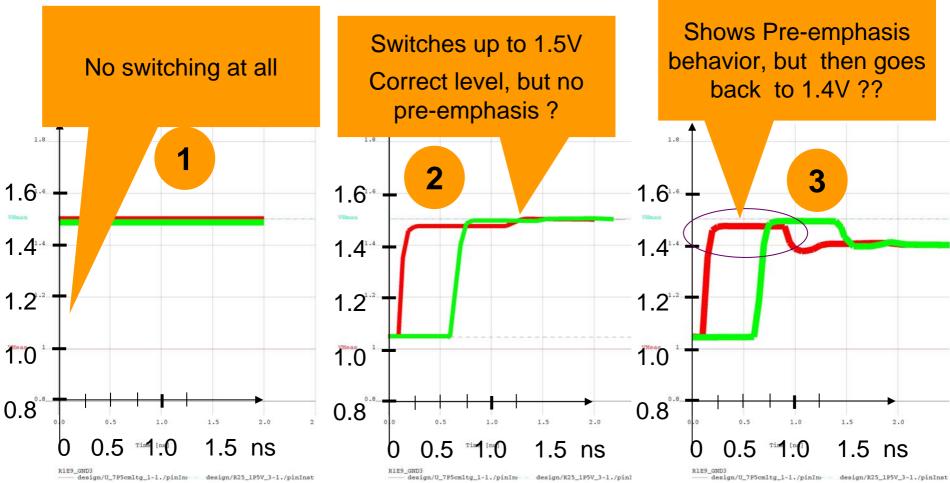


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CML- Preemphasis



Testload was a 3 inch transmission line with Rload 50 to 1P5V

Driver End of line



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Summary

Timing dependant drivers works fine

 Voltage dependant drivers should be possible with [submodel] and ,fall-back'

- Pre-emphasis modeling is possible, but only with fixed ,Pre-emphasis'
- Pattern dependant ,Pre-emphasis' with VHDL-AMS
- Check of combined static and dynamic waveforms necessary
- Driver schedule models have to be carefully checked





Thank You

•Questions ?