Gate Modulation Solution Validated by VHDL-AMS IBIS Implementation

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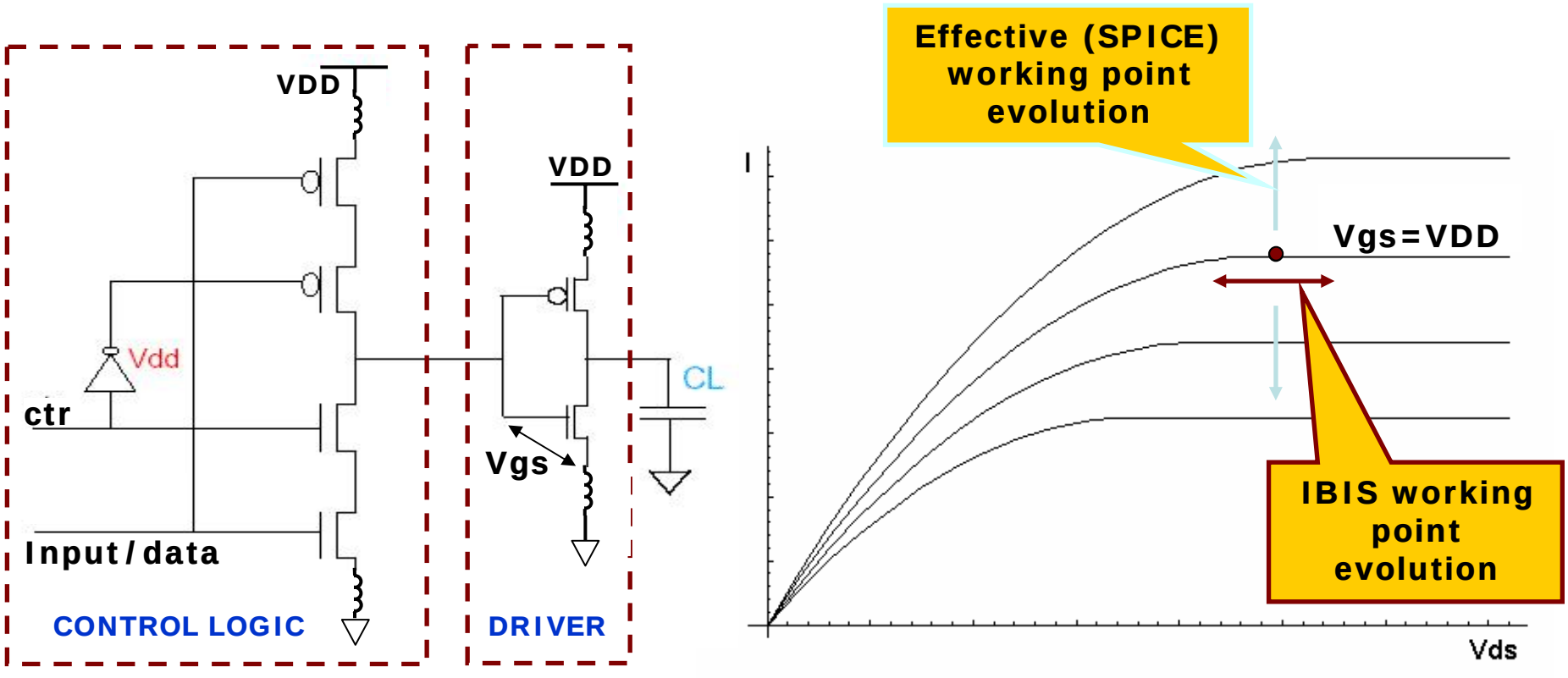
Agenda

- IBIS “Gate Modulation” solution: ST Proposal overview
- Implementation and Validation by the VHDL-AMS IBIS architecture
- BIRD98 & ST proposal convergence
- Conclusions

IBIS Gate Modulation Criticality

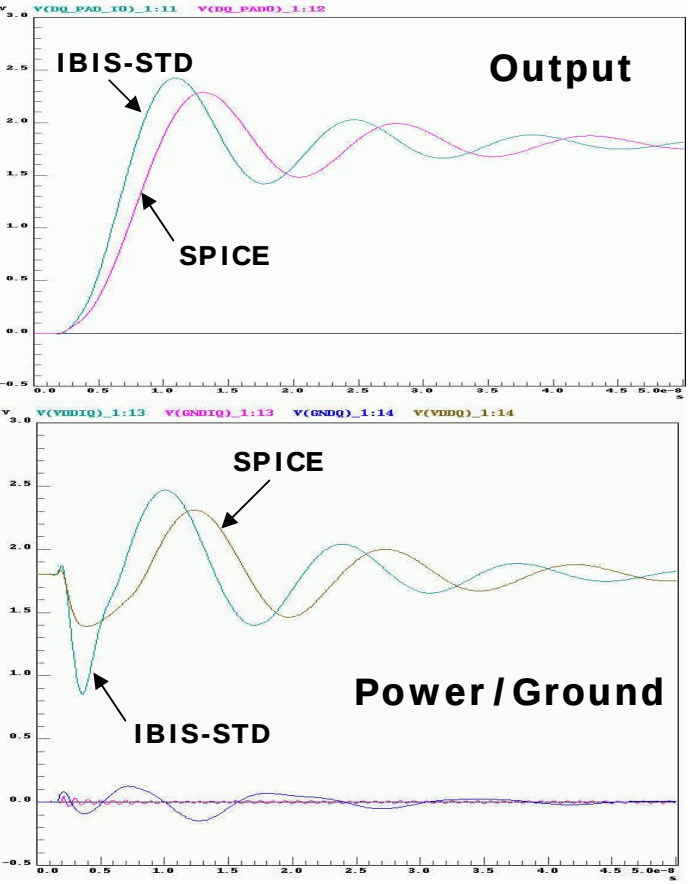


The IBIS simulation of a simultaneous switching noise does not model correctly the MOS Vgs voltage variation because the working point can move only along the same Vgs =VDD characteristic.

The higher is the bouncing noise, the higher is the mismatching between IBIS and Spice results

Benchmark SPICE vs IBIS Standard (IBIS-STD)

SSO – Rise Transition



Relative Percentage Error

Max Delay

22 %

Max overshoot/undershoot

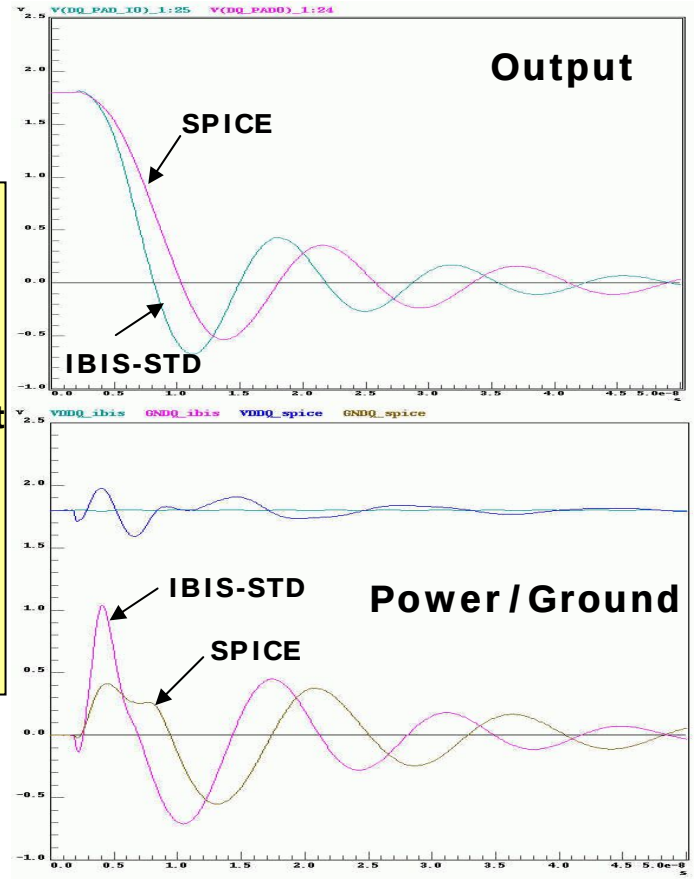
25 %

Diff. Power supply

32 %

Test-case: 128M Nor Flash Memory (120nm)

SSO – Fall Transition



Initial case of study: Simultaneous Switching Output (SSO) simulations by IBIS standard (IBIS-STD), compared with the related SPICE ones, have revealed strong discrepancies.

Initially, no equivalent load/impedance has been considered on the power and ground nodes of IBIS models.

Gate Modulation Coefficients

The ST "Gate Modulation" solution is based on the introduction of two coefficients, one for the Pullup and one for the Pulldown stage, which modulate properly the IBIS standard current (I_IBIS-STD) when a bouncing noise occurs on the power and ground nodes

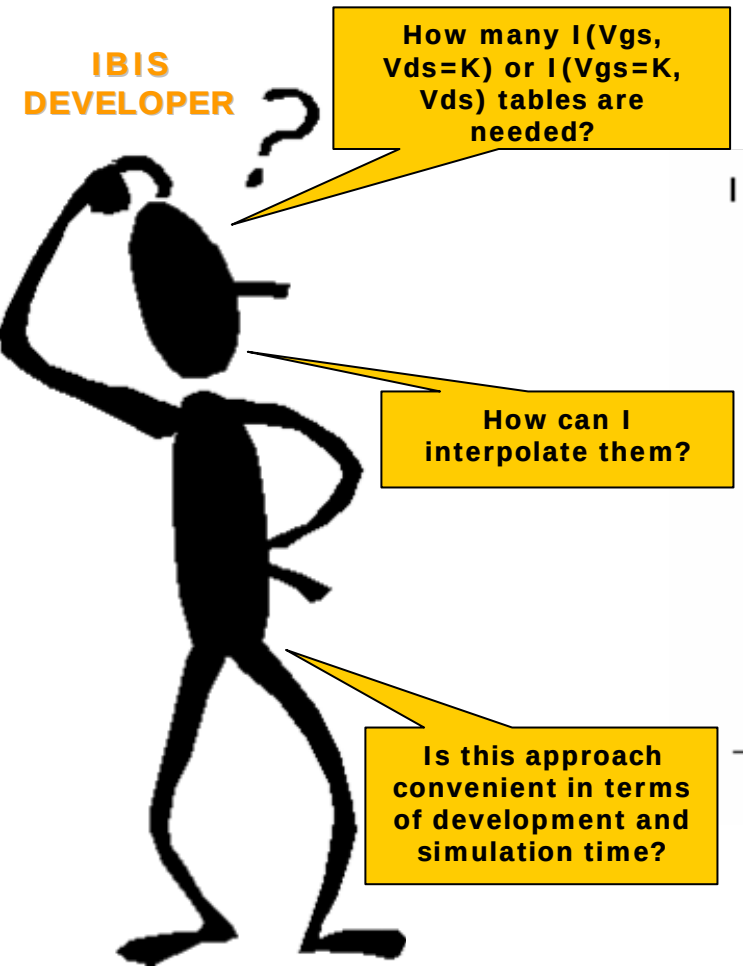
$$\underbrace{I(Vgs, Vds)}_{\text{Effective SPICE current}} = Kssn(Vgs,Vds) * \underbrace{I(Vgs=VDD,Vds)}_{\text{IBIS standard current}}$$

I_effective = Kssn(Vgs,Vds)*I_IBIS-STD

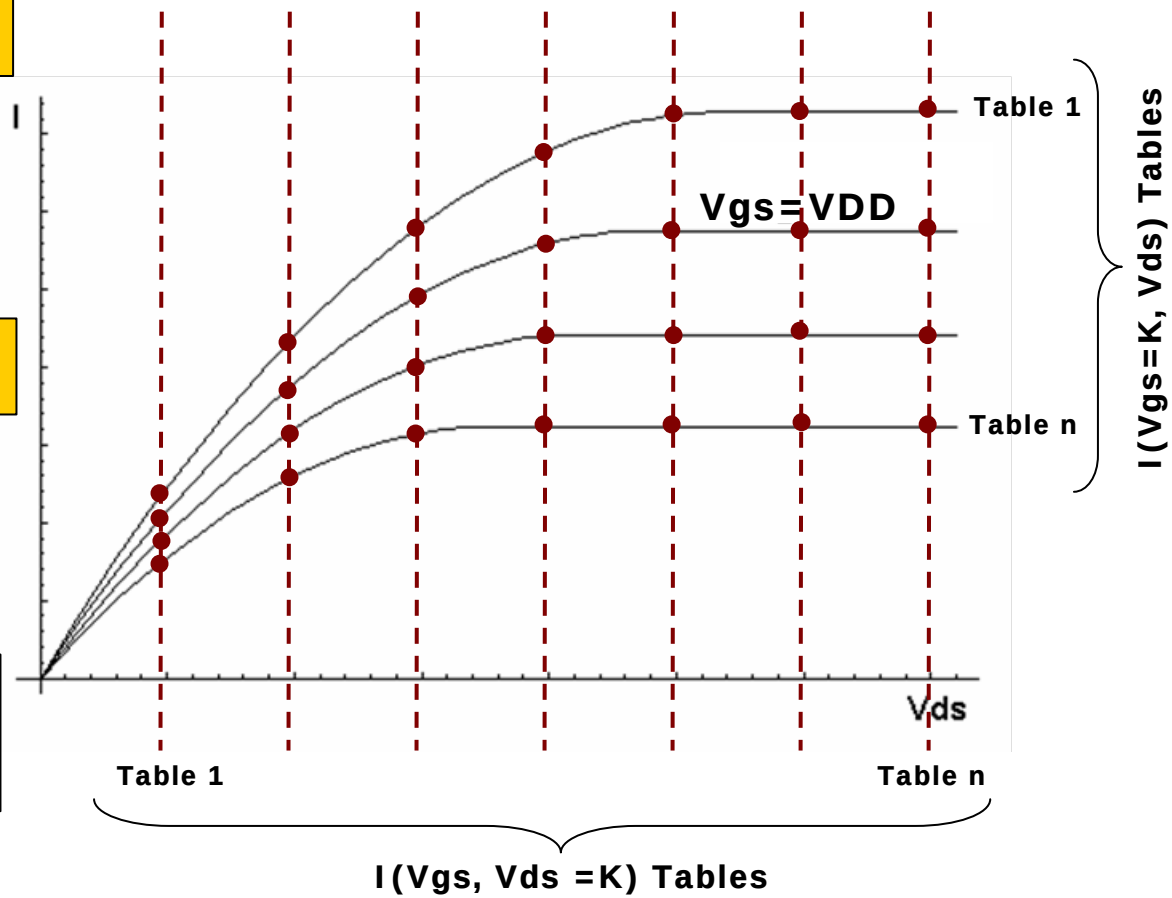
$$k_{ssn-pulldown} = \frac{I(v_{gs},vds)}{I(v_{gs}=vdd,vds)}$$

$$k_{ssn-pullup} = \frac{I(v_{sg},vsd)}{I(v_{sg}=vdd,vsd)}$$

Kssn(Vgs, Vds) Implementation by Table-format

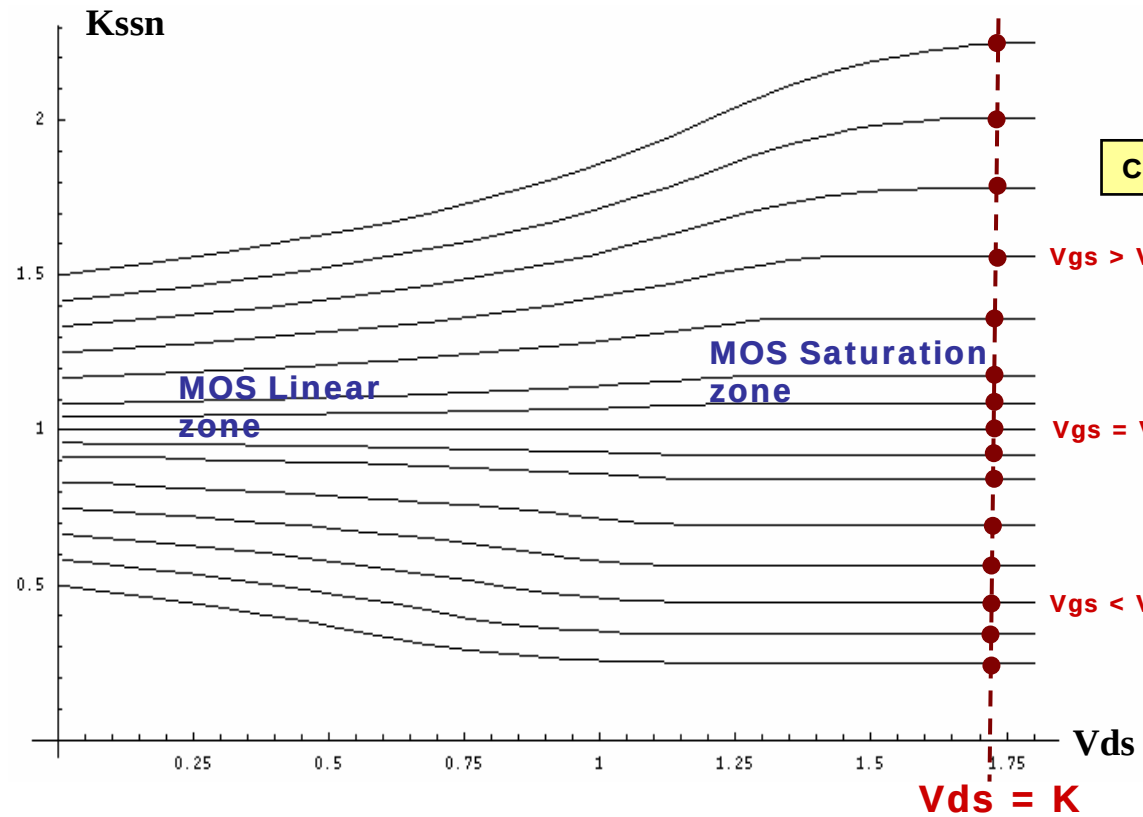


Note: K means constant value!!!



The effort has been focused on identifying a table-format implementation of Kssn coefficients, which could also be the best trade-off between accuracy and development/simulation time

Gate Modulation Coefficient Characteristics



Corrective behaviour of the Kssn coefficient

Vgs > VDD ⇒ Kssn > 1 ⇒ Ieffective > I_IBIS-STD

Vgs = VDD ⇒ Kssn = 1 ⇒ Ieffective = I_IBIS-STD

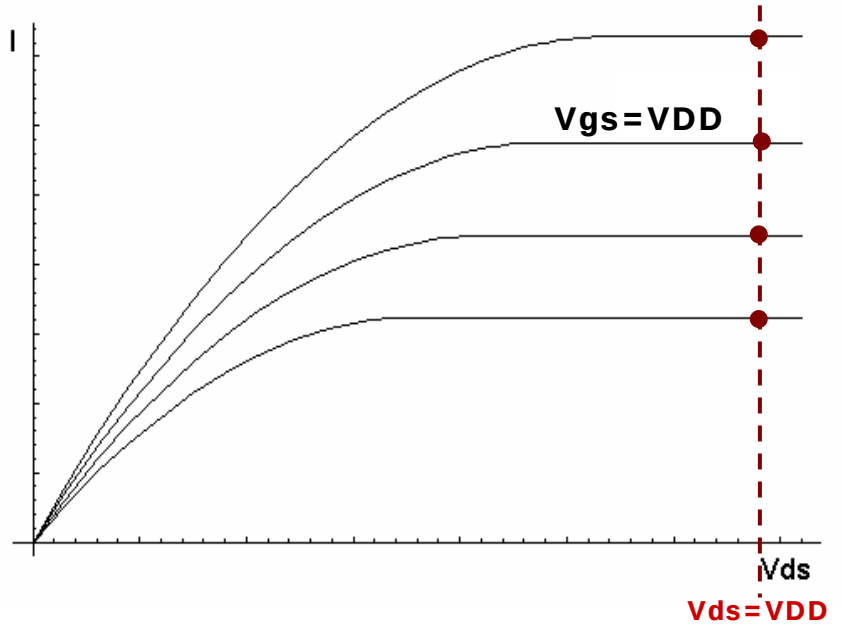
Vgs < VDD ⇒ Kssn < 1 ⇒ Ieffective < I_IBIS-STD

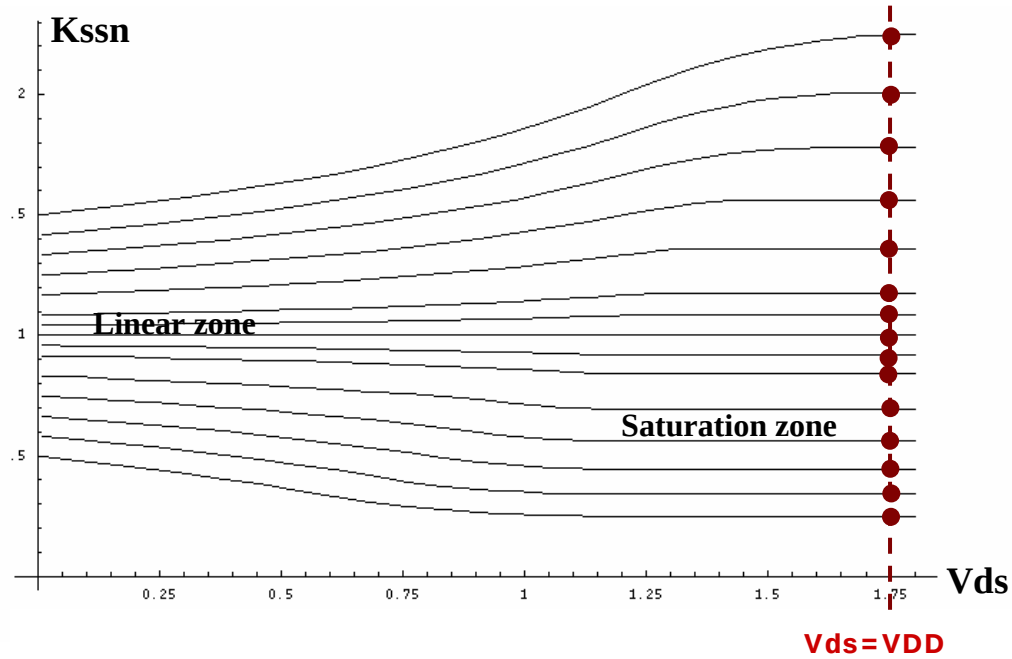
The Kssn coefficient is independent from the Vds voltage in the saturation zone and, approximatively, also in the linear zone, in the case of small Vgs changes.

It implies that one table Kssn(Vgs, Vds=K), with K in the saturation zone, can be enough for Pullup and Pulldown, respectively.

Therefore, a Two-Table approach may be a good compromise accuracy-complexity.

Two-Tables Solution





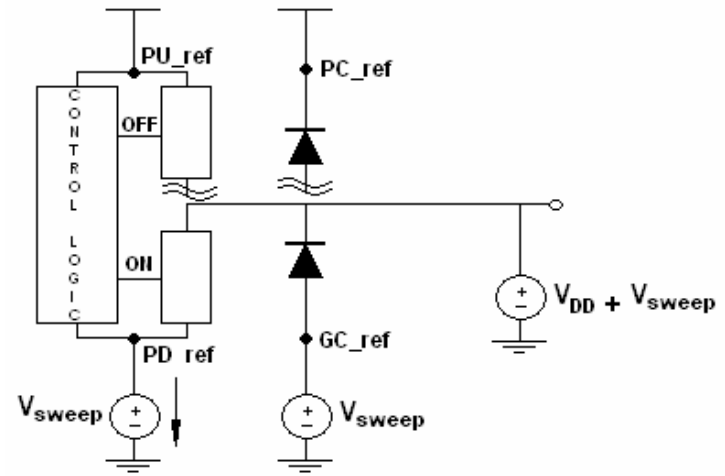
- K has been chosen equal to VDD (best choice if the MOS channel modulation effect is negligible)
- Kssn(Vgs, Vds=VDD) implies that the effective current to be drawn is

$$I\_effective\_pulldown = I(Vgs, Vds=VDD)$$

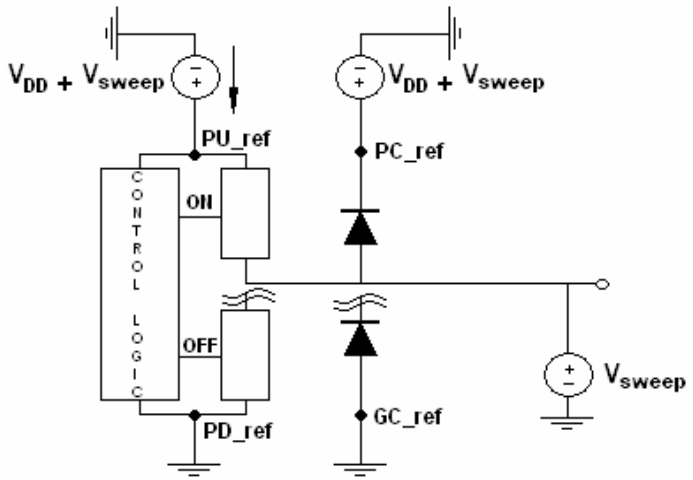
$$I\_effective\_pullup = I(Vsg, Vsd=VDD)$$

Effective Currents Extraction

Pulldown I(Vgs, Vds=VDD) table extraction



Pullup I(Vgs, Vds=VDD) table extraction



Vsweep=[-VDD, VDD]; Vgate is kept stable --→ the collected effective current is related to the source voltage (Vs) changes

VHDL-AMS

I(Vgs, Vds=VDD) Table

I(Vsg, Vsd=VDD) Table

→ **Kssn_pulldown** **Kssn_pullup** →

I_effective =Kssn*I_IBIS-STD

Since it is not possible to change the proprietary code of EDA tools that manage the IBIS models, the unique way identified for implementing and validating the solution has been to use the VHDL-AMS IBIS architecture, adding the Gate modulation coefficients algorithm.

Extension of the VHDL-AMS IBIS Implementation

VHDL-AMS IBIS

Traditional IBIS (Muranyi)

```
entity IBIS_IO is generic (C_comp : real := 4.55e-12;
……
 [Pullup Reference] and [Pulldown Reference] values
V_pu_ref : real := 5.0; V_pd_ref : real := 0.0;
Vectors of the IV curve tables
I_pc : real_vector := ( 0.08, 0.00, 0.00, 0.00);
……..
if (Extrapolation = "IV") and (X <= Xdata(0)) then m :=
(Ydata(1) - Ydata(0)) / (Xdata(1) - Xdata(0)); yvalue :=
Ydata(0) + m * (X - Xdata(0));
return yvalue;
……
```

I-V tables: Pullup&Power_clamp

V-t tables: Rising & Falling waveform

Ramp values: dV/dt_r; dV/dt_f

C_comp values

+

Gate Modulation Algorithm

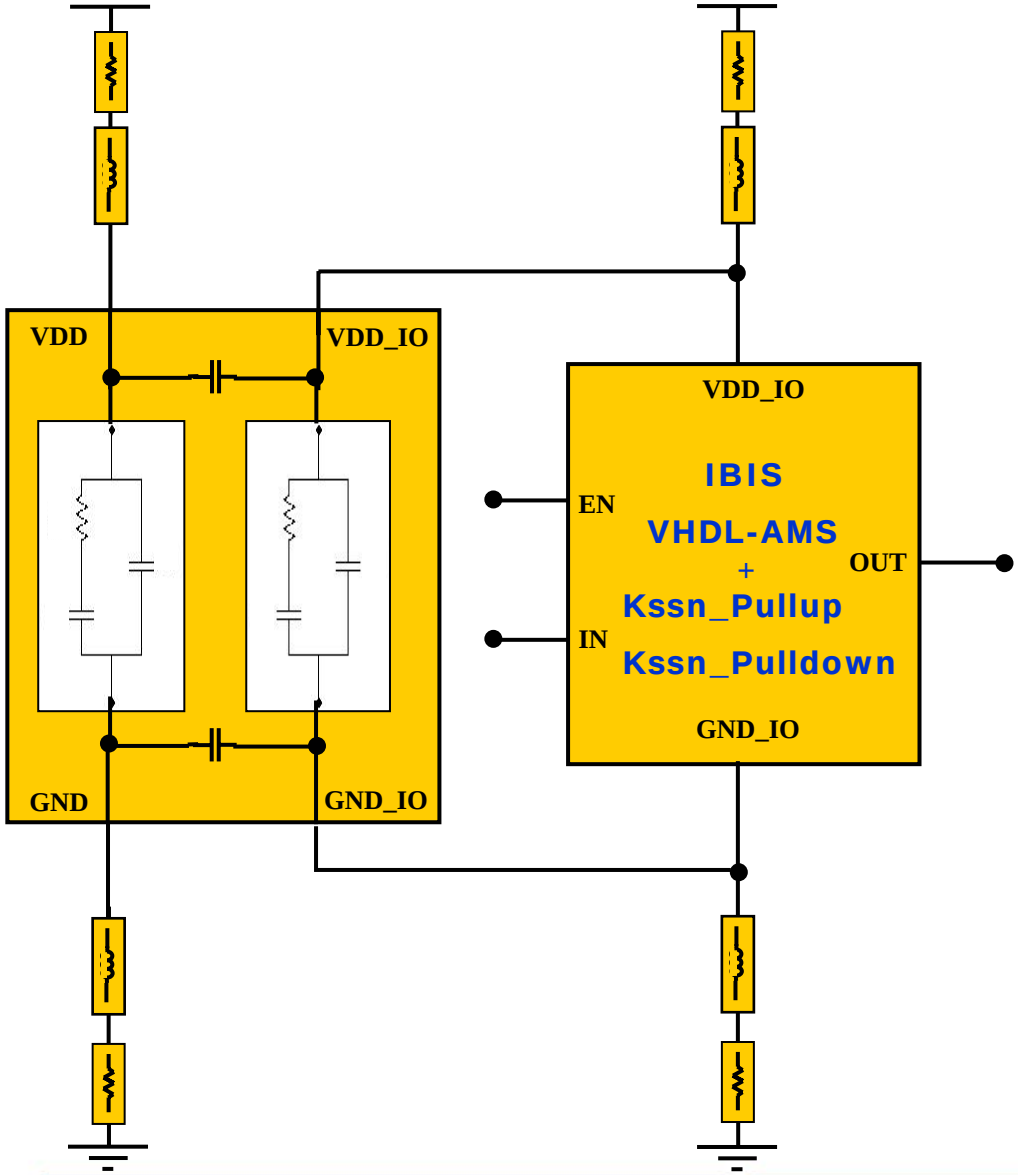
Kssn-pulldown & Kssn-pullup

I_effective = Kssn*I_IBIS-STD

I(Vgs,Vds=VDD)Pulldown table

I(Vsg,Vsd=VDD) Pullup table

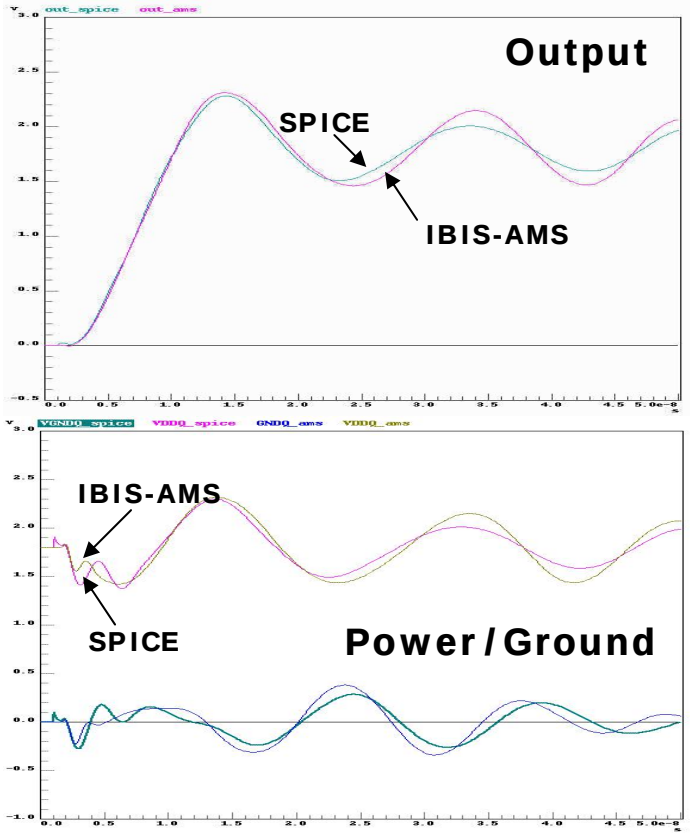
Implementation and Validation Strategy



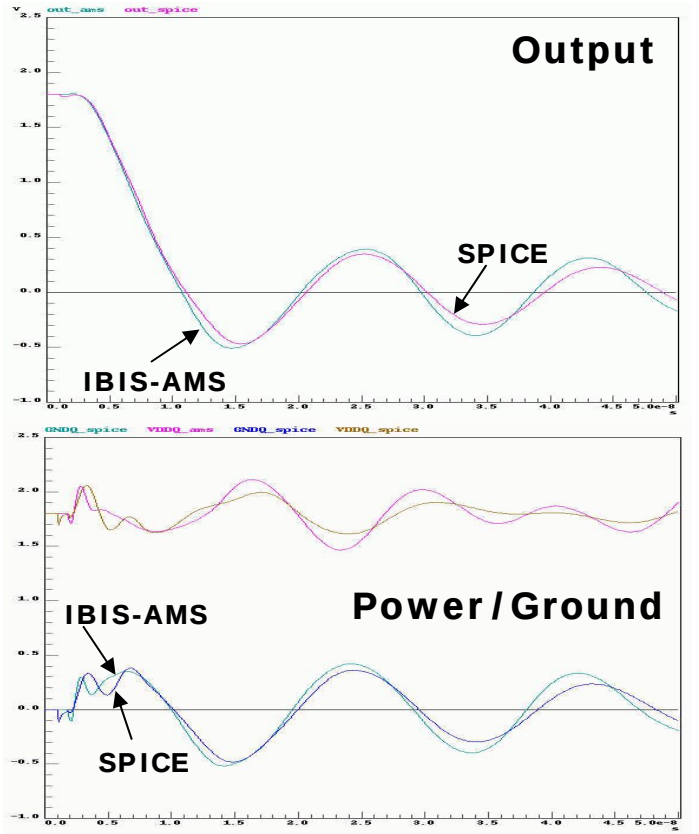
- NOR Flash memories test-cases
- SSO simulations have been carried out
- The VHDL-AMS IBIS implementation (IBIS-AMS) has been used
- The "Gate modulation" algorithm has been added to the VHDL-AMS IBIS initial code
- Equivalent impedance of power rails is also been considered

Benchmark SPICE vs IBIS-AMS

SSO – Rise Transition



SSO – Fall Transition



Relative Percentage Error

Max Delay

3 % (22 % IBIS-STD)

Max overshoot/undershoot

8 % (25 % IBIS-STD)

Diff. Power supply

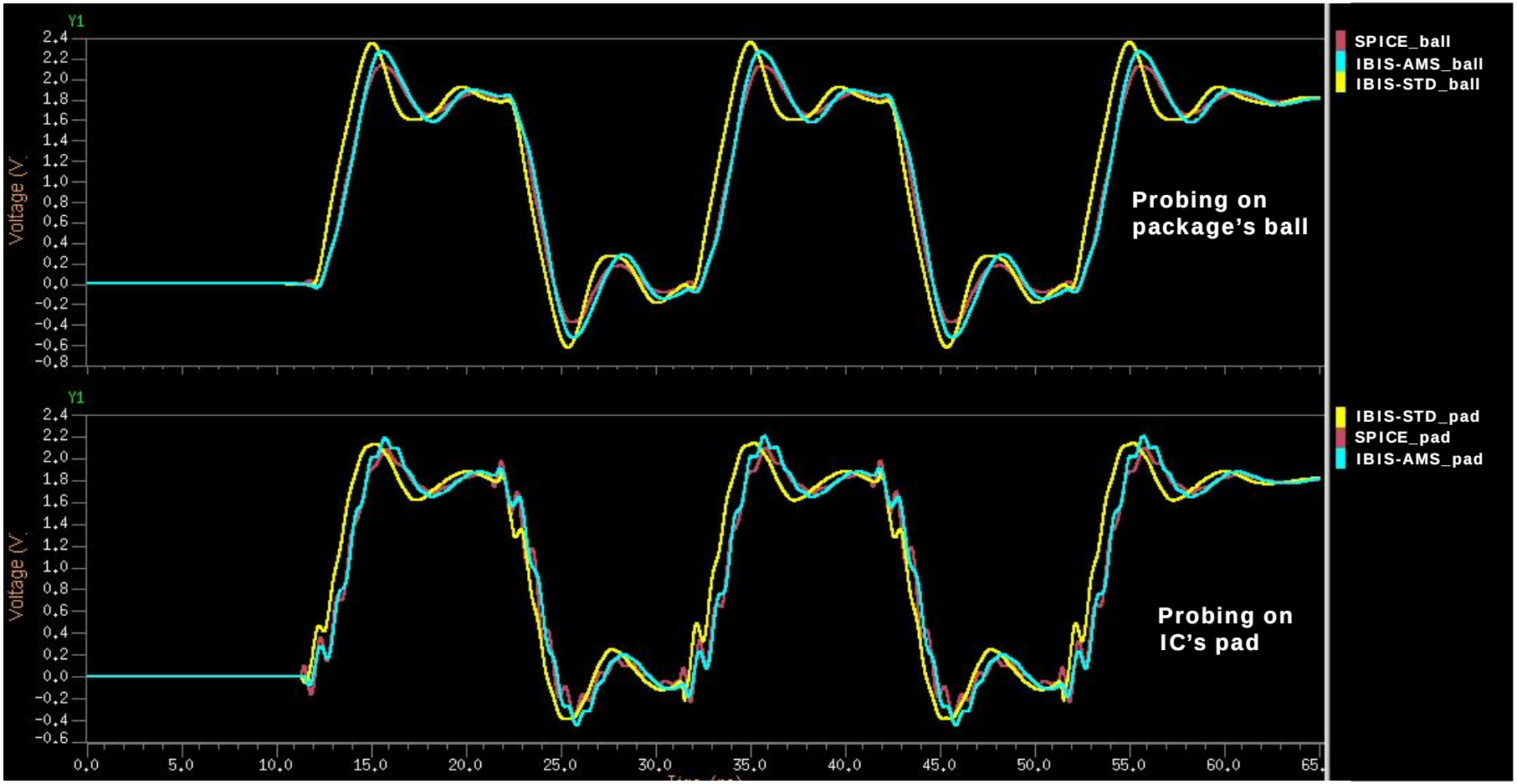
1 % (32 % IBIS-STD)

Test-case: 128M Nor Flash Memory (120nm)

A remarkable improvement has been achieved by implementing the ST "Gate Modulation" solution in the IBIS-AMS architecture.

Note: **The main contribution on recovering the error on the power/ground signals is due to the equivalent impedance put on the power nodes.**

IBIS-STD vs SPICE vs IBIS-AMS Comparison



Additional benchmarking results, extracted recently by SSO simulations on a 512Mb NOR Flash Memory (90nm).

BIRD98 & ST Proposal Convergence

- Today it is mandatory to provide to the IBIS community a reliable solution of the "Gate Modulation" problem. In fact, it is becoming a heavy bottleneck in every applications in which the SPICE simulations are not a possible alternative.

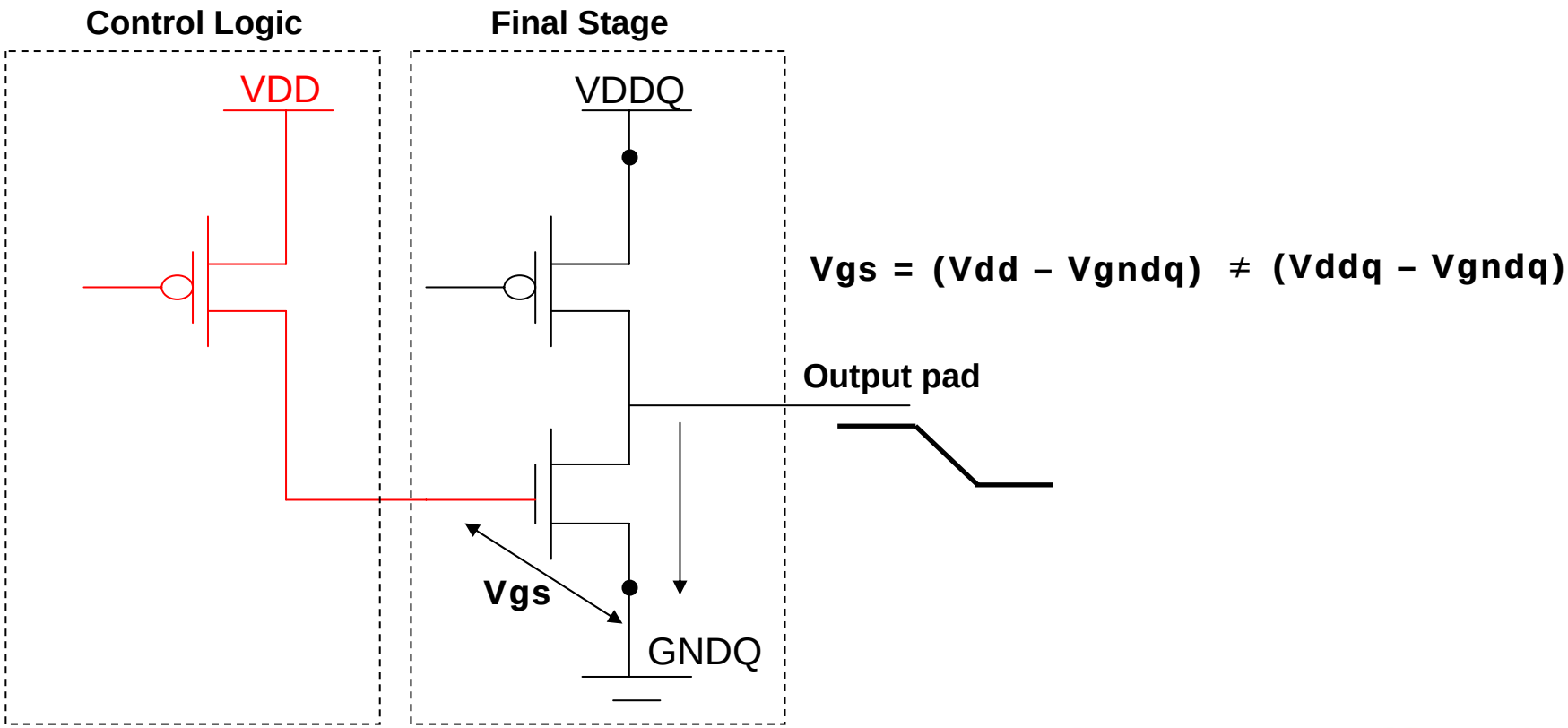
- Especially in the context of system-in-package design, where third parties' components may only be simulated by IBIS, and the power noise is critical because the ground planes are usually missing, it is impossible to predict fails before of the prototype-phase.

- Moreover, it has to be considered that the SPICE simulations seem too time-expensive, as IBIS alternative, in verifying the modern-system, whose complexity is rapidly increasing.

- The BIRD98 proposal is already a good solution for solving the "Gate Modulation Effect", but two changes are advised for making it much more accurate and general purpose. As well as for matching the ST proposal, validated by the IBIS-AMS implementation.

BIRD98 Suggested Change (1)

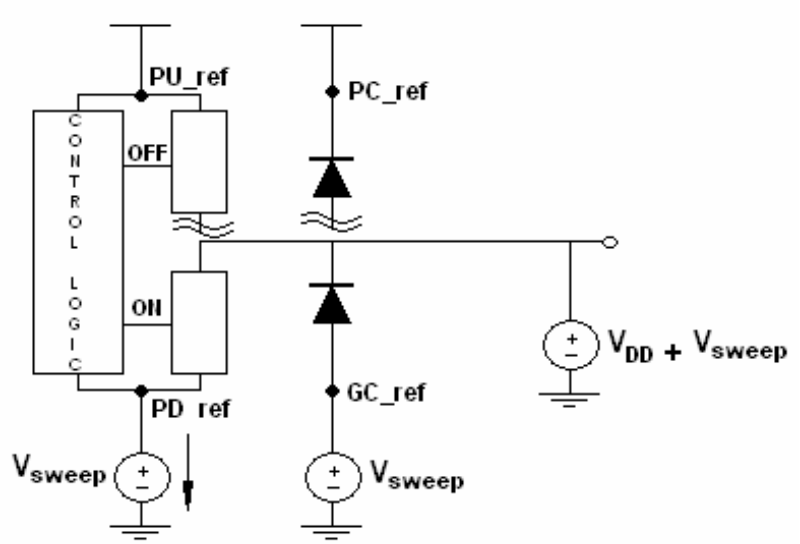
- To consider the instantaneous source voltage value (Vs) instead of the power supply one for the current scaling. This approach is more general purpose. In fact, it is **not always true** that the Vgs instantaneous value is the same of the power supply one during a bouncing noise. A typical case is when the control logic and the final stage are supplied with different supply voltages.

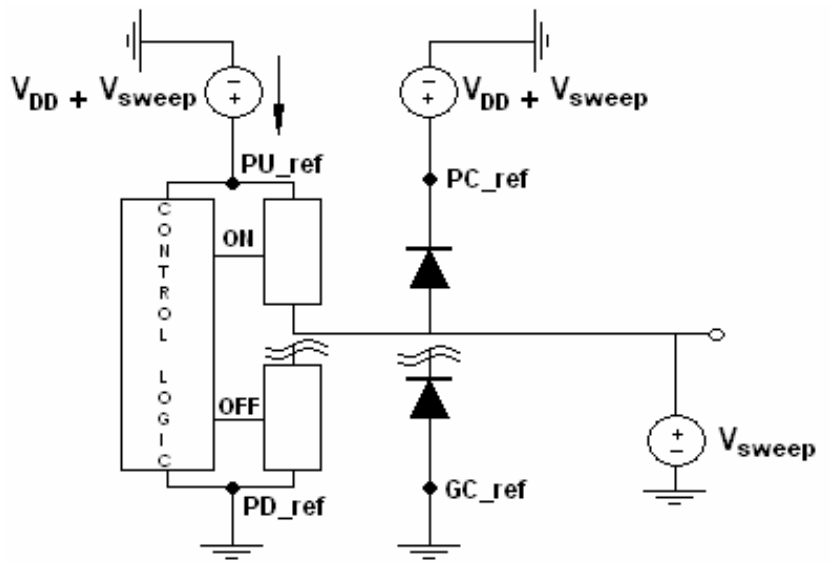


BIRD98 Suggested Change (2)

- It is preferable to draw the "effective" pullup (pulldown) currents by disconnecting the pulldown (pullup) stage from the pad, instead of the short current. In fact, to short the output pad to the reference node causes a change into the correct behaviour of the control logic driving capability when the control logic and the final stage are supplied by the same supply voltage.

- Below are reported the two advised circuits for drawing the "effective" pullup and pulldown currents





ST Proposal - Lowlights

- The Miller's capacitances (AC effects) are not included
- The final-stage's Ron instantaneous change is still a little bit under estimated compared to spice behaviour
- This proposal has been developed and validated only for CMOS driver

ST Proposal - Highlights

- It is a table-format solution
- Validated by the IBIS-AMS architecture on several test-cases
- Good trade-off between accuracy and complexity (both development and simulation time)
- Does not reveal proprietary information (full compliant with IBIS philosophy)
- Easy implementation into transistor-level EDA tools
- This proposal seems a reliable way for solving rapidly the gate modulation problem, which makes IBIS unusable in every non-ideal power supply simulation.

Reference Documents

- BIRD98 proposal (Arpad Muranyi, Intel)

http://www.vhdl.org/pub/ibis/birds/bird98.txt

- IBIS Simultaneous Switching Output Simulations Criticality (A. Girardi, STMicroelectronics)

http://www.vhdl.org/pub/ibis/futures/ST_Vgs_Presentation.pdf

- IBIS Gate Modulation Effect Proposal (A. Girardi, STMicroelectronics)

http://www.vhdl.org/pub/ibis/futures/ST_IBIS_Gate_Modulation_Effect.pdf

- IBIS Gate Modulation Effect (STMicroelectronics Proposal) (A. Girardi, G. Bernardi, R. Izzi, STMicroelectronics)

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