**6.1**

2) Voltage Ranges:

Points for each table must span the voltages listed in Table 1.

Table 1 – Voltage Ranges

| **Table** | **Low Voltage** | **High Voltage** |
| --- | --- | --- |
| [Pulldown] | GND – POWER | POWER + POWER |
| [Pullup] | GND – POWER | POWER + POWER |
| [GND Clamp] | GND – POWER | GND + POWER |
| [POWER Clamp] | POWER | POWER + POWER |
| [Series Current] | GND – POWER | GND + POWER |
| [Series MOSFET] | GND | GND + POWER |

As described in the [Pulldown Reference] keyword section, the I-V tables of the [Pullup] and the [POWER Clamp] structures are “Vcc relative”, using the equation:

*Vtable = Vcc - Voutput*

For example, a model with a 5 V power supply voltage should be characterized between (0 - 5) = -5 V and (5 + 5) = 10 V; and a model with a 3.3 V power supply should be characterized between (0 - 3.3) = -3.3 V and (3.3 + 3.3) = 6.6 V for the [Pulldown] table.

When tabulating output data for ECL type models, the voltage points must span the range of Vcc to Vcc - 2.2 V. This range applies to both the [Pullup] and [Pulldown] tables. Note that this range applies ONLY when characterizing an ECL output.

These voltage ranges must be spanned by the IBIS data. Data derived from lab measurements may not be able to span these ranges as such and so may need to be extrapolated to cover the full range. This data must not be left for the EDA tool to provide.

3) Ramp Rates:

The following steps assume that the default load resistance of 50 ohms is used. There may be models that will not drive a load of only 50 ohms into any useful level of dynamics. In these cases, use the semiconductor vendor’s suggested (nonreactive) load and add the load subparameter to the [Ramp] specification.

The ramp rate does not include packaging but does include the effects of the C\_comp parameter; it is the intrinsic output stage rise and fall time only.

The ramp rates (listed in AC characteristics below) should be derived as follows:

1. If starting with the silicon model, remove all packaging. If starting with a packaged model, perform the measurements as outlined below. Then use whatever techniques are appropriate to derive the actual, unloaded rise and fall times.
2. If: The Model\_type is one of the following: Output, I/O, or 3-state (not open or ECL types);

Then: Attach a 50 ohm resistor to GND to derive the rising edge ramp. Attach a 50 ohm resistor to POWER to derive the falling edge ramp.

If: The Model\_type is Output\_ECL, I/O\_ECL, 3-state\_ECL;

Then: Attach a 50 ohm resistor to the termination voltage (Vterm = VCC - 2 V). Use this load to derive both the rising and falling edges.

If: The Model\_type is either an Open\_sink type or Open\_drain type;

Then: Attach either a 50 ohm resistor or the semiconductor vendor suggested termination resistance to either POWER or the suggested termination voltage. Use this load to derive both the rising and falling edges.

If: The Model\_type is an Open\_source type;

Then: Attach either a 50 ohm resistor or the semiconductor vendor suggested termination resistance to either GND or the suggested termination voltage. Use this load to derive both the rising and falling edges.

1. Due to the resistor, output swings will not make a full transition as expected. However the pertinent data can still be collected as follows:
2. Determine the 20% to 80% voltages of the 50 ohm swing.
3. Measure this voltage change as “dV”.
4. Measure the amount of time required to make this swing “dt”.
5. Post the value as a ratio “dV/dt”. The EDA tool extrapolates this value to span the required voltage swing range in the final model.
6. Typ, Min, and Max must all be posted, and are derived at the same extremes as the I-V tables, which are:

Ramp rates for CMOS models:

typ = typical voltage, typical temp deg C, typical process

min = minimum voltage, max temp deg C, typical process, minus “Y%”

max = maximum voltage, min temp deg C, typical process, plus “Y%”

Ramp rates for bipolar models:

typ = typical voltage, typical temp deg C, typical process

min = minimum voltage, min temp deg C, typical process, minus “Y%”

max = maximum voltage, max temp deg C, typical process, plus “Y%”

where nominal, min, and max temp are specified by the semiconductor vendor. The preferred range is 50 deg C nom, 0 deg C min, and 100 deg C max temperatures.

Note that the derate factor, “Y%”, may be different than that used for the I-V table data. This factor is similar to the X% factor described above. As in the case of I-V tables, temperatures are junction temperatures.

1. During the I-V measurements, the driving waveform should have a rise/fall time fast enough to avoid thermal feedback. The specific choice of sweep time is left to the modeling engineer.

4) Transit Time Extractions:

The transit time parameter is indirectly derived to be the value that produces the same effect as that extracted by the reference measurement or reference simulation. See Figure 1.

The test circuit consists of the following:

1. A pulse source (10 ohms, 1 ns at full duration ramp) or equivalent and transitioning between Vcc and 0 V,
2. A 50 ohm, 1 ns long trace or transmission line,
3. A 500 ohm termination to the ground clamp reference voltage for TTgnd extraction and to the power clamp reference voltage for TTpower extraction (to provide a convenient, minimum loading 450 ohm - 50 ohm divider for high-speed sampling equipment observation of the component denoted as the device under test), and
4. The device under test (DUT).



1. - Example of TTgnd Extraction Setup

The TTgnd extraction will be done only if a [GND Clamp] table exists. A high to low transition that produces a positive “glitch,” perhaps several nanoseconds later, indicates a stored charge in the ground clamp circuit. The test circuit is simulated using the complete IBIS model with C\_comp and the Ct model defined under the [TTgnd] and [TTpower] keywords. An effective TTgnd value that produces a “glitch” with the same delay is extracted.

Similarly, the TTpower extraction will be done only if a [POWER Clamp] table exists. A low to high transition that produces a negative “glitch,” perhaps several nanoseconds later, indicates a stored charge in the power clamp circuit. An effective TTpower value that produces a glitch with the same delay is extracted.

It is preferred to do the extractions with the package parameters removed. However, if the extraction is done from measurements, then the package model should be included in the IBIS based simulation.

5) Series MOSFET Table Extractions:

An extraction circuit is set up according to Figure 2. The switch is configured into the “On” state. This assumes that the Vcc voltage will be applied to the gate by internal logic. Designate one pin of the switch as the source node, and the other pin as the drain node. The table currents designated as Ids are derived directly as a function of the Vs voltage at the source node as Vs is varied from 0 to Vcc. This voltage is entered as a Vgs value as a consequence of the relationship Vtable = Vgs = Vcc - Vs. Vds is held constant by having a fixed voltage Vds between the drain and source nodes. Note, Vds > 0 V. The current flowing into the drain is tabulated in the table for the corresponding Vs points.



1. - Example of Series MOSFET Table Extraction

It is expected that this data will be created from semiconductor vendor proprietary silicon models, and later correlated with actual component measurement.

**NEXT RELEASE**

2) Voltage Ranges:

Points for each table must span at least the typical column voltages listed in Table 1. Note, “0” is node 0 and represents a ground reference node. Also, the tables are not limited to the stated end points, but be careful of unintended extrapolations and of double counting clamp currents.

Table 2 – Voltage Ranges (End Points) for Vtable Entries

| **Table** | **Low Voltage** | **High Voltage** |
| --- | --- | --- |
| [Pulldown] | V(Pulldown\_ref, 0) - V(Pullup\_ref, Pulldown\_ref) | V(Pullup\_ref, 0) + V(Pullup\_ref, Pulldown\_ref) |
| [Pullup] | V(Pulldown\_ref, 0) - V(Pullup\_ref, Pulldown\_ref) | V(Pullup\_ref, 0) + V(Pullup\_ref, Pulldown\_ref) |
| [Pulldown] (ECL) | 0.0 V | 2.0 V |
| [Pullup] (ECL) | 0.0 V | 2.0 V |
| [GND Clamp] | V(Gnd\_clamp\_ref, 0) -V(Power\_clamp\_ref, Gnd\_clamp\_ref) | V(Gnd\_clamp\_ref, 0) + V(Power\_clamp\_ref, Gnd\_clamp\_ref) |
| [POWER Clamp] | V(Power\_clamp\_ref, 0) | V(Power\_clamp\_ref, 0) + V(Power\_clamp\_ref, Gnd\_clamp\_ref) |
| [Series Current] | -V(Power\_clamp\_ref, Gnd\_clamp\_ref) | V(Power\_clamp\_ref, Gnd\_clamp\_ref) |
| [Series MOSFET] | 0.0 V | V(Power\_clamp\_ref, Gnd\_clamp\_ref) |
| [ISSO PD] | -V(Pullup\_ref, Pulldown\_ref) | V(Pullup\_ref, Pulldown\_ref) |
| [ISSO\_PU] | -V(Pullup\_ref, Pulldown\_ref) | V(Pullup\_ref, Pulldown\_ref) |

As described in the [Pullup Reference] keyword section, the I-V tables of the [Pullup] and the [POWER Clamp] structures are “V(Pullup\_ref, 0.0) or V(Power\_clamp\_ref, 0) ~~Vcc~~ relative”, using the equation:

*Vtable\_pu = V(Pullup\_ref, Buffer\_I/O)*

*Vtable\_pc = V(Power\_clamp\_ref, Buffer\_I/O)*

[added, but put elsewhere and in same order as the above table

Vtable\_pd = V(Buffer\_I/O, Pulldown\_ref)

Vtable\_pc = V(Power\_clamp\_ref, Buffer\_I/O)

Vtable\_pd = V(Pulldown\_ref, Buffer\_I/O) for ECL

Vtable\_series = V(Pin1, Pin2) ??

Vtable\_mosfet = V(Vgs, 0.0) = V(Power\_clamp\_ref, Vs) ??]

Vtable\_isso\_pd = V(Buffer\_I/O, Pulldown\_ref)

Vtable\_isso\_pu = V(Pullup\_ref, Buffer\_I/O)

For example, a model with a 5 V power supply voltage (V(Pullup\_ref, 0.0) and 0 V V(Pulldown\_ref, 0.0)) should be characterized between (0 - 5) = -5 V and (5 + 5) = 10 V; and a model with a 3.3 V power supply should be characterized between (0 - 3.3) = -3.3 V and (3.3 + 3.3) = 6.6 V for the [Pulldown] table.

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