



IBIS Open Forum Minutes

Meeting Date: **February 1, 2019**

Meeting Location: **DesignCon 2019 IBIS Summit, Santa Clara, CA, USA**

VOTING MEMBERS AND 2019 PARTICIPANTS

ANSYS	Curtis Clark, Marko Marin*, Miyo Kawata* Toru Watanabe*, Akira Ohta*
Applied Simulation Technology	(Fred Balistreri)
Broadcom	(Yunong Gan)
Cadence Design Systems	Brad Brim, Ambrish Varma*, Ken Willis* Yingxin Sun*
Cisco Systems	(Stephen Searce)
CST	(Stefan Paret)
Ericsson	Anders Ekholm*, Anders Vennergrund*, Felix Mbairi* Hui Zhou*, Inmyung Song*, Mattias Lundqvist* Wenyan Xie*, Zilwan Mahmud*
GLOBALFOUNDRIES	Steve Parker*
Huawei Technologies	Antonio Ciccomancini*
Futurewei Technologies	Albert Baek*
IBM	Michael Cohen, Greg Edlund*
Infineon Technologies AG	Anke Sauerbrey*
Intel Corporation	Hsinho Wu*, Michael Mirmak*, Nhan Phan* Kinger Cai*, Eddie Frie*, Wendem Beyene* Yuanhong Zhao*
IO Methodology	[Lance Wang]
Keysight Technologies	Radek Biernacki*, Hee-Soo Lee*, Stephen Slater* Jian Yang*, Ming Yan*, Pegah Alavi*
Maxim Integrated	Joe Engert*, Yan Liang*, Charles Ganal*
Mentor, A Siemens Business	Arpad Muranyi*, Raj Raghuram*, Weston Beal* Vladimir Dmitriev-Zdorov*, Mikael Stahlberg* Todd Westerhoff*, Ed Bartlett*, Nitin Bhagwath*
Micron Technology	Randy Wolff, Justin Butterfield*
NXP	(John Burnett)
Raytheon	Joseph Aday*
SiSoft	Mike LaBonte*, Graham Kus*, Walter Katz*
SPISim	Wei-hsing Huang*
Synopsys	Ted Mido*, Adrien Auge*, John Ellis*, Sam Sim* Scott Wedge*
Teraspeed Labs	Bob Ross*
Xilinx	Ravindra Gali*
ZTE Corporation	(Shunlin Zhu)

Zuken
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(Michael Schaefer)
Lance Wang*

OTHER PARTICIPANTS IN 2019

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Socionext	Megumi Ono*, Motoaki Matsumura*, Yuji Nakagawa*
Toshiba	Imi Hitoshi*

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
February 22, 2019	624 227 121	IBISfriday11

For teleconference dial-in information, use the password at the following website:

<http://tinyurl.com/y7yt7buz>

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting.

NOTE: "AR" = Action Required.

OFFICIAL OPENING

The IBIS Open Forum Summit was held in Santa Clara, California at the Santa Clara

Convention Center, during the week of the 2019 DesignCon conference. About 76 people representing 33 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

<http://www.ibis.org/summits/feb19/>

Mike LaBonte welcomed everyone to the Summit, opening the meeting at 8:30 a.m. He thanked the sponsors Cadence Design Systems, Keysight Technologies, Mentor, a Siemens Business, and Synopsys for offsetting the cost of food and audio-visual equipment.

Mike stated IBIS was a big part of DesignCon and showed a list of the titles of DesignCon papers and sessions that mentioned IBIS. Mike noted the Summit presentations are up on the IBIS website.

IBIS UPDATE

Mike LaBonte (SiSoft, USA)

Mike LaBonte noted there are 26 members of the IBIS Open Forum currently. We recently had SPISim join IBIS. We have had 488 IBIS Open Forum teleconferences, not including all the IBIS Summit meetings. Mike reviewed that the IBIS parent organization is SAE and thanked them for their support. We expect to ratify IBIS 7.0 in 2019. Beyond IBIS 7.0 there are a few BIRDS up for consideration, as well as an IBIS-ISS syntax for modules. Mike noted that IBIS models are now widely available. He posed the question if system designers need any other information to do their analysis, such as timing analysis, FEC, optical links, PDN, etc. that IBIS could support.

Arpad Muranyi asked about using IBIS to model connectors. Mike replied this would be a good topic for the Interconnect task group to discuss.

JEITA EDA MODEL SPECIALTY COMMITTEE REPORT

Miyo Kawata (ANSYS, Japan)

Miyo Kawata gave an overview of JEITA's roles and their EDA Model Specialty Committee. The goal of the EDA Model Specialty Committee is to promote IBIS model use and help improve IBIS model quality. They help to improve IBIS model and S-parameter knowledge. One concern is that IBIS models are not using the latest keywords and model users should understand the latest keywords and know to look for them. They have held several Japan IBIS meetings since 2014 with large participation. The attendees were surveyed on major issues they see with IBIS models, and they highlight model availability as a key issue. Their upcoming activities include support for the 2019 Asian IBIS Summit, collecting requests for IBIS specification enhancements from Japan IBIS users, and investigating EDA models other than IBIS.

Mike LaBonte thanked JEITA for their support of IBIS and helping IBIS model users in Japan.

IBIS-ATM TASK GROUP REPORT

Arpad Muranyi (Mentor, a Siemens Business, USA)

Arpad Muranyi listed all the BIRDs discussed in the ATM task group. He noted that BIRD189 was approved this year that allowed other smaller BIRDs to be rejected. Looking ahead, there are four BIRDs currently up for discussion. He sent out an email about how to best proceed with redriver modeling to the IBIS and SI lists, but he has not received any feedback. The group has been discussing the C_comp proposal BIRD from Randy Wolff. The ATM group is also discussing DDR5 and possible support needed for single-ended IBIS-AMI models.

Weston Beal asked about BIRD189 replacing the need for [External Circuit]. Arpad replied that BIRD189 does not completely replace [External Circuit], as BIRD189 is focused on the interconnect and could include the on-die interconnect.

Mike LaBonte invited anyone who is interested in the meetings to join in the discussion. Arpad noted the meetings are on Tuesdays at noon Pacific time and the agendas are posted to the ibis-macro list at freelists.org.

INTRODUCING IBIS VERSION 7.0

Michael Mirmak (Intel Corporation, USA)

Michael Mirmak introduced IBIS 7.0 that has been assembled by the Editorial task group. He noted that draft 3 of IBIS 7.0 is currently available for review. The document is eligible for a vote at the IBIS Open Forum. Michael reviewed that 17 BIRDs are addressed in IBIS 7.0.

The Interconnect BIRD brings IBIS up-to-date for package modeling, and there are several related smaller BIRDs. The interconnect package modeling adds support to directly connect Touchstone and IBIS-ISS into the IBIS model. The BIRD also gives explicit buffer and die pad locations, which gives the ability to define better on die power networks.

IBIS 7.0 adds backchannel support for Tx and Rx equalizers to interact. IBIS now supports connecting 4-port Touchstone files for analog buffer characteristics. The Special_Param_Names parameter has been added to allow EDA functions beyond current IBIS limitations. Parameters can be passed to instances of [External Circuit]. Michael noted that supporting files can now be in directory structures.

IBIS 7.0 has additional editorial changes for readability, and there are now subsections with numbering. The document now contains hyperlinks to sections, tables and figures. Michael stated he is hoping to schedule a vote for IBIS 7.0 ratification on February 22, 2019 and hold the vote on March 15, 2019. Michael listed the BIRDs that were excluded from IBIS 7.0. There is also a list of known editorial issues already started. The next step for IBIS 7.0 would be to commission the IBIS parser.

Walter Katz commented that package modeling is greatly improved in IBIS 7.0. He noted we plan to start working on an Electrical Module Description (EMD) syntax to replace EBD.

Ambrish Varma asked if we could consider the DC_offset BIRD for IBIS 7.0. Michael replied this would cause a delay to IBIS 7.0. Michael asked if the DC_offset BIRD alone is enough to support DDR5.

IBIS VERSION 7.0 HIERARCHY ADDITIONS

Bob Ross (Teraspeed Labs, USA)

Bob Ross noted the hierarchy diagram under Section 3.3 includes all keywords and subparameters. The updated tree diagrams now include the new interconnect modeling keywords. The [Interconnect Model Group] and [Bus Label] keywords are scoped under [Component]. He noted the [Interconnect Model Set] keyword is a top-level keyword at the same level as [Component], or the [Interconnect Model Set] keyword can be located in a “.ims” file by itself.

Bob stated that the [Interconnect Model Group] definitions are in Section 5. Section 5 also provides examples of using the [Interconnect Model Group]. The [Interconnect Model Set] keyword is defined in Section 11, which also contains examples of using the new related keywords. Bob described how power and ground rails are defined, as well as I/O terminals for signals. He highlighted that the new interconnect modeling does still require a one-to-one pin mapping for signals.

Michael Mirmak asked if we can put the actual SPICE circuit information inside the IBIS file. Bob replied that the SPICE IBIS-ISS and Touchstone files must be linked in with the Interconnect syntax. Michael asked if the parser will check the .ims files, but not the SPICE files. Bob stated the parser will only check the .ims syntax, and he does not plan to have the parser check the IBIS-ISS files.

Arpad Muranyi asked if BIRD189 syntax can support one-to-one to connections for the signal pins while power supply connections can be many-to-many. Bob stated this is correct.

Bob asked Miyo Kawata what the subject for the next JETIA meeting will be and if the discussion will include the new interconnect modeling. Miyo stated it is not yet decided.

IBIS V7 AND IEEE 2401 HARMONIZATION

Genichi Tanaka (Renesas, Japan)

Genichi Tanaka shared an overview of the JEITA organizational structure. His group includes the Semiconductor Industry Association Japan. The LSI Package Board (LPB) standard is enabled by IEEE 2401 and IEC 63055 standards, which handle EDA standards. He would like to see IBIS standardized by IEC. He would also like to have closer communication with the IBIS committee. IEC's goal is to standardize the language for package and board terms. He shared their standardization strategy. The LPB format consists of 5 components: Management of Project, Netlist, Component, Rule of Design, and Geometry. Many different formats can be wrapped into the LPB. He noted there could be an issue since some IBIS models will include package models with interconnect models, and they do not want to double count the package effects. LPB introduced some additional functionality for package, pin, and shorts to use the IBIS 7.0 models correctly. He stated they are working on the latest draft of the LPB currently.

Walter Katz asked if there were any provisions for connector models or cables. Genichi replied that they do not exist. Walter stated IBIS would like to have models that can work with LPB.

Genichi requested that IBIS 7.0 become a formal standard. Mike LaBonte stated that he can put the formal standardization of IBIS on the agenda for an upcoming meeting.

COM & IBIS-AMI – HOW THEY RELATE & WHERE THEY DIVERGE

Hsinho Wu, Masashi Shimanouchi, Mike Li (Intel Corporation, USA)

Hsinho Wu reviewed Channel Operating Margin (COM) as a figure of merit considering the signal impairments defined by uncompensated channel effects, including ISI, jitter, noise, crosstalk, etc. COM is a standard followed by IEEE 802.3, OIF CEI, and JEDEC 204C. The goal of COM is to define the channel requirements.

Hsinho noted that COM does use an approach of looking at the pulse response similar to IBIS-AMI simulation. He noted that he is often asked how COM and IBIS-AMI compare and whether COM can be used to analyze a system. The differences between COM and IBIS-AMI include: use of reference Rx, Tx and package models, jitter and noise definitions, equalization tuning, margin calculation, and handling of non-linear behaviors.

Hsinho used both COM and IBIS-AMI in the analysis of a 50Gbs ethernet link. The COM result gives a ratio of the signal to the uncompensated noise at a BER. The IBIS-AMI simulations were run with the full channel. The first comparison between IBIS-AMI Init and COM showed a significant difference. He noted the primary reason for the difference was that the Tx noise was much smaller in the IBIS-AMI simulation than in the COM analysis. For simulation case 2, they made some adjustments to the Init Tx noise to get closer results. In case 3, they simulated the GetWave model to include the nonlinearities, which gave worse results than the COM calculation. Cases 4 and 5 compared not having jitter/noise amplification with not having a constant SNR at the Tx. Case 6 was a simulation with more realistic Rx and Tx characteristics. The result is better, but it is not COM equivalent. The conclusion is that the Tx gives comparable results, but for the Rx, the IBIS-AMI simulation can include the CDR and nonlinearities which are not accounted for with COM.

A question was asked if there was any plan to use JCOM as another method. Hsinho replied that JCOM can be more accurate than COM, but this could hurt interoperability.

Michael Mirmak asked, for an LTI system, if the Tx noise could be included at the Rx side. Hsinho replied the noise would be attenuated by the channel, so it needs to be accounted for at the Tx side. Michael asked if we should add a Tx noise parameter to the IBIS-AMI model. Hsinho suggested this should consider the amplitude, bandwidth, and distribution of the noise.

Ambrish Varma asked if BER is not really considered for COM. Hsinho replied that the amplitude is a peak-to-peak ratio for COM, while IBIS-AMI is running an actual simulation.

Graham Kus commented that he has seen similar work, but he expressed doubt that COM can be used for channel characterizations.

Vladimir Dmitriev-Zdorov asked about equalization optimization which is done together for COM, while for AMI the Tx and Rx are not optimized together. Hsinho replied that in his case the results are fairly close for the optimized Tx and Rx settings for both methods. But, there are small differences due to the different methods. Vladimir noted that JCOM would be the worst case of the best solution for the optimization. Hsinho noted there is good synergy between JCOM and the IBIS-AMI Init method, but there is a different API for JCOM. Todd Westerhoff commented that the results depend on how well Tx and Rx are modeled.

BASELINE WANDER, ITS TIME-DOMAIN AND STATISTICAL ANALYSIS

Vladimir Dmitriev-Zdorov (Mentor, a Siemens Business, USA)

Vladimir Dmitriev-Zdorov noted Baseline Wander (BLW) is low frequency noise when there is a DC blocking cap. There are two conditions for BLW. The first is where low-frequency noise can be passed into the channel. The second is from input data dependencies with low-frequency components.

Vladimir noted for most simulation techniques we have a finite length impulse response, with limited frequency information. The symbol response is affected by the limitations differently. The symbol response is also affected by both the channel attenuations and the DC blocking cap high pass filter effect. He noted that the problem with baseline wander in simulation is that it has very low frequency response. He proposed to separate the high and low frequency responses. State variables can be used to represent the low-frequency response. This can be used to simulate 100 million UI in about 1 second. The problem is the typical simulation data pattern does not have statistical coverage for BLW. When we have equalization at the Tx and Rx, we can have the equalization change the DC gain of the channel. The equalization does not reduce the baseline wander. For statistical analysis, we need to know the DC gain to reconstruct the response. He would like to see the DC gain as an IBIS-AMI reserved parameter.

Graham Kus asked about the motivation for including BLW in IBIS-AMI, as it seems like a lot of complication, and it might be better to consider it as part of the standard. Vladimir replied the user wants to know how big the BLW is and if it can be neglected. IBIS-AMI might be a good fit.

CHANNEL SIMULATION USING IBIS MODELS WITH ASYMMETRIC RISING AND FALLING EDGES

Ken Willis, Kumar Keshavan, Ambrish Varma (Cadence Design Systems, USA)

Ken Willis noted that, as we start to use equalization techniques for DDR, IBIS-AMI simulations will start to be used. One of the problems with using IBIS-AMI for DDR is that the rising and falling edges will be asymmetric. For impulse response generation, he used similar techniques that have been used for SerDes analysis. With this approach, the results show a difference when the IBIS-AMI simulation is compared to the circuit simulation. He looked at several iterations of ways to capture the rise and fall time differences. He achieved better correlation by looking at both the rise and fall responses in the IBIS-AMI simulation. He commented that this is not defined in the IBIS-AMI flow, and this information may be outside the scope of what IBIS should define in terms of what the EDA tool should provide as input to the GetWave model.

Todd Westerhoff asked if this approach is outside of the IBIS-AMI reference flow and if we should add a new reference flow for these cases. Ken replied that he is not following the reference flow, and his opinion is that EDA tool vendors can offer simulation methods outside of the defined reference flow. Todd stated that EDA tool customers want to compare results between tools and get comparable results. Ken stated this is not a priority for the IBIS committee. He noted this study is correlating to circuit simulation as the standard, which anyone can do. Walter Katz commented that we explicitly did not define how to generate the input data to the GetWave function.

Eddie Frie asked if this was a specific case or if Ken had looked at other asymmetric IOs. Ken replied that he has successfully used this approach with other asymmetric IOs.

Graham Kus commented that Xilinx had presented at DesignCon last year on simulation correlation between several different tools. Ken commented that these studies need to be careful to make sure the inputs are the same.

METHODS TO REDUCE EFFECTS OF DDR5 RISE/FALL ASYMMETRY IN IBIS-AMI SIMULATIONS

Walter Katz (SiSoft, USA)

Walter Katz stated he has also looked at the rise and fall time differences for IBIS-AMI simulation. DDR5 specifies DRAM equalization, and equalization is expected at the controller side, but the JEDEC specification is still being developed. Rise and fall impedances can also be different. Walter compared the rising step response and an inverted falling step response. He presented two methods to improve the responses used by IBIS-AMI. The first he called a “melled” response and is an average of the rising and inverted falling responses. The “mixed” response uses the rising response on the rising edges and the falling response on the falling edges, with the DC value for each forced to an average value. He noted the “mixed” impulse response gave the best results when compared with the circuit simulation.

Arpad Muranyi asked if this method will give an asymmetric eye. Walter Katz replied the “mixed” method would give an asymmetric eye. Todd Westerhoff commented that this does not follow the reference flow. Walter stated that the EDA tool is responsible for generating the waveform input into GetWave, and in this case, it is a more complicated impulse response. Todd stated that this is not compliant, and he suggested we should use consistent language to describe these techniques. Ken Willis stated the most important thing is to make sure we can recreate the circuit simulation as closely as possible. Todd commented that for the IBIS standard we should consider adding an additional reference flow. Walter noted he is publishing his method for generating the responses, and he is open to including it as a reference flow.

Steve Parker asked if this can be done inside the IBIS-AMI executable. Walter replied that you would have to put the response processing in the GetWave flow.

Vladimir Dmitriev-Zdorov asked if this is the digital flow or the older flow. Walter stated that this is looking at the responses edge-by-edge for GetWave.

Nitin Bhagwath asked why not clarify the flow that is being used to eliminate the confusion. Ken

commented that these are EDA tool issues.

STUDY ON POTENTIAL FEATURE ADDITIONS FOR BIT-BY-BIT SIMULATION TECHNIQUE TO ADDRESS DDR5 REQUIREMENTS

Ted Mido (Synopsys, Japan)

Ted Mido highlighted the challenges for DDR simulation including the addition of equalization for DDR5. He compared a few simulation methods to simulation the equalization. The first simulation method being convolution where the input pattern is convolved with the channel response. The second simulation method was using the pulse response and superposition to create the waveform. The pulse response can capture some of the nonlinearity. The third method compared was a transient circuit simulation. He proposed a configurable test bench to simulate these different methods.

Ted looked at methods for capturing SSO with superposition techniques. He highlighted the timing variation from SSO noise due to the timing shifts in the chip. He proposed to use superposition to capture the SSO noise in a PDF and compare this to the transient simulation. He noted the nature of the SSO noise is a gaussian response. Using a PDF for SSO noise and jitter in the IBIS-AMI simulation showed good correlation to the circuit simulation. Ted also suggested to use the clock_times vector as an input variable to pass in the clock information to the IBIS-AMI executable. He gave two example simulations, one with correlated jitter and one with uncorrelated jitter between DQ and DQS. The results showed that the jitter tracking between DQ and DQS was important for the DFE timing.

John Ellis asked if this study included the several UI delay between DQ and DQS. Ted replied that it did not, but he may consider it for a future study.

Mike LaBonte asked if Ted thought we should have a BIRD to address this issue. Ted replied yes, but was not sure about writing it. Mike encouraged him to partner with another IBIS member.

STUDY OF DDR ASYMMETRIC RT/FT IN EXISTING IBIS-AMI FLOW

Wei-hsing Huang#, Wei-kai Shih## (SPISim, #USA, ##Japan)

Wei-hsing Huang noted there are still questions about using IBIS-AMI for DDR including the DQ centered around VREF and the possibility of asymmetric rise and fall times. He derived a linear transform between rise and fall times and looked at an example with an alternative bit pattern. He noted there could be issues with glitches when constructing the GetWave input from asymmetric rising and falling edges.

Todd Westerhoff asked if these techniques have been implemented in the simulation tools. Wei-hsing replied that this study looked at the issue from the model makers view point, and this is an experiment to find the best approach.

MODELING FORWARDED CLOCK INTERFACES WITH IBIS-AMI

Justin Butterfield (Micron Technology, USA)

Justin Butterfield described upcoming DDR interfaces, which expect to use equalization features, both at the DRAM and controller side. He noted IBIS-AMI is directed toward modeling a CDR rather than use of a forwarded clock. DQ is clocked by DQS, but they use independent paths. Two different modeling approaches are under consideration: use a CDR as the modeling construct relying on existing jitter parameters or use the clock_times vector as an input.

Justin showed a DQ and DQS simplified circuit where correlated jitter on both DQ and DQS might not cancel out due to the DQS clock tree delays. He noted the cancelation will depend on the frequency of the jitter. He showed a sinusoidal jitter example. At low frequency, the sinusoidal jitter partially canceled out. While at high frequency, there was an additive effect to the jitter.

Walter Katz commented that DDR is different from traditional SerDes, as it can have small burst lengths and quick turnaround times. He noted IBIS-AMI does not deal with short bursts very well.

John Ellis asked if the diagram showing clock tree with equal delays to the DQs was true. Justin replied that the delays could be the same, but it is not always the case. John asked if you have different tree path delays, how you would do the frequency calculation for each DQ. Justin replied that he does not see a significant delta across the clock tree to each DQ.

Wendem Beyene asked if "clock times vector" refers to "clock ticks". Justin replied that, yes, these mean the same thing.

RX CLOCK FORWARDING INVESTIGATION

Stephen Slater (Keysight Technologies, USA)

Stephen Slater commented he was pleased to see Justin's presentation, though they had not coordinated. He reiterated that, for DDR, the DQS clocks more than one DQ signal. It is important to capture internal delays to get accurate jitter. He asked why not provide the clock times. He also proposed to go one step further and present the clock waveform to the model. This could use an interpolator on the strobe signal to align the timing to the DQ signals, which would model how the controller adapts or tunes the sampling of the strobe to optimize the eye.

Stephen started with a DDR4 simulation reference case and made assumptions for DDR5. He did not have an IBIS model for the Tx, but he used an ideal model with correct die capacitance, drive strength, rise and fall times, and ODT for Reads. For the DRAM, he used a simulator-specific optimization of the DFE taps based on the impulse response. He noted that Keysight is focusing on bit-by-bit simulation currently, and he commented that they already characterize the rise and fall responses before running the IBIS-AMI flow. He also commented that they are happy with the DC_Offset BIRD. Stephen noted in the results, when the DFE taps are fixed, the eye is not sensitive to small changes in strobe timing, but there is a strong relationship between signal, clock timing, and DFE tap values that the controller can use to optimize the link.

IMPACT OF TRUE STROBE TIMING ON DDR CHANNEL SIMULATION WITH IBIS-AMI MODELS

Ken Willis, Kumar Keshavan, Ambrish Varma (Cadence Design Systems, USA)

Ambrish Varma noted that we can use a CDR as an idealized clock. In the Cadence flow the clock is recovered currently. They implemented a separate strobe path and compared this with the CDR approach. The result in the ideal case is that the strobe case gave a better eye. In the True Strobe Timing (TST) approach the jitter made a big impact. In the CDR flow the jitter is tracked. Using the CDR flow can hide impairments.

Ambrish Varma noted that we can use a CDR as an idealized clock, but this can be a problem. In the Cadence flow, clocks can be ideally sampled by the eye sampler, or they can be generated by the models, with a CDR for instance, and sent to the eye sampler. He compared the approach of using a CDR and using TST. He simulated a 6Gbps system with both Rx CTLE and 4 tap DFE for the following cases: CDR, TST, and TST with jitter impairments. The result is that the CDR method hides the shift seen in the strobe-based method. When jitter is added to the system the CDR can incorrectly remove some of the jitter impairments.

Michael Mirmak asked if they included crosstalk effects, particularly between data and strobe. Ambrish replied this is a first order study, but he would like to include crosstalk and other effects in a later study.

Todd Westerhoff asked if they are using an IBIS-AMI model for the DQS Rx. Ambrish stated they are using an IBIS-AMI model for the data but not for the strobe. He noted that the same channel is used for both data and strobe, but with different data patterns.

Stephen Slater commented that we may need to expand the footprint of IBIS-AMI to treat multiple DQ for one DQS.

ON DIE DE-CAP MODELING PROPOSAL

Kazuki Murata*, Megumi Ono** (Ricoh*, Socionext**, Japan)

Megumi Ono noted, for the chip PDN, the on-die resistance affects both the IR drop and Q factor and the on-die decoupling capacitance (de-cap) affects the high-frequency power supply noise. Many papers in IBIS have reported the importance of on-die de-cap starting as early as 1997 through 2017. A survey of board and system designers at the LPB developers workshop in September 2017 found that guidelines were available, but most designers could not get an on-die cap model. Megumi proposed a new IBIS keyword for the on-die de-cap, but will also investigate IBIS 7.0 support.

Megumi suggested that measurement could be used, until the chip's PDN model information was made available. For measurement, they examined the impedance between VCC and GND pins using a VNA or impedance analyzer. Good correlation was seen up to and just above 100 MHz when compared to the design value. There is a voltage dependency effect, highlighting the need to properly bias the on-chip PDN. Megumi showed the equivalent circuit and how it would map to the proposed IBIS keyword. They are planning to submit a BIRD by March 14 to address this issue.

Walter Katz commented that IBIS 7.0 supports an on-die and an on-package model for the PDN. Megumi replied that a simple approach was presented here using the proposed keyword. A more complex method would be supported through IBIS-ISS or TS. Walter commented the downside is that Touchstone does not cover process or voltage variations.

Zhiping Yang stated the package is a per-pin model and asked if we have a way to do a distributed model in the package. Zhiping also commented for on-die, power gating makes measurement very difficult. You will need to model power gating to accurately represent the measurement. Walter suggested that [Pin Mapping] can associate different buffer groups to subsets of pins. Genichi Tanaka commented we would need to specify the control signals for the power gating, and this is not supported today in IBIS.

Mike LaBonte asked if LPB supports the on-die capacitance currently. Genichi replied this can be done through C-format, but having it in IBIS would be preferable.

IBIS BASED MODELING FOR SYSTEM-LEVEL POWER DELIVERY

Zhiping Yang*, Songping Wu*, Kinger Cai**, Joshua Luo***, Yinxin Sun*** (Google*, Intel Corporation**, Cadence Design Systems***, USA)

Zhiping Yang showed a typical consumer device's platform with on-die elements, the package, USB charging ports, and a battery. He posed common PDN questions including IR drop issues and supplying sufficient transient current. The battery is also a concern, and simulations for the battery and charger are difficult due to lack of models. PDN questions can be analyzed, but having a unified analysis flow would help. It would be useful to do power and thermal co-simulation.

Zhiping showed a DC simulation common methodology involving looking for worst-case, package resistance network, and the die as a current sink/load. Current models (non-IBIS) and datasheets show maximum current and minimum voltage. Today, for VRMs, no high-quality models are available for either the AC or DC characteristics. He noted VRM models are typically behavioral, transistor, or Simplis models. There are also challenges getting R_{die}/C_{die} or Chip Power Model (CPM, active) data from vendors. Zhiping proposed to include current consumption information in IBIS to simulate power effects.

Michael Mirmak asked about VRMs and feedback and if the use of an IBIS-AMI like approach for analog behaviors would work, due to lack of feedback. Zhiping replied, yes, feedback is involved.

Mike LaBonte asked if IP protection is a concern. Zhiping responded yes.

An audience member asked whether Zhiping would like to incorporate the entire power network and behavior in the model. Zhiping replied, yes, eventually.

OPEN DISCUSSION

None.

CONCLUDING ITEMS

Mike LaBonte again thanked the sponsors Cadence Design Systems, Keysight Technologies, Mentor, a Siemens Business, and Synopsys, the presenters, organizers and attendees.

The meeting concluded at approximately 4:30 PM.

NEXT MEETING

The next IBIS Open Forum teleconference meeting will be held on February 22, 2019. The following teleconference meeting is tentatively scheduled for March 15, 2019.

NOTES

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This meeting was conducted in accordance with ANSI guidance.

All inquiries may be sent to info@ibis.org. Examples of inquiries are:

- To obtain general information about IBIS.
- To ask specific questions for individual response.
- To subscribe to the official ibis@freelists.org and/or ibis-users@freelists.org email lists (formerly ibis@eda.org and ibis-users@eda.org).
- To subscribe to one of the task group email lists: ibis-macro@freelists.org, ibis-interconn@freelists.org, or ibis-quality@freelists.org.
- To inquire about joining the IBIS Open Forum as a voting Member.
- To purchase a license for the IBIS parser source code.
- To report bugs or request enhancements to the free software tools: `ibischk6`, `tschk2`, `icmchk1`, `s2ibis`, `s2ibis2` and `s2iplt`.

The BUG Report Form for `ibischk` resides along with reported BUGs at:

<http://www.ibis.org/bugs/ibischk/>
<http://www.ibis.org/bugs/ibischk/bugform.txt>

The BUG Report Form for `tschk2` resides along with reported BUGs at:

<http://www.ibis.org/bugs/tschk/>
<http://www.ibis.org/bugs/tschk/bugform.txt>

The BUG Report Form for `icmchk` resides along with reported BUGs at:

<http://www.ibis.org/bugs/icmchk/>
http://www.ibis.org/bugs/icmchk/icm_bugform.txt

To report `s2ibis`, `s2ibis2` and `s2iplt` bugs, use the Bug Report Forms which reside at:

<http://www.ibis.org/bugs/s2ibis/bugs2i.txt>
<http://www.ibis.org/bugs/s2ibis2/bugs2i2.txt>
<http://www.ibis.org/bugs/s2iplt/bugspl.txt>

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

<http://www.ibis.org/>

Check the IBIS file directory on ibis.org for more information on previous discussions and results:

<http://www.ibis.org/directory.html>

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SAE STANDARDS BALLOT VOTING STATUS

Organization	Interest Category	Standards Ballot Voting Status	November	December	January	February 1,
			30, 2018	21, 2018	11, 2019	2019
ANSYS	User	Active	-	X	X	X
Applied Simulation Technology	User	Inactive	-	-	-	-
Broadcom Ltd.	Producer	Inactive	-	-	-	-
Cadence Design Systems	User	Active	X	X	X	X
Cisco Systems	User	Inactive	-	-	-	-
CST	User	Inactive	-	-	-	-
Ericsson	Producer	Inactive	-	-	-	X
GLOBALFOUNDRIES	Producer	Active	X	-	X	X
Huawei Technologies	Producer	Inactive	-	-	-	X
IBM	Producer	Active	-	-	X	X
Infineon Technologies AG	Producer	Inactive	-	-	-	X
Intel Corp.	Producer	Active	X	X	X	X
IO Methodology	User	Active	X	X	X	-
Keysight Technologies	User	Active	X	X	X	X
Maxim Integrated	Producer	Inactive	-	-	-	X
Mentor, A Siemens Business	User	Active	X	X	X	X
Micron Technology	Producer	Active	X	X	X	X
NXP	Producer	Inactive	-	-	-	-
Raytheon	User	Inactive	-	-	-	-
SiSoft	User	Active	X	X	X	X
SPISim	User	Inactive	-	-	-	X
Synopsys	User	Active	X	-	X	X
Teraspeed Labs	General Interest	Active	X	X	X	X
Xilinx	Producer	Inactive	-	-	-	X
ZTE Corp.	User	Inactive	-	-	-	-
Zuken	User	Inactive	-	-	-	X

Criteria for SAE member in good standing:

- Must attend two consecutive meetings to establish voting membership
- Membership dues current
- Must not miss two consecutive meetings

Interest categories associated with SAE standards ballot voting are:

- Users - members that utilize electronic equipment to provide services to an end user.
- Producers - members that supply electronic equipment.
- General Interest - members are neither producers nor users. This category includes, but is not limited to, government, regulatory agencies (state and federal), researchers, other organizations and associations, and/or consumers.