



## IBIS Open Forum Minutes

Meeting Date: **November 12, 2018**

Meeting Location: **Tokyo, Japan**

### VOTING MEMBERS AND 2018 PARTICIPANTS

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Broadcom	(Yunong Gan)
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CST	Stefan Paret
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Infineon Technologies AG	(Christian Sporrer)
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IO Methodology	Lance Wang
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Maxim Integrated	Joe Engert, Yan Liang
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University of Siegen	Elmar Griese
University of Technology Hamburg	Torben Wendt
Xrossvate	Toshiyuki Kaneko*
Yamaha Corp.	Tetsuya Kakimoto*

In the list above, attendees at the meeting are indicated by \*. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

## UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
November 14, 2018	Asian IBIS Summit (Shanghai) – no teleconference	
November 16, 2018	Asian IBIS Summit (Taipei) – no teleconference	
November 30, 2018	624 227 121	IBISfriday11

For teleconference dial-in information, use the password at the following website:

<http://tinyurl.com/y7yt7buz>

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting.

NOTE: "AR" = Action Required.

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## OFFICIAL OPENING

The Asian IBIS Summit took place on Monday, November 12, 2018 at the Akihabara UDX building in Tokyo. About 135 people representing 81 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

<http://www.ibis.org/summits/nov18a/>

Mike LaBonte opened the summit by welcoming everyone and thanking the sponsors ANSYS, Inc., Apollo Giken Co., Cadence Design Systems, Cybernet Systems, Keysight Technologies, Ricoh, Toshiba Corporation, and Zuken, Inc. Mike thanked JEITA for organizing the event and for their continued support of the JEITA/IBIS partnership. He noted that minutes of the meeting would be posted.

Miyo Kawata gave a welcome address on behalf of JEITA, mentioning the history of JEITA/IBIS meetings, and explaining meeting logistics.

Takayuki Shiratori of Zuken also helped conduct the meeting.

### **JEITA EDA MODEL SPECIALTY COMMITTEE REPORT**

Miyo Kawata (ANSYS Japan K.K., Japan)

The EDA Model Specialty Committee replaced the IBIS Promotion Working Group in 2017. It falls under the Engineering Chain Management Committee within JEITA. Their focus is broadening beyond IBIS to include other models required for EDA analysis, such as S-parameters. The committee has a number of activities, which will include IBIS training workshops in both Tokyo and Osaka, and JEITA members attending DesignCon 2019. At each meeting, members have been surveyed to understand the needs of IBIS users. The percentage of circuit designers and simulation engineers participating has increased, and model availability is still a problem. The most used models are IBIS, with S-parameters coming in second, and IBIS-AMI third.

### **IBIS UPDATE**

Mike LaBonte (SiSoft, USA)

The status and activities of the IBIS Open Forum were described. Mike showed the progress on development of the IBIS 7.0 specification, which he estimated might be ratified in March of 2019, if all goes well. Mike noted that few BIRDS were currently in the pipeline for further development, encouraging the audience to consider submitting their own ideas for IBIS. He planned to give a short walk-through of the BIRD submission and adoption process during final discussion, if time would permit.

### **PACKAGE MODELS FOR CRITICAL TIMING VALIDATION WITH IBIS**

Yukio Masuko (Japan Electronics Packaging and Circuits Association (JPCA), Japan)

JPCA is involved in a number of areas, and this presentation fell under the Circuits area. The JPCA Design Academy created a trial PCB with an FPGA and DDR4 SDRAMs. The stackup and layout carefully modelled the 1.2V VCC power planes. The package power delivery model is important, and BIRD189.7 should help with that. However, DDR4 timing requires verification of metrics that IBIS does not yet support. Timing should be measured at the die, but the quality of that measurement depends on the type of package model used. [Define Package Model]

does not support both coupled matrices and distributed RLC models with length. Lumped LCR models suffice for signal and power integrity analyses, but distributed models are better for timing analysis. S-parameter models are best, but transmission line models are sufficient as long as impedance variations are captured.

## **BEST CASE ANALYSIS**

Shinichi Maeda (KEI Systems, Japan)

IBIS models have data for three process corners. The variations in IC performance are normally distributed within the lots of wafers, within each wafer, and even across a single chip. Drivers and receivers are not correlated for performance, and there is a wide range of performance scenarios for the combination of chips. As chip speeds increase, making them work in all scenarios may not be feasible. Adaptive equalization is required to compensate for the extreme variation. Training protocols make this possible, selecting the best case settings. In IBIS, this means capturing more variation than just typ/min/max settings. [Model Selector] is available to represent other variations, but classic IBIS buffers do not model equalization. IBIS-AMI does model equalization, and is suitable for best case analysis, but because they use executables, they are more difficult to inspect.

## **A PRACTICAL METHODOLOGY FOR SERDES DESIGN**

Amy Zhang\*, Guohua Wang\*, David Zhang\*, Zilwan Mahmud\*, Anders Ekholm\*\* (Ericsson, \*China, \*\*Sweden)

[Presented by Anders Ekholm (Ericsson, Sweden)]

Analyzing a SerDes channel to find the best case operation involves not only many combinations of driver and receiver settings, but also a significant number of interconnect characteristics that must be explored under typ/min/max conditions. Simulating 1 million bits across all possible variations for one example would take 506.25 days. The challenge is to make satisfactory design decisions without running many simulations. Ideally, we would create an equation that quickly models system performance, given all of the system condition inputs that can vary. This can be done using Design of Experiments (DOE) methods to statistically sample the parameter space, producing a Response Surface Model (RSM) using relatively few simulations. A CEI-28g example was shown, with the quality of the RSM fit evaluated. Sensitivity analysis was used to assign a different sampling distribution to each factor. Millions of conditions were then evaluated very quickly. Increasingly, we will find that the best/worst case analysis supported by typ/min/max data will not suffice for design closure. Adding an option for IBIS-AMI to represent a full distribution of data would help with DOE analysis, and would allow for predicting performance confidence intervals.

## **MODEL CORRELATION FOR IBIS-AMI**

Wenyan Xie\*, Guohua Wang\*, David Zhang\*, Anders Ekholm\*\* (Ericsson, \*China, \*\*Sweden)

[Presented by Anders Ekholm (Ericsson, Sweden)]

Once simulation results are correlated to corresponding measured results, simulation can be used to verify cases that are beyond the scope of measurement. A method for correlating IBIS-AMI Tx models was described. A slow clock pattern made it easier to compare edges and

amplitudes, and also to compare FFE tap action. Each tap setting was swept across all values, and correlation evaluated for each. It is necessary to achieve good correlation for the Tx first, because it will be used to drive the Rx for Rx correlation. Sweeping Tx FFE tap settings again, the Rx eye at the decision point was monitored. Some devices have an internal ability to report the internal Rx eye. Example correlation results for eye width and height were shown. Time domain waveforms can also be compared using Figure of Merit (FOM) or Feature Selective Validation (FSV). More than the usual 5 FSV metrics should be used, each weighted differently. The example was correlated against only typical silicon. We do not know the span of real silicon performance that IBIS-AMI min and max corners captures. Having models with statistical distribution for each parameter would be better.

A question was asked about how the silicon sample was chosen to match the typ case model. The answer was that no special effort was made to select the silicon, it just happened that way.

## **BREAK AND DISCUSSION**

With presentations ending ahead of time before the planned break, Mike LaBonte took the opportunity to briefly show the IBIS website to explain the process by which the IBIS specification is developed. BIRD documents are written by people from one or more organizations using a template, and submitted to the IBIS Chair. Often there are multiple authors, from different companies. The BIRD includes a statement of the issue to be addressed, particular requirements for the solution, and proposed changes to the current IBIS specification to meet the requirements. Anyone may submit a BIRD, but only official IBIS members may vote. The BIRD is discussed in meetings, sometimes over an extended period, and finally a vote to accept it is taken in an IBIS Open Forum meeting. If it passes, the BIRD eventually will be incorporated into a future IBIS specification produced by the IBIS Editorial Task Group.

## **CONCERNS WHEN APPLYING CHANNEL SIMULATION TO DDR INTERFACE**

Masaki Kirinaka, Akiko Tsukada (Fujitsu Interconnect Technologies Limited, Japan)  
[Presented by Masaki Kirinaka (Fujitsu Interconnect Technologies Limited, Japan)]

The JEDEC standard for DDR4 SDRAM requires proving  $1e-16$  maximum Bit Error Rate (BER), theoretically requiring the simulation of a very large number of bits. SPICE is too slow, but it can be done with IBIS-AMI if the channel and models are Linear Time Invariant (LTI). A test was done to see if the DDR4 DQ signal would be LTI, comparing the rise and fall impulse responses, as well as the linearity of impedance curves. Max corner simulations were performed using both SPICE and IBIS-AMI. With increasing speed, a difference was observed, with the SPICE crossing point shifting upward. Experimentally, the IBIS-AMI rise and fall launch times were shifted, resulting in a much better match with SPICE for memory write transactions. It was also discovered that the On Die Termination (ODT) I-V curve of the controller Rx was non-linear, resulting in asymmetric rise/fall impulse responses for read transactions. A future experiment might be to similarly test DDR5. A comment was made that an eye pattern waveform closer to SPICE might be obtained by adding a Tx\_DCD condition to the input pattern.

A question was asked if SPICE analysis was using the SPICE model or using the IBIS model. The answer was that it was analyzed using the IBIS model. Another question was about how the non-linear ODT on slide 17 was described. It was represented by the IV curve of the IBIS

model. A question was asked about how was it that in a channel simulation, the rising waveform and falling waveform would always be symmetric. Another question was if convolution flow was being used with classic (non-AMI) IBIS buffers. The answer was that convolution method was used with waveforms from classic IBIS buffers. It was believed that the convolution integration was producing symmetry.

## **SIMULATION TECHNOLOGY FOR MEMORY DESIGNERS IN DDR4/5**

Satoshi Nakamizo (Keysight Technologies, Japan)

With DDRx speeds increasing, Inter-Symbol Interference (ISI) and crosstalk increase, although jitter is improving slowly. Various LPDDRx technologies run at different speeds and voltages, and with different evaluation criteria. Internal calibrations of Vref and data channel skews improve performance. Packages, PCB, and connectors were producing greater ISI at higher speeds. The use of masks to check DDR4 eyes was a paradigm shift from setup/hold, slew derating, and voltage thresholds. Four DDR5 challenges were described: increased ISI and Rj, crosstalk, SSO/SSN, and channel attenuation. For modeling DDR5, it was noted that IBIS-AMI discards the common mode signal, and assumes a 0V center voltage. For DQ, a Vref center voltage would need to be specified. Also, IBIS-AMI must deal with asymmetric rise and fall. The pros and cons of statistical, IBIS-AMI time domain, and SPICE/Verilog-A simulation approaches were compared.

## **STUDY OF DDR ASYMMETRIC RT/FT IN EXISTING IBIS-AMI FLOW**

Wei-kai Shih\*, Wei-hsing Huang\*\* (SPISim, \*Japan, \*\*USA)

[Presented by Wei-kai Shih (SPISim, Japan)]

Wei-kai described how statistical and time domain IBIS-AMI flows worked. For asymmetric rise/fall, Wei-kai described a method for deriving a fall edge from the rise edge, or vice-versa, using a transfer function. He noted it would still be necessary for IBIS-AMI to know the common mode DC offset for single-ended signals. Wei-kai showed example pseudo-code for the transfer function to recover a fall response from the rise response. This could be used to construct eye diagrams with rise/fall asymmetry. A recursive algorithm for calculating eye PDF with asymmetric rise/fall was described. Simulating bit-by-bit with Tx and Rx AMI\_GetWave should work well, but there would be glitches if convolution was involved at the Rx. Pseudo-code for the AMI\_GetWave process was shown.

## **STUDY ON POTENTIAL FEATURE ADDITIONS FOR BIT-BY-BIT SIMULATION TECHNIQUE TO ADDRESS THE DDR5 REQUIREMENTS**

Ted Mido (Synopsys, Japan)

Ted gave an overview of IBIS-AMI and compared convolution, superposition, and transient analysis techniques. New DDR technologies require equalization and new statistical verification methods. A configurable testbench would be needed. Ted described a two-step approach for including SSO in eye diagram generation. He showed that the ISI for a Power Delivery Network (PDN) would take a relatively long time to settle, as the networks are large. The slopes of the rise and fall step responses could be used to calculate jitter from voltage noise. Convolution

would be used to apply the SSO jitter to the eye diagram. A testcase showed good correlation with SPICE transient analysis. Ted described JEDEC stressed eye tests, which would require IBIS-AMI to accept an external clock reference for the Rx DFE. He showed a proposal for IBIS-AMI to accept external clock times using the existing clock\_times argument to AMI\_GetWave, with a new External\_Clock Reserved\_Parameter to designate IBIS-AMI models capable of accepting the new input. Ted showed how applying the same sinusoidal jitter to DQ and DQS would result in the suppression of jitter in the resulting eye, by affecting DFE timing. If the jitter differs from DQ to DQS, it would propagate through to the decision point, however.

A question was asked about how the phase of SSO noise was handled. The answer was that it was a good question, and that it would need to be handled in the future.

### **CLOSING REMARKS**

Mike LaBonte closed the summit, thanking the sponsors, JEITA, the authors and presenters, and all participants. He encouraged all to consider proposing their ideas for IBIS through the BIRD process. The summit was adjourned.

### **NEXT MEETING**

The next IBIS Open Forum teleconference meeting will be held on November 30, 2018. The following IBIS Open Forum teleconference meeting is tentatively scheduled on December 21, 2018.

The Asian IBIS Summit in Shanghai will be held November 14, 2018. The Asian IBIS Summit in Taipei will be held November 16, 2018. No teleconferences will be available for the Summit meetings.

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### **NOTES**

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This meeting was conducted in accordance with ANSI guidance.

All inquiries may be sent to [info@ibis.org](mailto:info@ibis.org). Examples of inquiries are:

- To obtain general information about IBIS.
- To ask specific questions for individual response.
- To subscribe to the official [ibis@freelists.org](mailto:ibis@freelists.org) and/or [ibis-users@freelists.org](mailto:ibis-users@freelists.org) email lists (formerly [ibis@eda.org](mailto:ibis@eda.org) and [ibis-users@eda.org](mailto:ibis-users@eda.org)).
- To subscribe to one of the task group email lists: [ibis-macro@freelists.org](mailto:ibis-macro@freelists.org), [ibis-interconn@freelists.org](mailto:ibis-interconn@freelists.org), or [ibis-quality@freelists.org](mailto:ibis-quality@freelists.org).
- To inquire about joining the IBIS Open Forum as a voting Member.
- To purchase a license for the IBIS parser source code.
- To report bugs or request enhancements to the free software tools: `ibischk6`, `tschk2`, `icmchk1`, `s2ibis`, `s2ibis2` and `s2iplt`.

The BUG Report Form for `ibischk` resides along with reported BUGs at:

<http://www.ibis.org/bugs/ibischk/>  
<http://www.ibis.org/bugs/ibischk/bugform.txt>

The BUG Report Form for tschk2 resides along with reported BUGs at:

<http://www.ibis.org/bugs/tschk/>  
<http://www.ibis.org/bugs/tschk/bugform.txt>

The BUG Report Form for icmchk resides along with reported BUGs at:

<http://www.ibis.org/bugs/icmchk/>  
[http://www.ibis.org/bugs/icmchk/icm\\_bugform.txt](http://www.ibis.org/bugs/icmchk/icm_bugform.txt)

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

<http://www.ibis.org/bugs/s2ibis/bugs2i.txt>  
<http://www.ibis.org/bugs/s2ibis2/bugs2i2.txt>  
<http://www.ibis.org/bugs/s2iplt/bugsplt.txt>

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

<http://www.ibis.org/>

Check the IBIS file directory on ibis.org for more information on previous discussions and results:

<http://www.ibis.org/directory.html>

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## SAE STANDARDS BALLOT VOTING STATUS

Organization	Interest Category	Standards Ballot Voting Status	September	October	November	November
			21, 2018	12, 2018	2, 2018	12, 2018
ANSYS	User	Active	X	X	X	X
Applied Simulation Technology	User	Inactive	-	-	-	-
Broadcom Ltd.	Producer	Inactive	-	-	-	-
Cadence Design Systems	User	Active	-	X	X	X
Cisco Systems	User	Inactive	-	-	-	-
CST	User	Inactive	-	-	-	-
Ericsson	Producer	Active	-	-	X	X
GLOBALFOUNDRIES	Producer	Active	X	X	X	-
Huawei Technologies	Producer	Inactive	-	-	-	-
IBM	Producer	Inactive	-	-	X	-
Infineon Technologies AG	Producer	Inactive	X	-	-	-
Intel Corp.	Producer	Active	X	X	X	-
IO Methodology	User	Inactive	X	X	-	-
Keysight Technologies	User	Active	X	X	X	X
Maxim Integrated	Producer	Inactive	-	-	-	-
Mentor, A Siemens Business	User	Active	X	X	X	X
Micron Technology	Producer	Active	X	X	X	X
NXP	Producer	Inactive	-	-	-	-
Raytheon	User	Inactive	-	-	-	-
SiSoft	User	Active	X	X	X	X
Synopsys	User	Active	-	X	X	X
Teraspeed Labs	General Interest	Active	X	X	X	-
Xilinx	Producer	Inactive	-	-	-	-
ZTE Corp.	User	Inactive	-	-	-	-
Zuken	User	Inactive	-	-	-	X

Criteria for SAE member in good standing:

- Must attend two consecutive meetings to establish voting membership
- Membership dues current
- Must not miss two consecutive meetings

Interest categories associated with SAE standards ballot voting are:

- Users - members that utilize electronic equipment to provide services to an end user.
- Producers - members that supply electronic equipment.
- General Interest - members are neither producers nor users. This category includes, but is not limited to, government, regulatory agencies (state and federal), researchers, other organizations and associations, and/or consumers.